TELEDYNE LECROY
Everywhereyoulook™

980 DP1.4 USB-C/eDP Video Generator / Analyzer Module

User Guide

Rev: B1

Table of Contents

1 About the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer Module

This chapter provides an overview of features of the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module and the 980 GUI Manager. The module can be equipped the 980B Advanced Test Platform – 4-slot chassis with a 15 inch touch display

The 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module supports video pattern testing and audio testing of DP 1.4 capable displays at 8.1Gb/s link rates per 4 lanes. It is equipped with two (2) Tx ports and two (2) Rx port—one each for standard DisplayPort and USB-C with DP alt mode support. Only one of the Tx ports and one of the Rx ports can be active at any one time.

The 980 GUI Manager is a PC application to manage and use the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module.

1.1 Scope of this User Guide

This User Guide provides descriptive and procedural information on the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module for testing DP display devices.

Although you can operate the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module through the “embedded GUI,” most of the examples used in the procedures in this User Guide are taken from the external standalone PC 980 GUI Manager. The procedures are nearly identical between the embedded GUI running through the 980B/980R front panel display and the external standalone PC application but the look and feel is slightly different.

There are separate User Guides for the other 980 series modules. The following is a list of the User Guides available with the 980B/980R and its modules. These are available from the downloads and product web pages of the Quantum Data website http://www.quantumdata.com/products/980.asp:

The following is a list of the User Guides available for the 980 systems:

- 980 HDMI Protocol Analyzer Gen 3 System – Covers source analysis testing for HDMI and MHL source devices as well as various transmitter features. This user guide is specifically for the functions of the 980 HDMI Protocol Analyzer Gen 3 system sold through 2012.
- 980 HDMI Protocol Analyzer module – Covers source analysis features of the 980 HDMI Protocol Analyzer module. Used in conjunction with the 980 Advanced Test Platform Quick Start Guide for purchases in 2013.
- 980 Advanced Test Platform Quick Start Guide – Covers startup procedures for the 980/980B platform. Used in conjunction with the 980 HDMI Protocol Analyzer Module User Guide for purchases in 2013.

- 980 9G HDMI Protocol Analyzer module for HDMI Testing – Covers source analysis testing for HDMI source devices as well as various transmitter features. This user guide is specifically for the functions of the 980 HDMI Protocol Analyzer module equipped in one of the 980 Advanced Test Platform slots (980 Gen 3 or 980B). Used in conjunction with the 980 Advanced Test Platform Quick Start Guide.
- 980 9G HDMI Protocol Analyzer HDMI Source Compliance Test – Covers source compliance testing for both MHL and HDMI sources. These compliance test applications are provided by the 980 HDMI Protocol Analyzer module or the 980 HDMI Protocol Analyzer Gen 3 system. Used in conjunction with the 980 Advanced Test Platform Quick Start Guide.
- 980 9G HDMI Protocol Analyzer Sink Compliance Test – Covers sink compliance testing for both MHL and HDMI sinks (and MHL dongles). These compliance test applications are provided by the 980 HDMI Protocol Analyzer module or the 980 HDMI Protocol Analyzer Gen 3 system. Used in conjunction with the 980 Advanced Test Platform Quick Start Guide.
- 980 18G Video Generator module for HDMI Testing – Covers the features and functions offered by the 980 18G Video Generator module. Used in conjunction with the 980 Advanced Test Platform Quick Start Guide.
- 980 18G Protocol Analyzer module for HDMI Testing – Covers source analysis features of the 980 HDMI 2.0 Protocol Analyzer module. Used in conjunction with the 980 Advanced Test Platform Quick Start Guide.
- 980 DP 1.4 Video Generator / Analyzer module – Covers the features and functions offered by the 980 DP Video Generator module. Used in conjunction with the 980 Advanced Test Platform Quick Start Guide.
- 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module (This User Guide) – Covers the features and functions offered by the 980 DP USB-C/eDP Video Generator module. Used in conjunction with the 980 Advanced Test Platform Quick Start Guide.

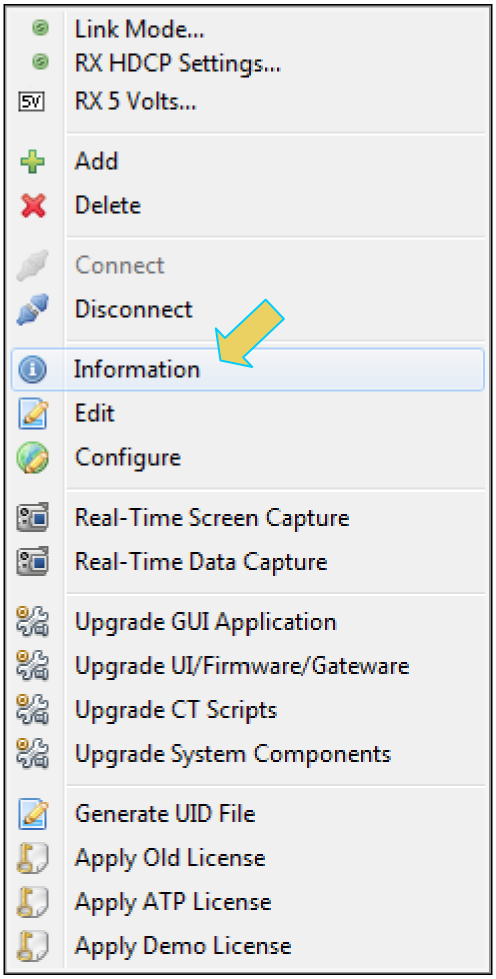
1.2 Changes to this User Guide

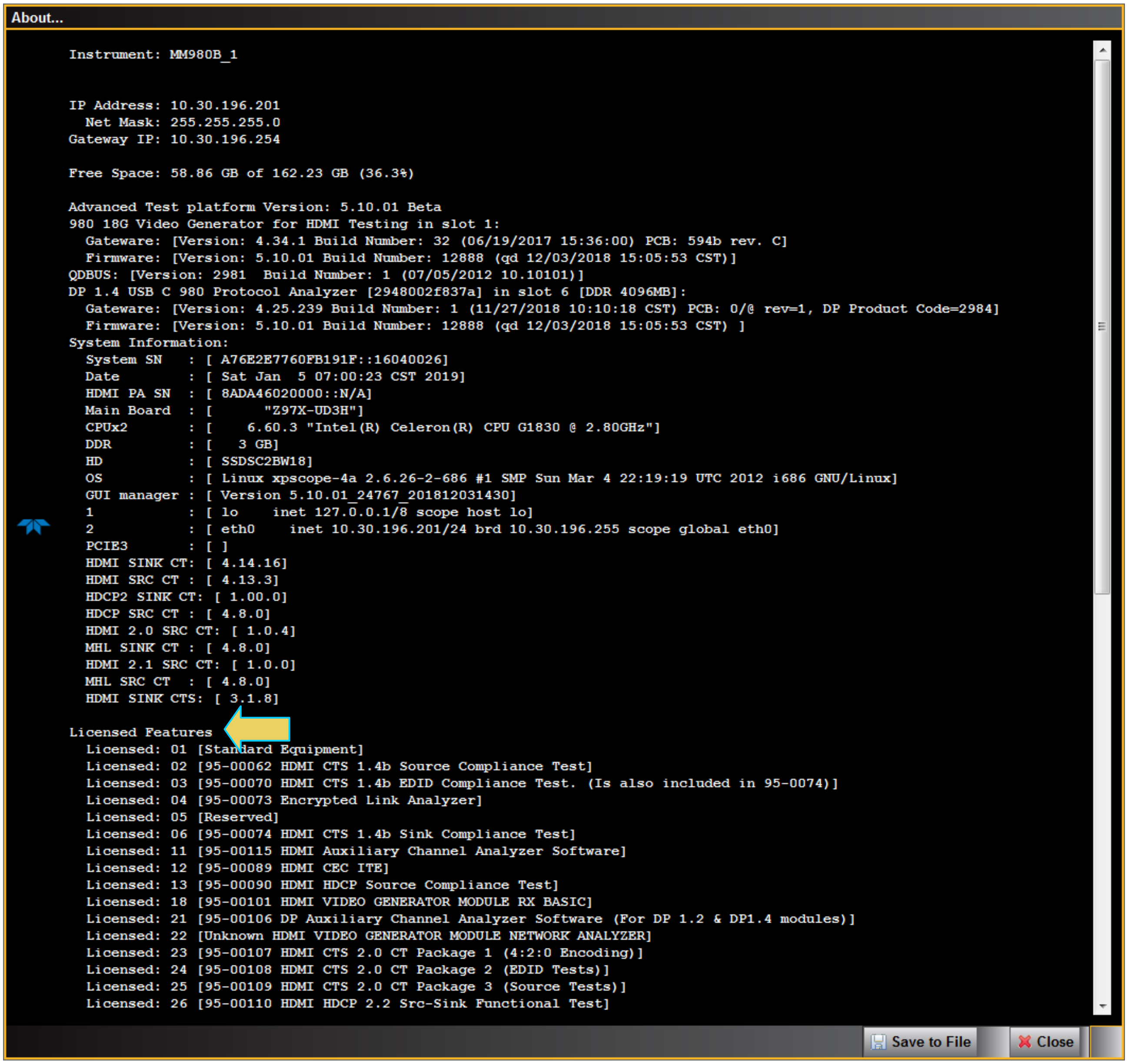
This User Guide has been enhanced to cover eDP features.

Note: Please be sure to check the Quantum Data website for updates to this User Guide.

1.3 What options are available with the 980?

You can determine what options the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer is equipped with by accessing the Instrument Information screen on either the built-in or external 980 GUI manager. When using the external 980 GUI Manager you must be connected to the 980B/980R in order to read the Instrument Information.


Link Mode...
RX HDCP Settings...
RX 5 Volts...
Add
Delete
Connect
Disconnect
Information
Edit
Configure
Real-Time Screen Capture
Real-Time Data Capture
Upgrade GUI Application
Upgrade UI/Firmware/Gateware
Upgrade CT Scripts
Upgrade System Components
Generate UID File
Apply Old License
Apply ATP License
Apply Demo License



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Instrument: MM980B_1


IP Address: 10.30.196.201
  Net Mask: 255.255.255.0
Gateway IP: 10.30.196.254

Free Space: 58.86 GB of 162.23 GB (36.3%)

Advanced Test platform Version: 5.10.01 Beta
980 18G Video Generator for HDMI Testing in slot 1:
  Gateware: [Version: 4.34.1 Build Number: 32 (06/19/2017 15:36:00) PCB: 594b rev. C]
  Firmware: [Version: 5.10.01 Build Number: 12888 (qd 12/03/2018 15:05:53 CST)]
QDBUS: [Version: 2981  Build Number: 1 (07/05/2012 10.10101)]
DP 1.4 USB C 980 Protocol Analyzer [2948002f837a] in slot 6 [DDR 4096MB]:
  Gateware: [Version: 4.25.239 Build Number: 1 (11/27/2018 10:10:18 CST) PCB: 0/@ rev=1, DP Product Code=2984]
  Firmware: [Version: 5.10.01 Build Number: 12888 (qd 12/03/2018 15:05:53 CST) ]
System Information:
  System SN    : [ A76E2E7760FB191F::16040026]
  Date         : [ Sat Jan  5 07:00:23 CST 2019]
  HDMI PA SN   : [ 8ADA46020000::N/A]
  Main Board   : [      "Z97X-UD3H"]
  CPUx2        : [    6.60.3 "Intel(R) Celeron(R) CPU G1830 @ 2.80GHz"]
  DDR          : [   3 GB]
  HD           : [ SSDSC2BW18]
  OS           : [ Linux xpscope-4a 2.6.26-2-686 #1 SMP Sun Mar 4 22:19:19 UTC 2012 i686 GNU/Linux]
  GUI manager : [ Version 5.10.01_24767_201812031430]
  1            : [ lo    inet 127.0.0.1/8 scope host lo]
  2            : [ eth0    inet 10.30.196.201/24 brd 10.30.196.255 scope global eth0]
  PCIE3        : [ ]
  HDMI SINK CT: [ 4.14.16]
  HDMI SRC CT : [ 4.13.3]
  HDCP2 SINK CT: [ 1.00.0]
  HDCP SRC CT : [ 4.8.0]
  HDMI 2.0 SRC CT: [ 1.0.4]
  MHL SINK CT : [ 4.8.0]
  HDMI 2.1 SRC CT: [ 1.0.0]
  MHL SRC CT  : [ 4.8.0]
  HDMI SINK CTS: [ 3.1.8]

Licensed Features
  Licensed: 01 [Standard Equipment]
  Licensed: 02 [95-00062 HDMI CTS 1.4b Source Compliance Test]
  Licensed: 03 [95-00070 HDMI CTS 1.4b EDID Compliance Test. (Is also included in 95-0074)]
  Licensed: 04 [95-00073 Encrypted Link Analyzer]
  Licensed: 05 [Reserved]
  Licensed: 06 [95-00074 HDMI CTS 1.4b Sink Compliance Test]
  Licensed: 11 [95-00115 HDMI Auxiliary Channel Analyzer Software]
  Licensed: 12 [95-00089 HDMI CEC ITE]
  Licensed: 13 [95-00090 HDMI HDCP Source Compliance Test]
  Licensed: 18 [95-00101 HDMI VIDEO GENERATOR MODULE RX BASIC]
  Licensed: 21 [95-00106 DP Auxiliary Channel Analyzer Software (For DP 1.2 & DP1.4 modules)]
  Licensed: 22 [Unknown HDMI VIDEO GENERATOR MODULE NETWORK ANALYZER]
  Licensed: 23 [95-00107 HDMI CTS 2.0 CT Package 1 (4:2:0 Encoding)]
  Licensed: 24 [95-00108 HDMI CTS 2.0 CT Package 2 (EDID Tests)]
  Licensed: 25 [95-00109 HDMI CTS 2.0 CT Package 3 (Source Tests)]
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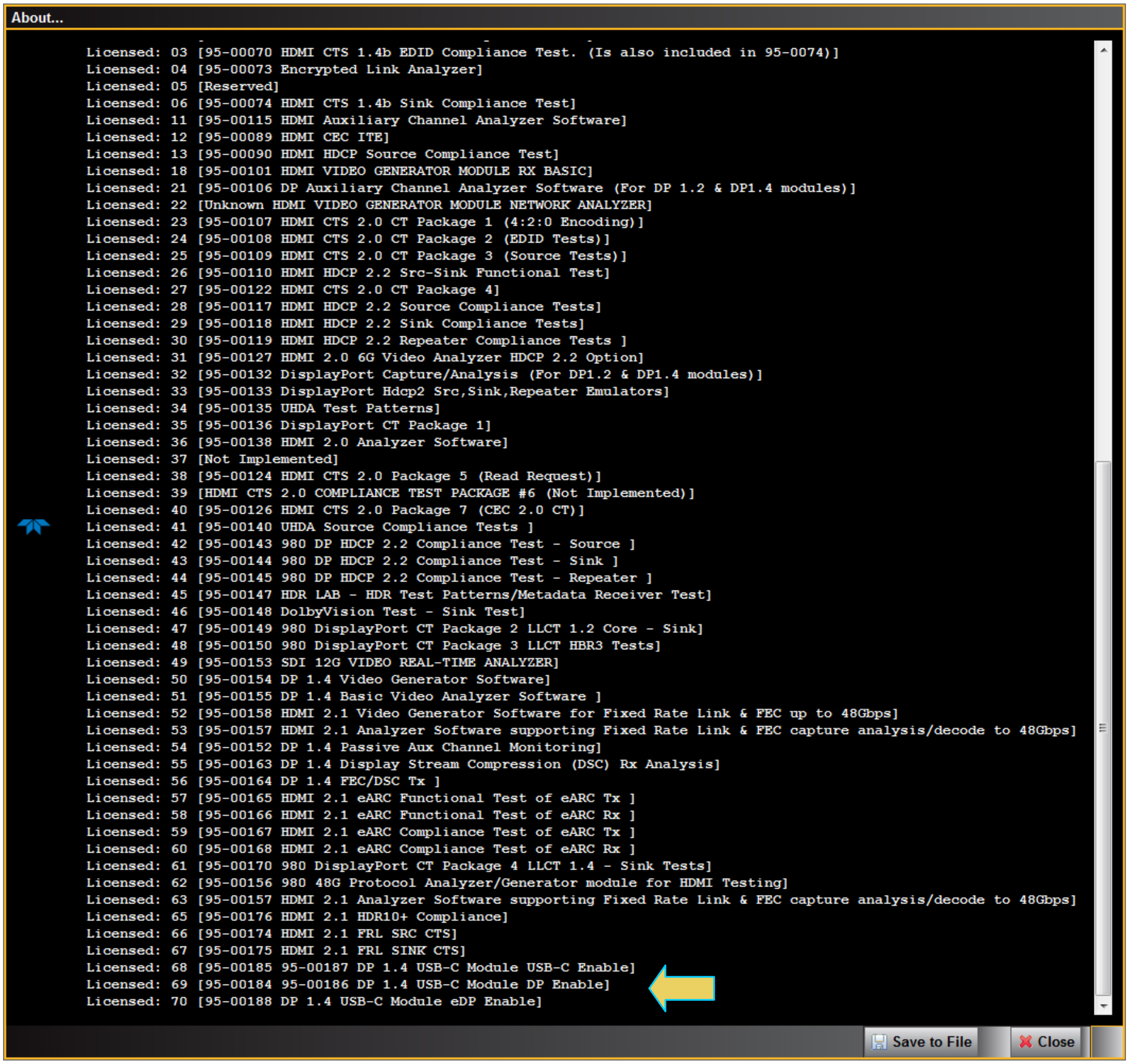

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Licensed: 11 [95-00115 HDMI Auxiliary Channel Analyzer Software]
Licensed: 12 [95-00089 HDMI CEC ITE]
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Licensed: 18 [95-00101 HDMI VIDEO GENERATOR MODULE RX BASIC]
Licensed: 21 [95-00106 DP Auxiliary Channel Analyzer Software (For DP 1.2 & DP1.4 modules)]
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Licensed: 31 [95-00127 HDMI 2.0 6G Video Analyzer HDCP 2.2 Option]
Licensed: 32 [95-00132 DisplayPort Capture/Analysis (For DP1.2 & DP1.4 modules)]
Licensed: 33 [95-00133 DisplayPort Hdcp2 Src,Sink,Repeater Emulators]
Licensed: 34 [95-00135 UHDA Test Patterns]
Licensed: 35 [95-00136 DisplayPort CT Package 1]
Licensed: 36 [95-00138 HDMI 2.0 Analyzer Software]
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Licensed: 51 [95-00155 DP 1.4 Basic Video Analyzer Software ]
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Licensed: 53 [95-00157 HDMI 2.1 Analyzer Software supporting Fixed Rate Link & FEC capture analysis/decode to 48Gbps]
Licensed: 54 [95-00152 DP 1.4 Passive Aux Channel Monitoring]
Licensed: 55 [95-00163 DP 1.4 Display Stream Compression (DSC) Rx Analysis]
Licensed: 56 [95-00164 DP 1.4 FEC/DSC Tx ]
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Licensed: 67 [95-00175 HDMI 2.1 FRL SINK CTS]
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Licensed: 70 [95-00188 DP 1.4 USB-C Module eDP Enable]
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1.4 980 User Interface

The 980B/980R provide a graphical user interface for operation. This GUI can run both on the 980B/980R through the built-in color touch screen display or as a standalone application running on a PC. The look and feel and functions are similar but not identical. The first illustration below shows a PC (left) connected to the 980B through an Ethernet cable for operation through the external 980 GUI Manager. The second illustration depicts the embedded 980 GUI Manager.

1.4.1 External 980 GUI Manager

The external 980B GUI Manager provides convenient operation of the 980 DP 1.4 Video Generator module from your PC. The larger screen size on the external 980 GUI Manager enables you to use multiple panels at the same time.

1.4.2 Embedded 980 GUI Manager

You can operate the 980B/980R fully through the built-in color touch screen display.

2 Getting Started

This chapter explains what is involved in getting your 980B/980R system up and operating to capture data.

2.1 What is shipped with the 980 DP Video Generator / Analyzer module?

The 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module can optionally be equipped in the 980B/980R Advanced Test Platforms. The following items are included with the 980 DP Video Generator / Analyzer module:

- DP cable (P/N 30-00162) – used for connecting to the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module to the device under test.
- USB-C to USB-C cable (P/N 42A0000009033) – One (1) meter cable used for connecting to the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module from either the USB-C Tx or Rx ports to the USB-C source or display device under test.

2.2 Operational workflow for DP Video Pattern Testing

The following are the high level steps you will need to follow to get your 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module up and running.

2.2.1 Procedures covered in 980 Advanced Test Platform Quick Start Guide:

The following list of activities are described in the 980 Quick Start Guide.

1. Remove the 980B from the shipping box.
2. Assemble the source device under test into your lab area and power it up.
3. Connect the 980B power cable (provided) to a suitable outlet (110-240V 50/60Hz) and apply power to the 980.
4. (Optional – not required if using the built-in display) Select a suitable PC to host the 980 GUI Manager application. A minimum of 512MB of RAM is recommended. (Note that you do not need a PC because you can use the built-in Front Panel display; however the external 980 GUI Manager provides you with a larger viewing area).
5. (Optional – not required if using the built-in display) Determine how you are going to connect to the 980/980B from the external 980 GUI Manager in order to operate the instrument:
    - Put the 980B on your corporate network and enable DHCP using an available Ethernet patch cable, or…
    - Connect directly with a host PC or laptop using the Ethernet crossover cable provided.
6. (Optional – not required if using the built-in display) Assign an IP address to the 980B/980R either directly or by enabling DHCP.
7. (Optional – not required if using the built-in display) Download the latest 980 GUI Manager application from the Quantum Data website:
   www.quantumdata.com/downloads.html.
8. (Optional – not required if using the built-in display) Install the 980 Manager application on your host PC.
9. (Optional – not required if using the built-in display) Establish a connection to the 980B from the 980 Manager resident on your host PC.
10. (Optional – not required if using the built-in display) Through the 980 Manager “Add” the 980B as an Instrument.

2.2.2 Procedures covered in this User Guide:

1. Connect the sink device under test to the DP Tx port on the 980 DP Video Generator / Analyzer module.
2. Selecting video formats (resolutions).
3. Setting the colorimetry and video mode.
4. Selecting the test patterns.
5. Running other tests on DP sink devices.

3 Testing DP Displays with the 980 DP Video Generator / Analyzer module

This chapter describes how to operate the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module to test DP display devices (HDTVs, PC monitors).

3.1 Workflow for running the video pattern testing of DP displays

The workflow below is a high level set of tasks for operating the 980 DP Video Generator / Analyzer module. Note that the installation of the external 980 GUI Manager and the Ethernet session are optional; you can run the tests through the embedded GUI Manager.

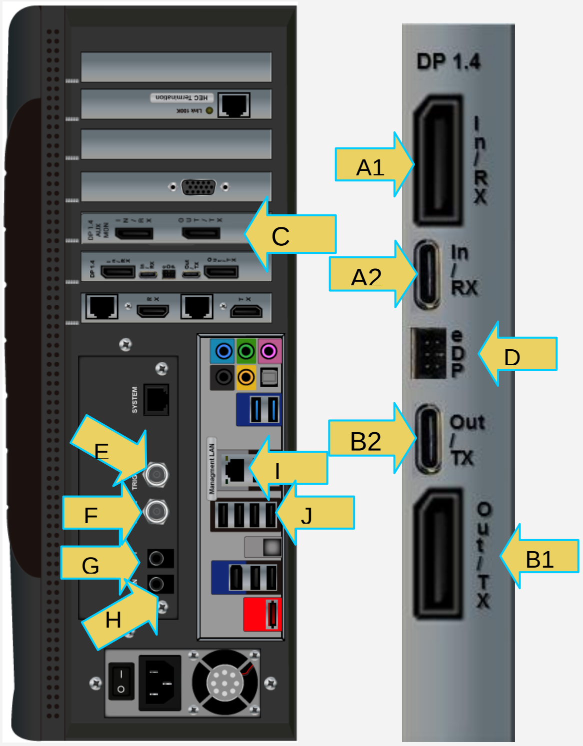
1. Power up the 980. Refer to the procedures in Powering up the 980.

   Note: The power switch in the front is used when you are turning off the 980 for a short period of time. For extended periods of off time, it is best to power the 980 down by first using the power button on the front and then the rocker switch on the back.

2. (Optional) Establish an Ethernet/IP connection between the external 980 GUI Manager and the 980B/980R Advanced Test Platform using the procedures in the 980 Advanced Test Platform Quick Start Guide.
3. Connect the DP sink device under test to one of the module’s Tx ports (DP or USB-C).
4. Access the module’s interface through the 980 GUI Manager.
5. Select DP.
6. Select the formats (timing or resolution).
7. Select the test patterns you wish to test with.
8. Select any video options and settings.
9. Select the audio format.
10. Monitor the sink DUT for any anomalies.

3.2 Connector Description

Use the following table to identify the connector function and descriptions on your 980 DP 1.4 Video Generator module.

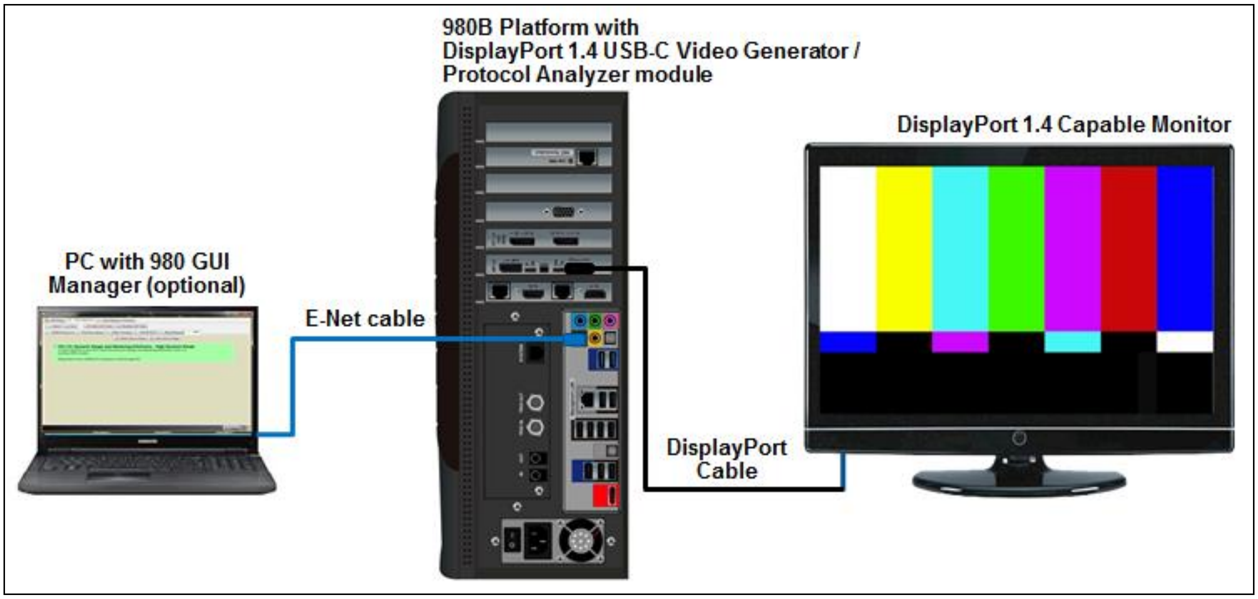
980 Configurations	Information / Function
DP Video Generator module – 980B  	The following is a description of each connector: **980 DP Video Generator / Analyzer module:** ▪ A1 – DP Rx port for analyzing DP sources. ▪ A2 – USB-C DP Alt Mode port for analyzing DP sources. ▪ B1 – DP Tx port for DP video/audio generation. ▪ B2 – USB-C DP Alt Mode port for testing DP sinks. ▪ D – eDP Pins for testing eDP functions. **Note**: This eDP pin header is not currently functional. **980 DP Video Generator / Analyzer Aux Board module:** ▪ C – DP Aux Passive Monitoring module Tx and Rx for passively monitoring the DP Aux Chan between a source and a display. **980B QD Bus Board:** ▪ E – BNC Trig OUT connector. Not used for this module. ▪ F – BNC Trig IN connector. Not used for this module. ▪ G – RCA OUT connector for SPDIF function. Not used for this module. ▪ H – RCA IN connector for SPDIF function. Not used for this module. **980B Lower Panel:** ▪ I – Ethernet port for connection to PC host for 980 GUI Manager application, telnet for command line control and FTP for transferring files. ▪ J – Various USB ports for transferring files and restoring system.

3.3 Making the physical DP connections

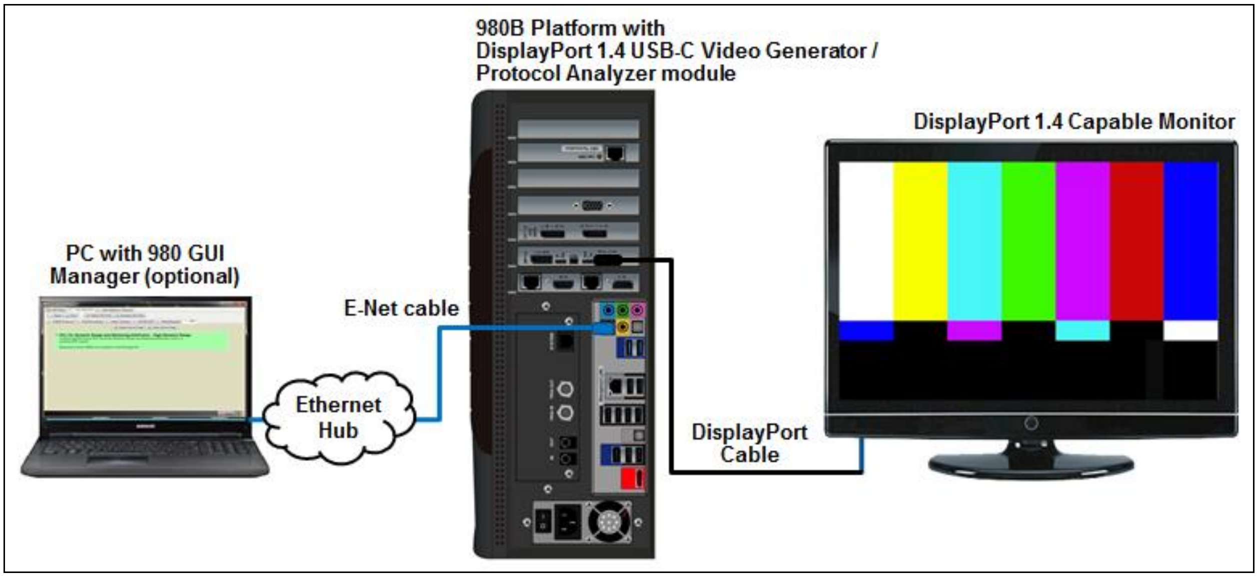
Important Note: Do not try and connect cables to the two DP Tx ports (standard DP and USB-C) or the two DP Rx ports (standard DP and USB-C).

Note: The 980 DP USB-C module will detect the connected cable, either standard DP or USB-C).

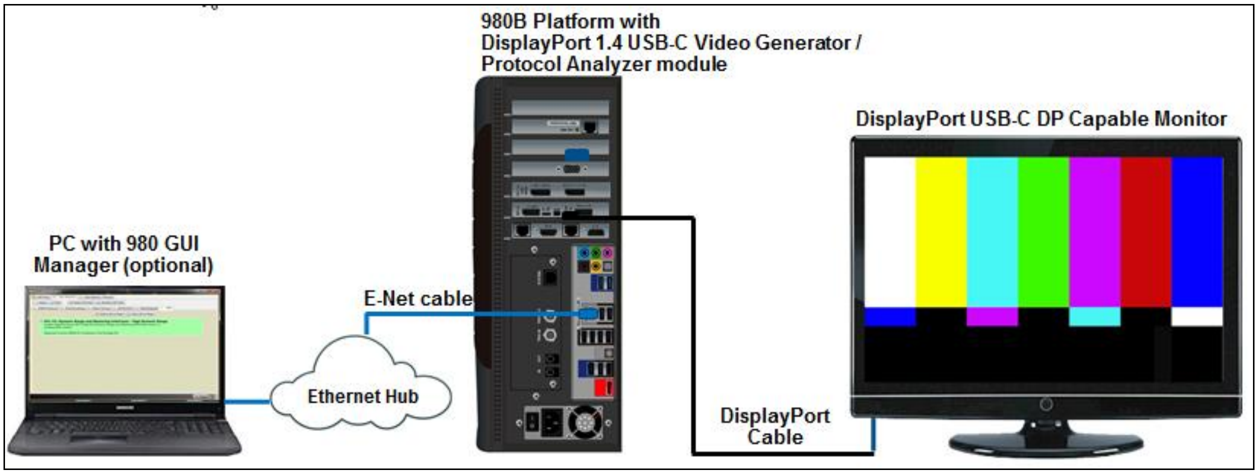
This subsection describes the physical DP connections required to run the video pattern tests on a DP display.



Connection for Video Display Testing Standard DP Port – 980B Direct Connection



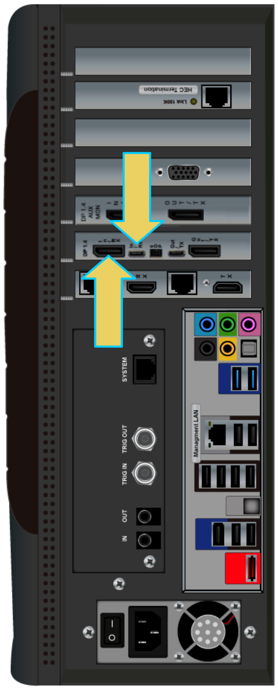
Connection for Video Display Testing with Standard DP Port – 980B Ethernet hub or corporate LAN example



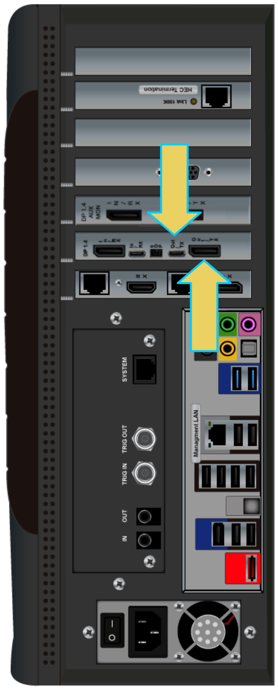
Connection for Video Display Testing with USB-C Port – 980B Ethernet hub or corporate LAN example

To make the physical DP connections:

This procedure assumes that you have assembled the 980B with the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module and the DP display device under test and applied power to all these devices. Refer to the procedures below and the diagram above. There are multiple connection scenarios depending on whether you are testing with the standard DP ports or the USB-C ports and whether you are testing a source or a sink.



Rx (Input) ports for source testing



Tx (Output) ports for sink testing

1. For source testing, connect your DP source device under test to one of the DP Rx (Standard DP or USB-C) connectors on the 980 DP Video Generator / Analyzer module.
2. For sink testing, connect your DP display device under test to one of the DP Tx (Standard DP or USB-C) connectors on the 980 DP Video Generator / Analyzer module.

Note: The DP Video Generator module can be installed in either slot 3 (shown) or slot 6 of the 980B and slot 1, 3 or 6 in the 980R.

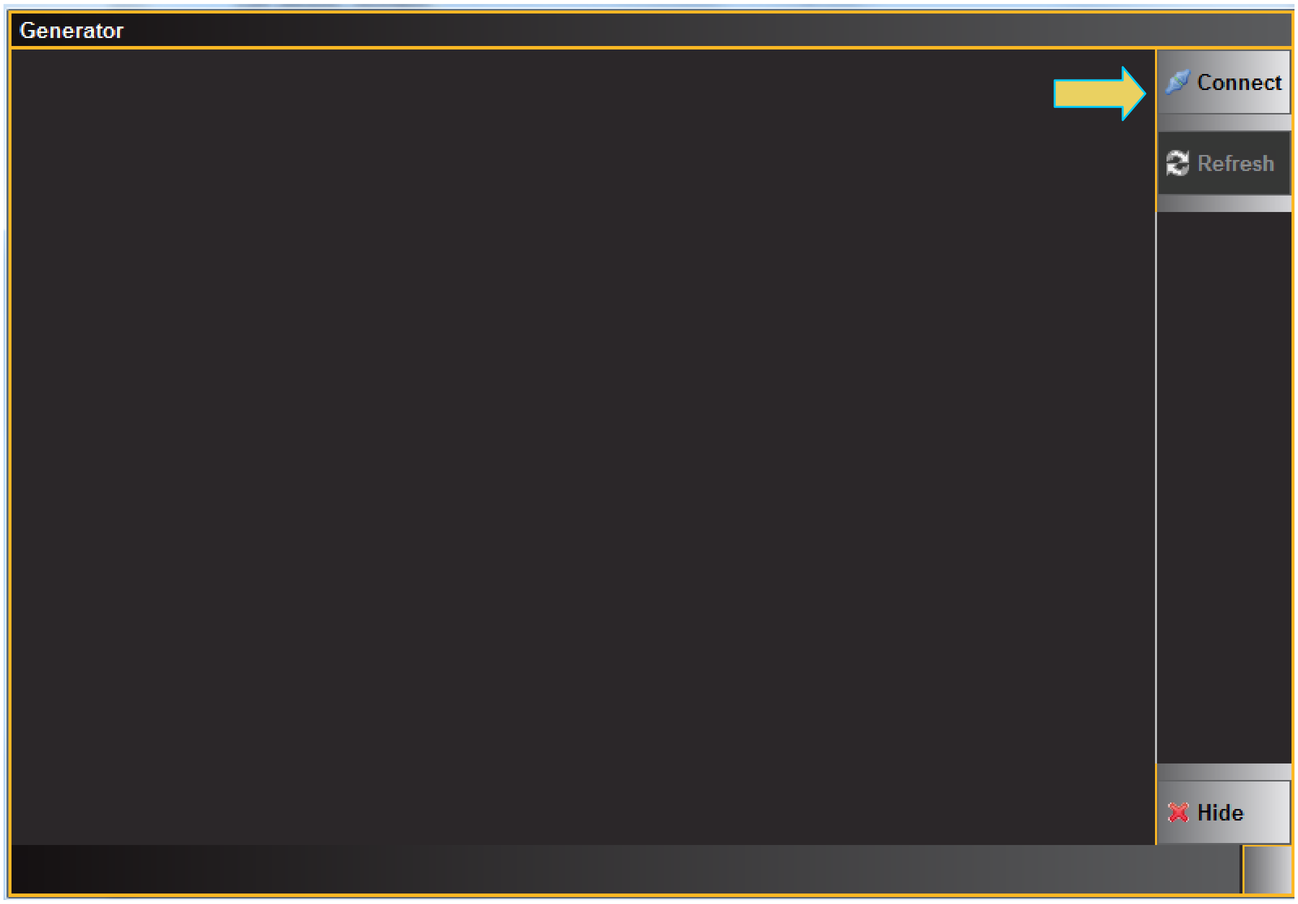
3.4 Navigating through the 980 GUI Manager interface

Use the following procedures to navigate to the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module testing functions. You can access the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module functionality through the Card Control tab (Page 1 of 4) of the Apps panel. Use the procedures provided below.

To navigate to the video test functions:

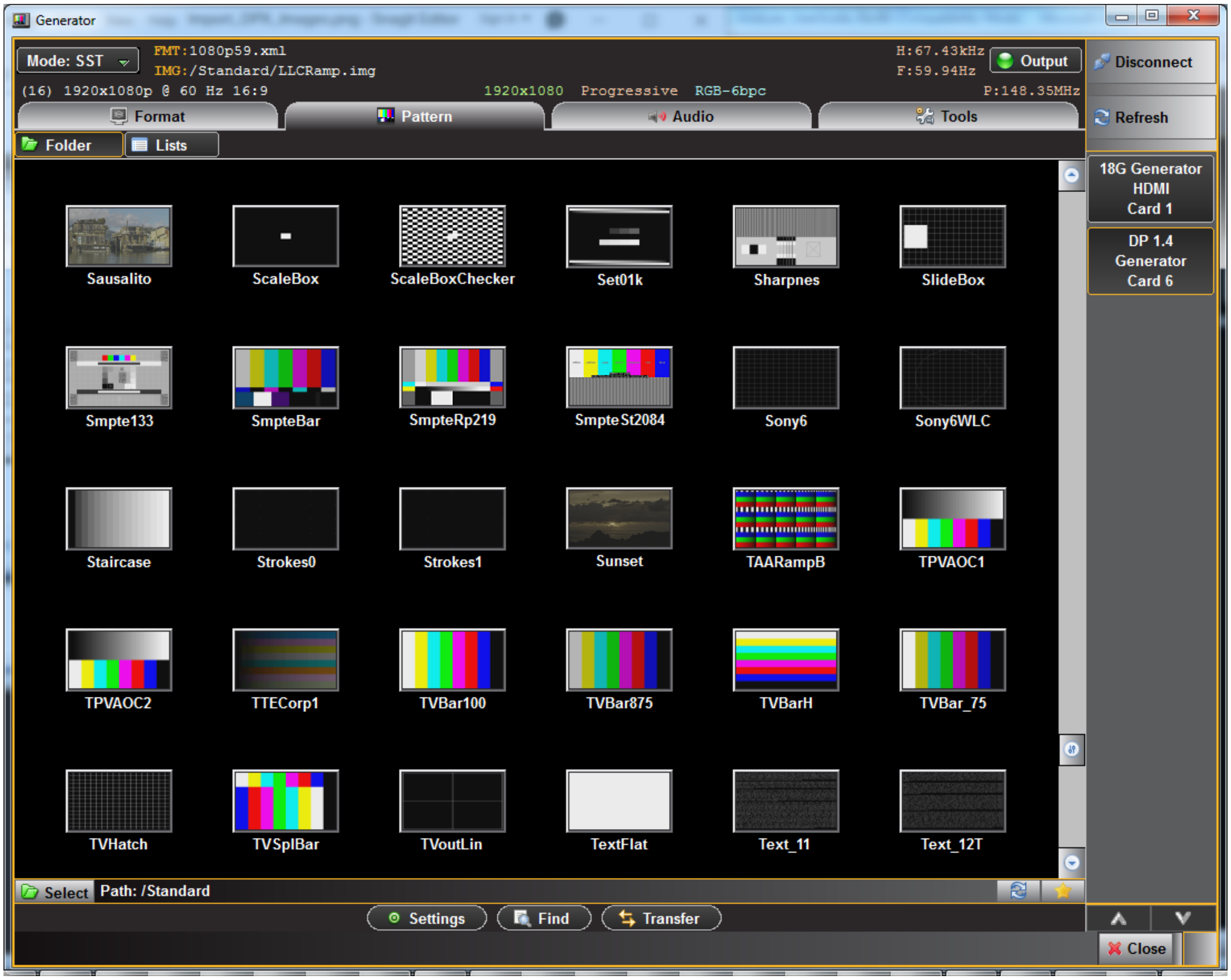
1. From the **View** menu, enable select the **Generator** item.

A blank **Generator** panel appears as shown below asking you to connect to the 980B/980R.

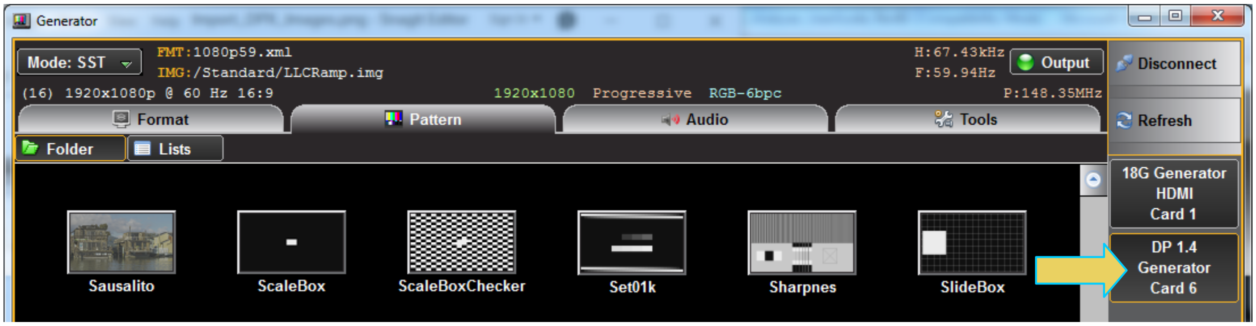


2. Click on the **Connect** button to initiate a connection between the 980 GUI Manager and the 980 Generator application.

   Once you establish the connection, the **Generator** panel will be populated as shown below:



There are a set of port selector/indicator buttons on the right side of the panel (indicated below). The module will be in one of slots 1 through 7 on the 980B.



The Generator screen has a status area on the top of its panel. The status area provides the following information:

Generator Status Area (Top)	
Item	**Description**
Port	Active port, in this case the two Tx connectors (T30 and T31).
INTF	The currently selected interface type for the module. This could be either, DP, HDMI or

Generator Status Area (Top)	
Item	**Description**
	DVI. The sampling mode is included in parentheses after the interface.
FMT	The currently active format (selected resolution) and its directory path.
IMG	The currently active image (selected test pattern) and its directory path.
Video Identification Code (VIC)	The VIC code is shown on the lower left of the upper status panel
Resolution, scan and color	The resolution, scan and colorimetry type are shown on in the lower portion of the upper status panel in the center.
H:(Rate)	The horizontal refresh rate of the selected timing.
F:(Rate)	The frame or vertical refresh rate of the selected timing.
P:(Pixel Rate)	The pixel clock rate of the selected timing.

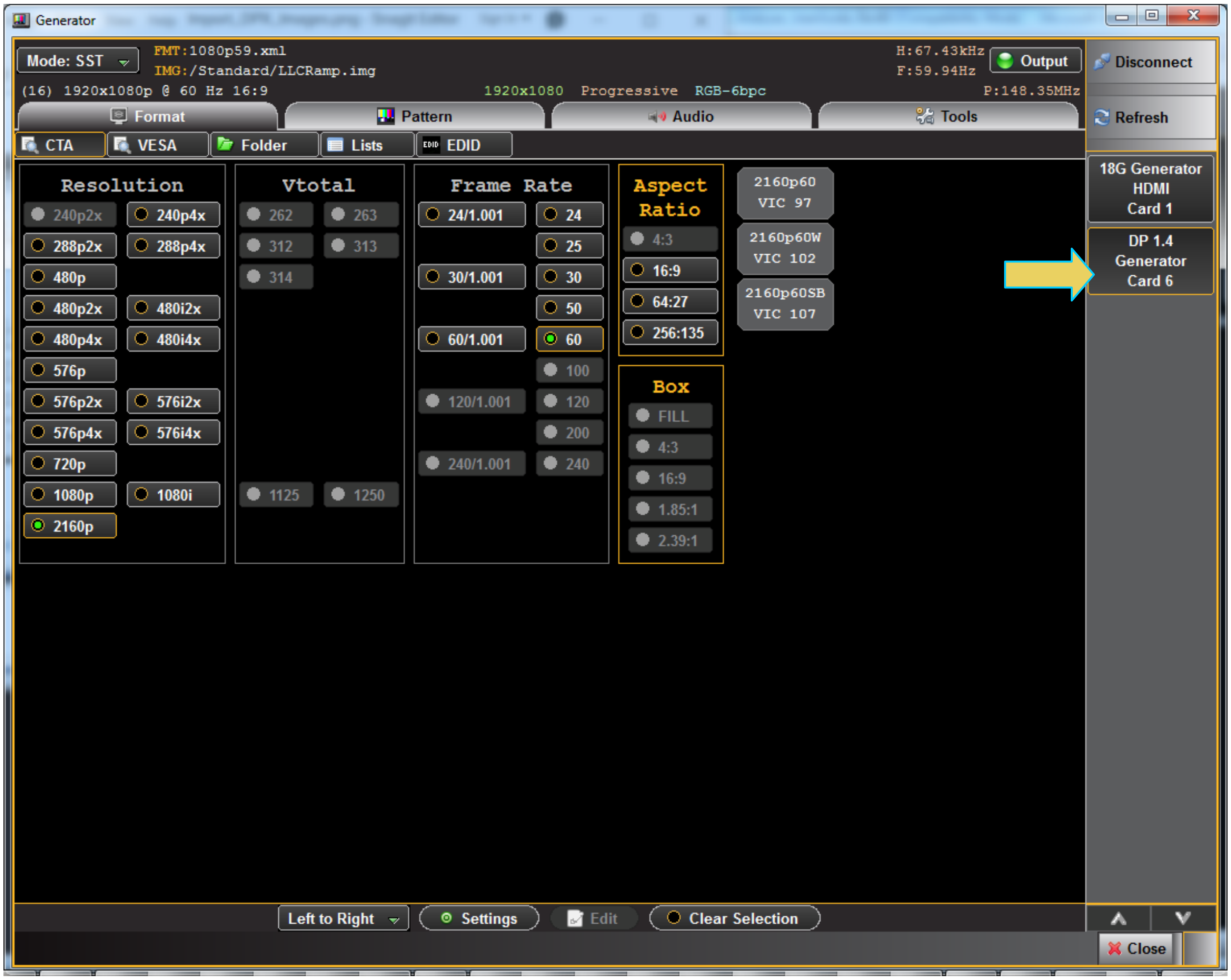
Please note that if you are also making changes through the command line the information in the status area is not automatically updated. You must click on the **Refresh** activation button to re-sync the status area.

3.5 Selecting DP formats

Use the following procedures to select the mode, DP, in the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module.

To select interface (DP):

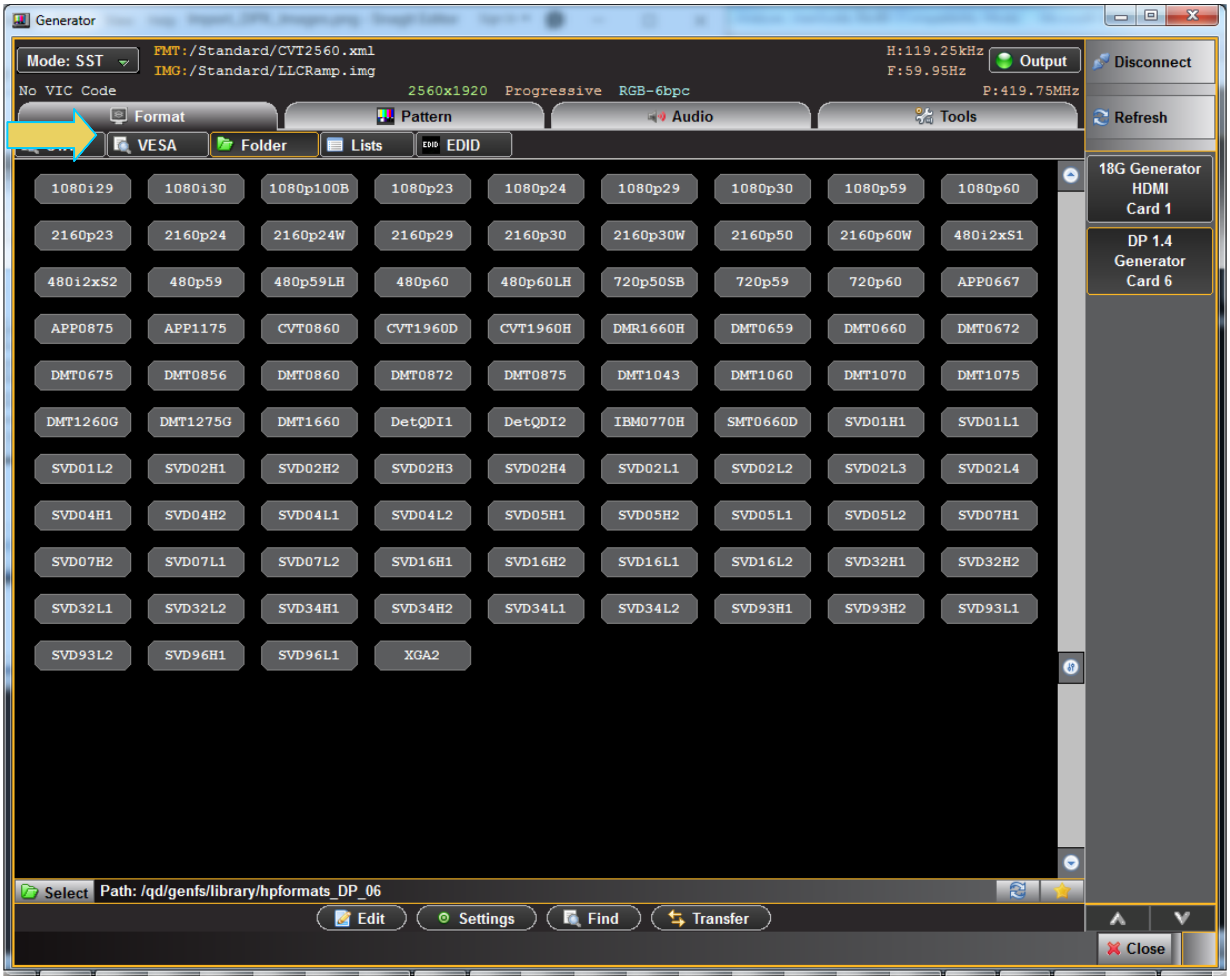
1. From the **Main** menu of the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module, click the **DisplayPort Generator Card** button on the right.



```
FMT:1080p59.xml
IMG:/Standard/LLCRamp.img
(16) 1920x1080p @ 60 Hz 16:9
1920x1080  Progressive  RGB-6bpc
H:67.43kHz
F:59.94Hz
P:148.35MHz
```

Mode: SST

When you select the DP module you will get a listing of DP formats in the main window.



FMT:/Standard/CVT2560.xml
IMG:/Standard/LLCRamp.img
H:119.25kHz
F:59.95Hz
No VIC Code
2560x1920 Progressive RGB-6bpc
P:419.75MHz
Path: /qd/genfs/library/hpformats_DP_06

3.6 Selecting formats (resolutions)

You can select formats (timings) from the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module’s format library or from the CEA parameter filters. When selecting from the Format Library list, you can select either from the entire list of formats or you can select from a subset or reduced set of the formats. You can select from a reduced set or subset of formats in either of two ways:

- Select from a custom list you have created using the Format List Editor.
- Select from a list of formats configured from the EDID of the connected display.

Use the following procedures to select a video resolution (format).

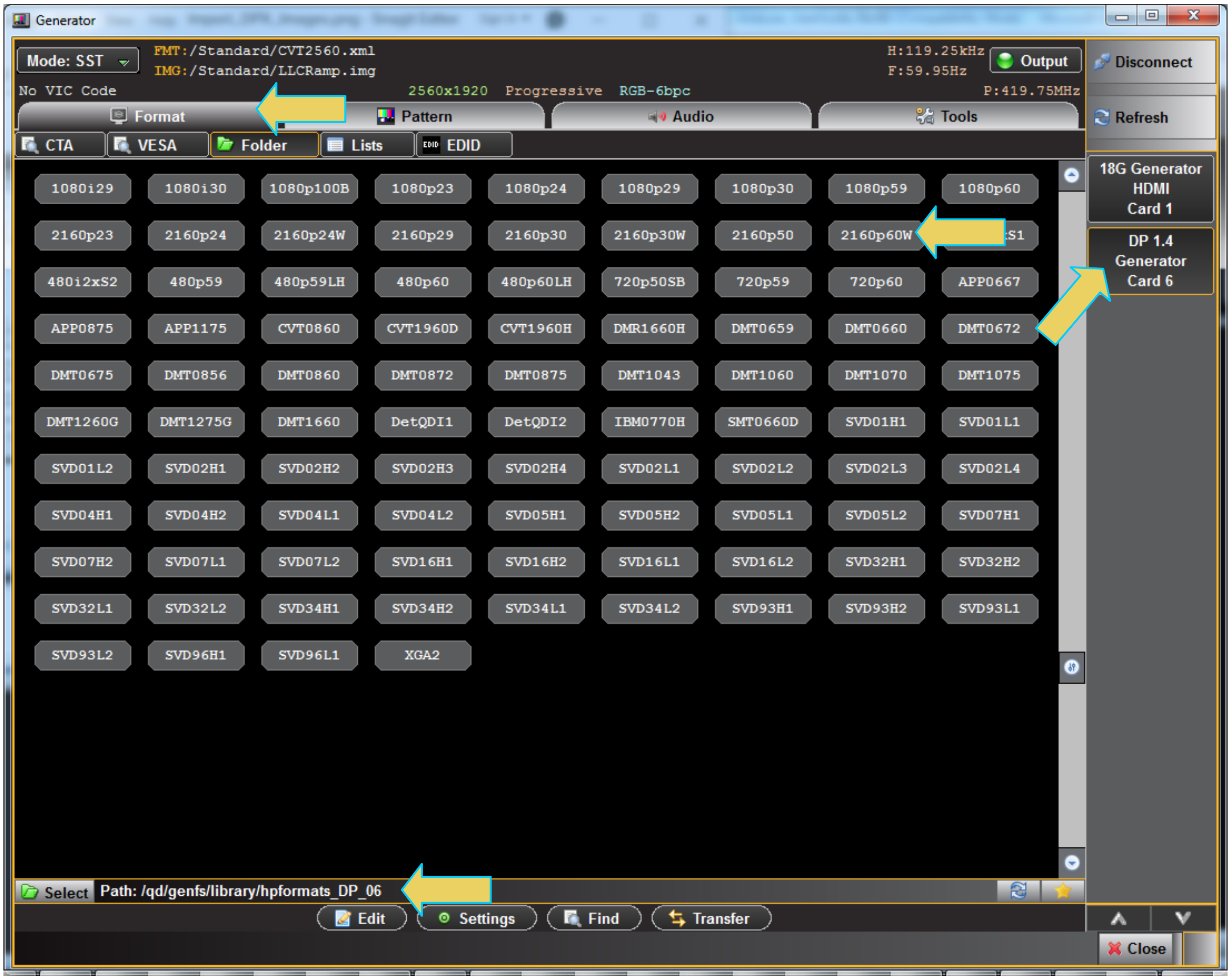
3.6.1 Selecting formats using the Library list

Use the following procedures to select a video resolution (format) using the Library List method. The procedure assumes that you have already selected the DP interface.

To select a format from the library list:

1. From the main window of the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module, click the **Format** tab.

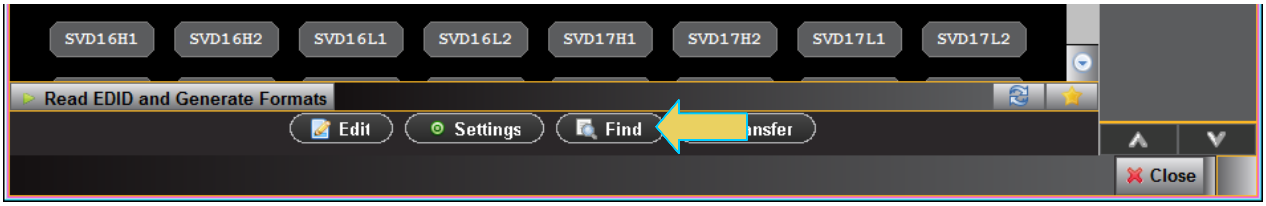
   A list of DP, HDMI or DVI formats will appear as shown in the example below.



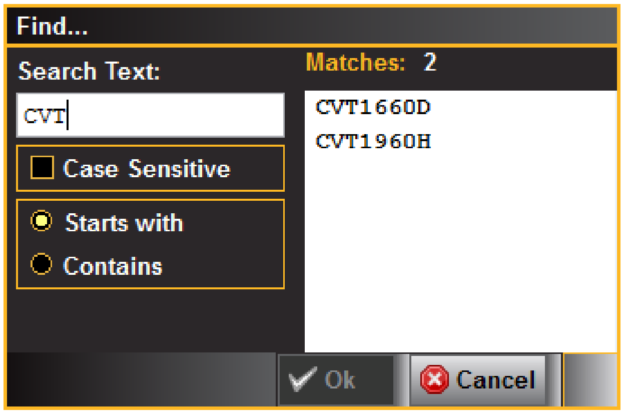
The highlighted format is the format that is active. You can also determine this from the status information at the top of the panel. Alternatively you can click on the Star ★ button to show the selected format. When you click on the Star button the list of formats will be repositioned such that the selected format is shown on the top line.

Note that you can browse for a format using the scroll bar. You can also search for a format using a test strings on the Find Format dialog box.

2. Select a format from the list by clicking on it.
3. Click on the Find activation button on the lower portion of the Format panel.



The **Find Format** dialog box appears as shown below. Enter a string in the Search Text field to find a format. You can specify either Starts with or Contains using the radio buttons and you select the Case Sensitive check box to indicate case sensitivity in your text. Click on the **OK** button when you have located the format.



Search Text: CVT

☐ Case Sensitive

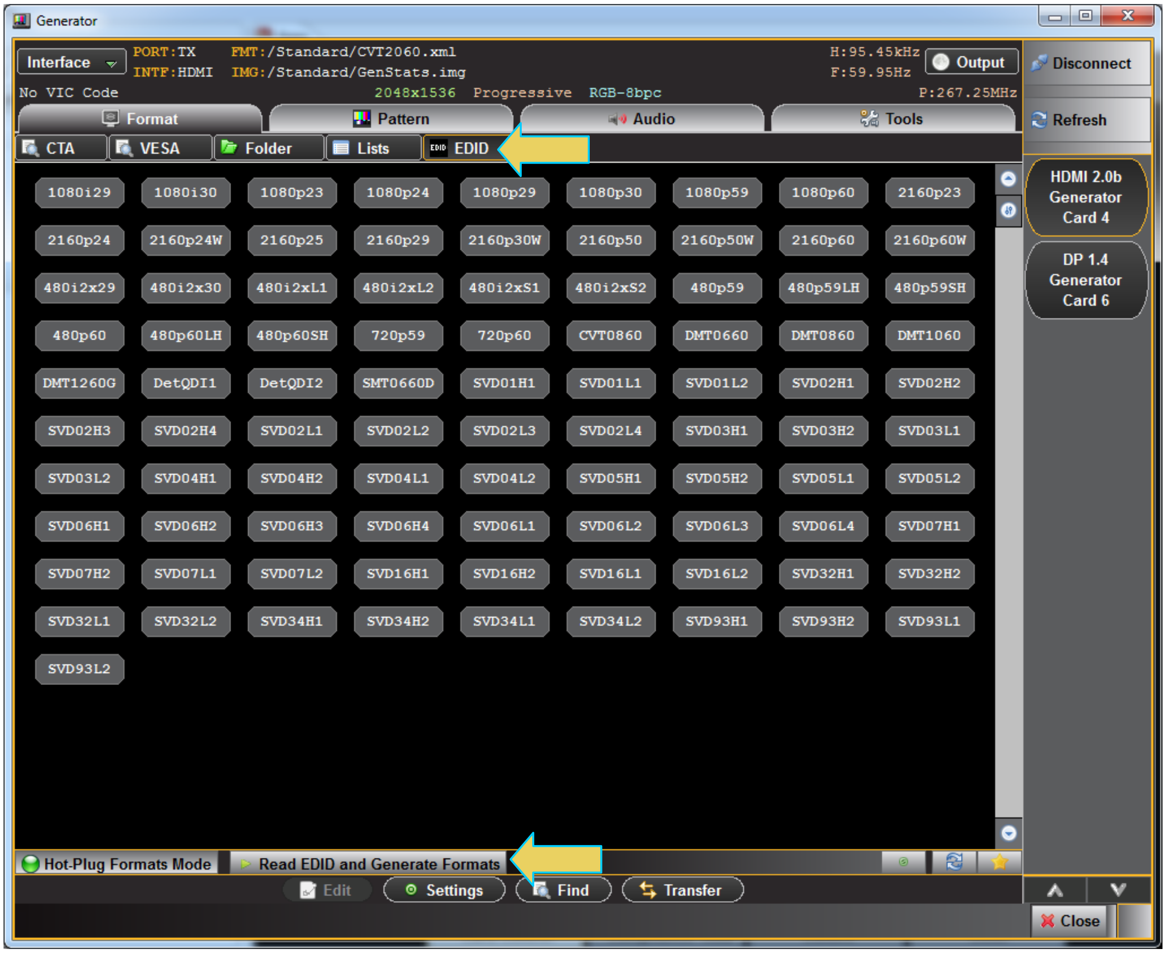
● Starts with

○ Contains

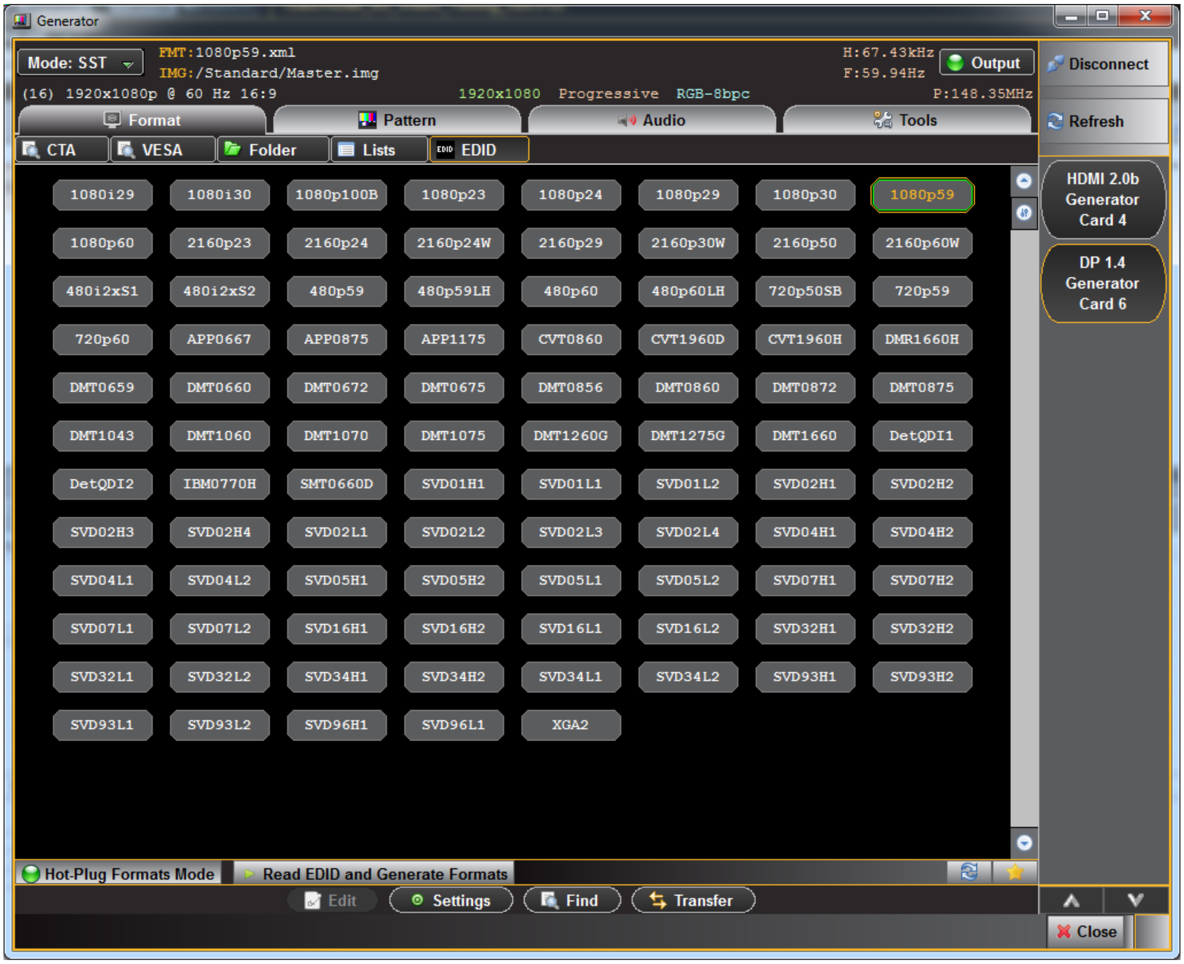
Matches: 2

CVT1660D
CVT1960H

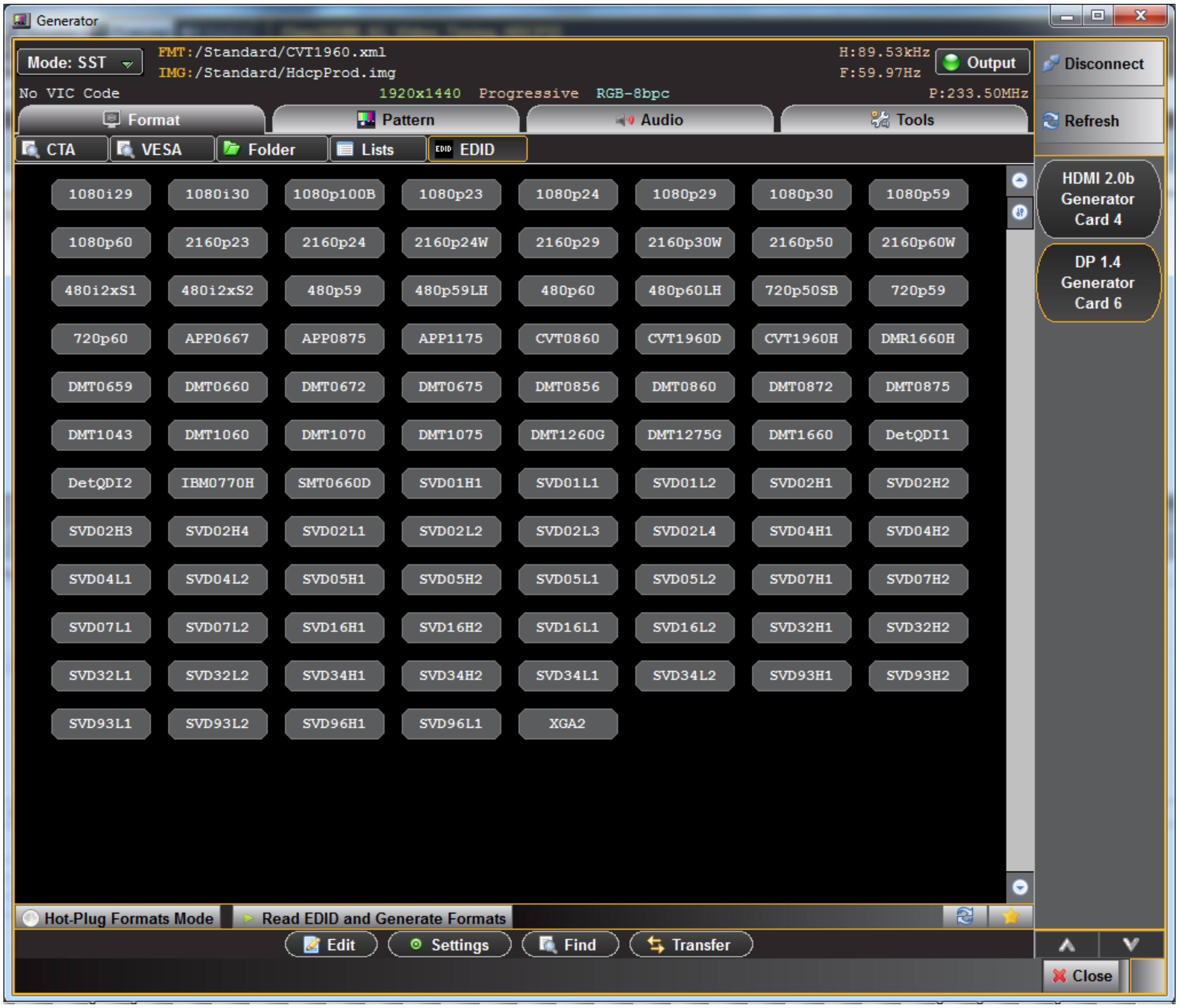
4. Click on the EDID smart activation button on the top left to configure the list of formats in accordance with the EDID for the connected display.



```
PORT:TX    FMT:/Standard/CVT2060.xml              H:95.45kHz
INTF:HDMI  IMG:/Standard/GenStats.img             F:59.95Hz
No VIC Code         2048x1536  Progressive  RGB-8bpc     P:267.25MHz
```



FMT:1080p59.xml
IMG:/Standard/Master.img
(16) 1920x1080p @ 60 Hz 16:9
1920x1080 Progressive RGB-8bpc
H:67.43kHz
F:59.94Hz
P:148.35MHz



Mode: SST

FMT:/Standard/CVT1960.xml

IMG:/Standard/HdcpProd.img

H:89.53kHz

F:59.97Hz

No VIC Code

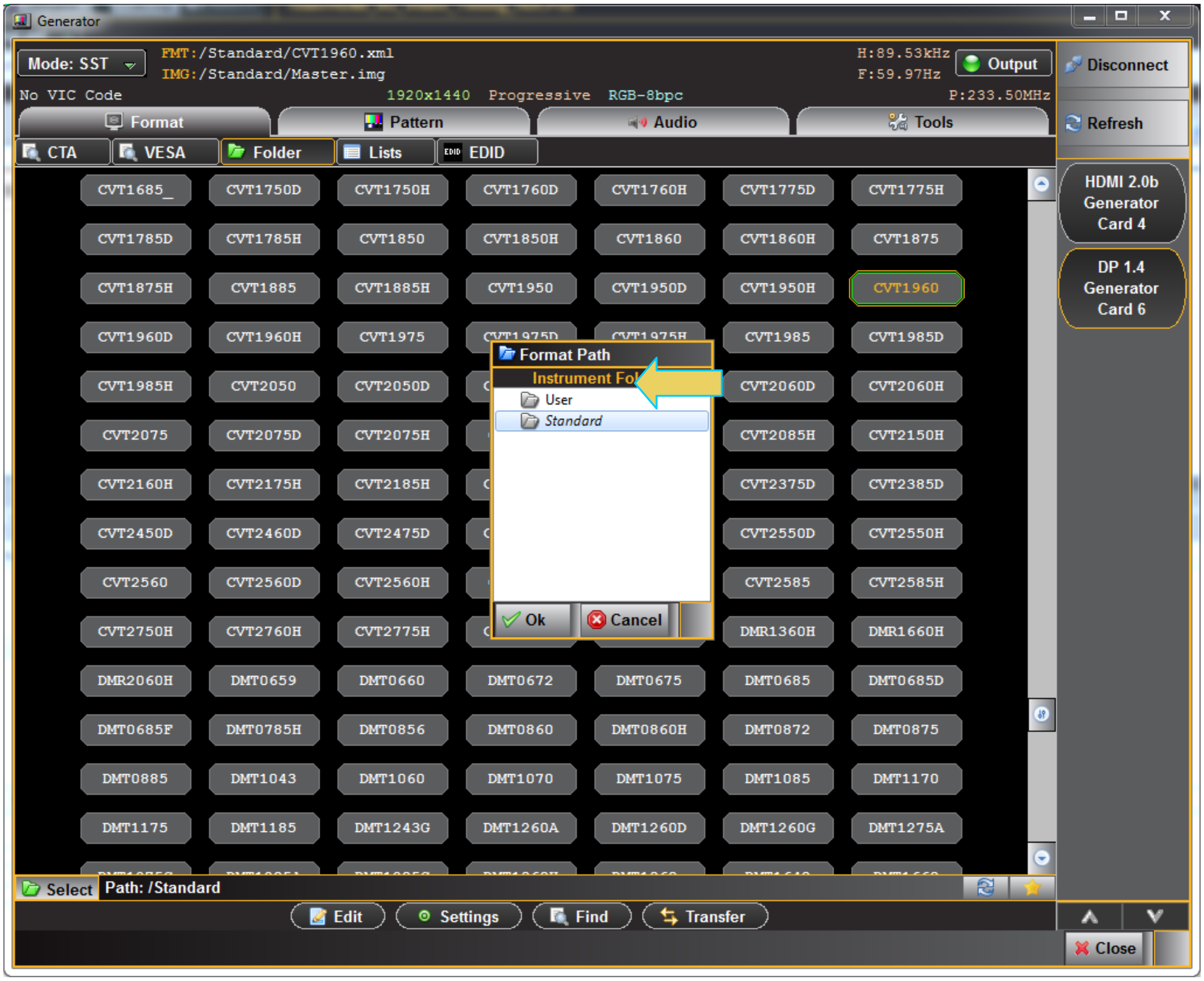
1920x1440 Progressive RGB-8bpc

P:233.50MHz

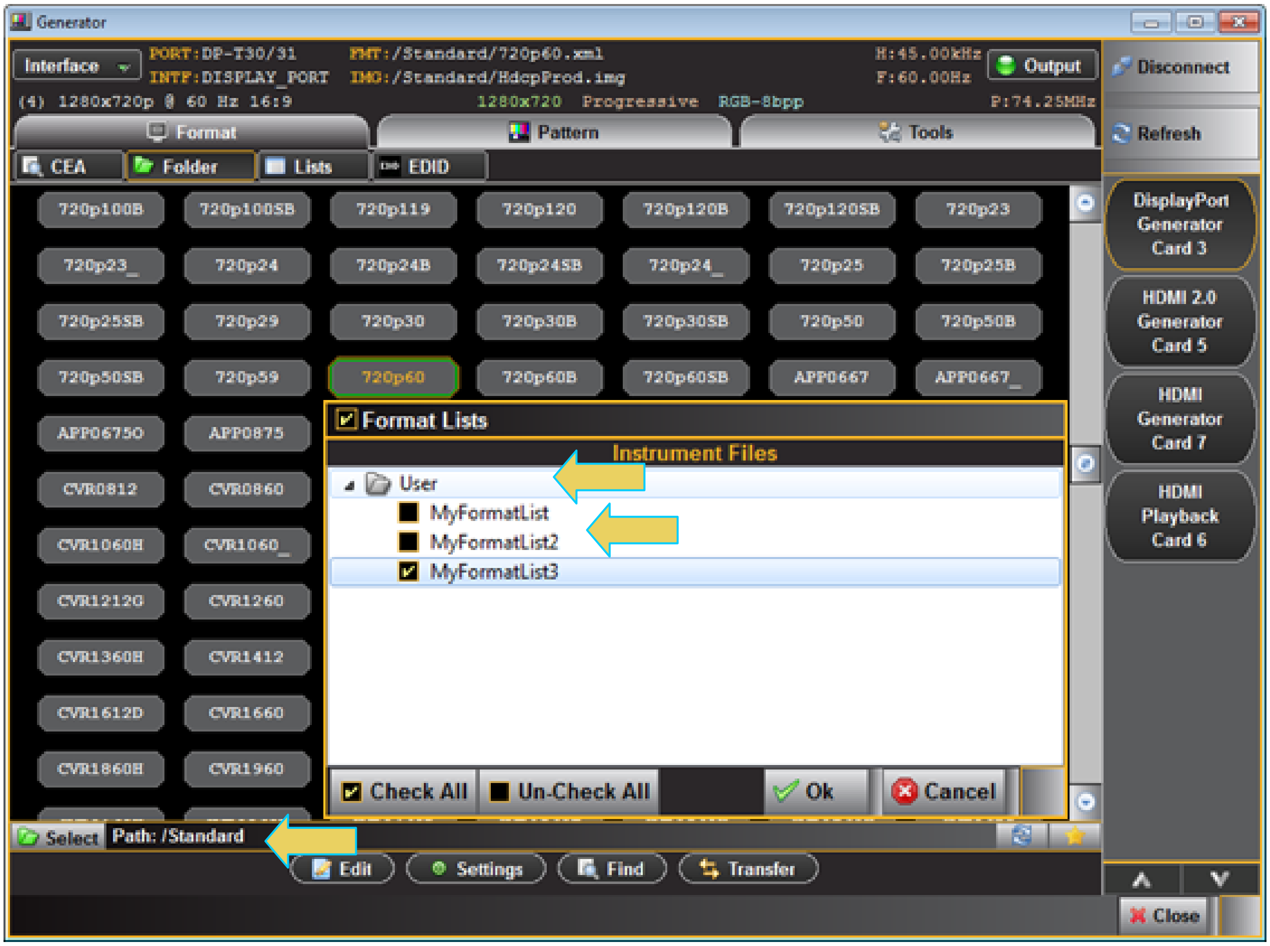
You can determine if the list of formats displayed is derived from the EDID of the connected display by looking at lower status area of the panel Read EDID and Generate Formats.

When EDID formats are not active, the directory whose formats are being displayed is listed in the lower panel Select Path: /Standard. Typically this would be the Standard directory where the 980 module's format list is stored. The default path is the Standard path.

You might wish to change the directory path if you have created your own custom formats using the Format Editor to create custom formats. Note also that you can configure a smaller list of formats to choose from using the **Format List Edit**; refer to Format List Editor. By default when you create a custom format, the new format will be saved in the User path. You can change the directory by clicking on the Select activation button Select on the bottom of the panel which opens up a in the dialog box below.



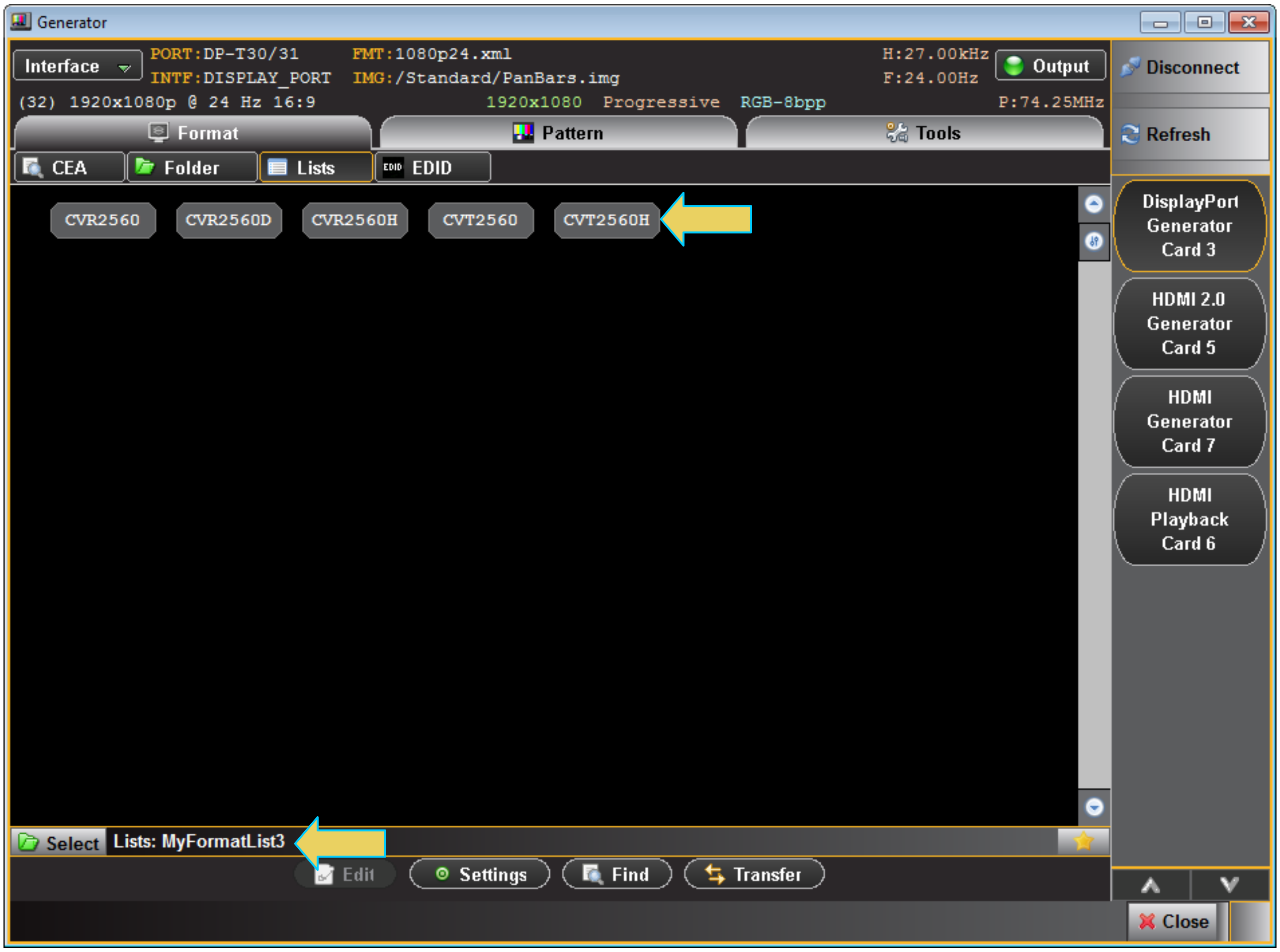
You can open up and activate any custom Format Lists you have previously defined with the associated icon Select. A dialog box will appear enabling you to select a custom format list or lists (below).



PORT:DP-T30/31
INTF:DISPLAY_PORT
FMT:/Standard/720p60.xml
IMG:/Standard/HdcpProd.img
H:45.00kHz
F:60.00Hz
(4) 1280x720p @ 60 Hz 16:9
1280x720 Progressive RGB-8bpp
P:74.25MHz

Path: /Standard

You can select all or one custom Format List any combination if you have several defined. The example above shows selecting one Format List. The Check All and Un-Check All activation buttons allow convenient selection where you have many Format Lists to choose from. The result of selecting one custom Format List is shown in the screen example below. A limited set of formats are displayed. The Path icon on the bottom status panel will display that new list (indicated below).



PORT:DP-T30/31
INTF:DISPLAY_PORT
FMT:1080p24.xml
IMG:/Standard/PanBars.img
H:27.00kHz
F:24.00Hz
(32) 1920x1080p @ 24 Hz 16:9
1920x1080 Progressive RGB-8bpp
P:74.25MHz
Lists: MyFormatList3

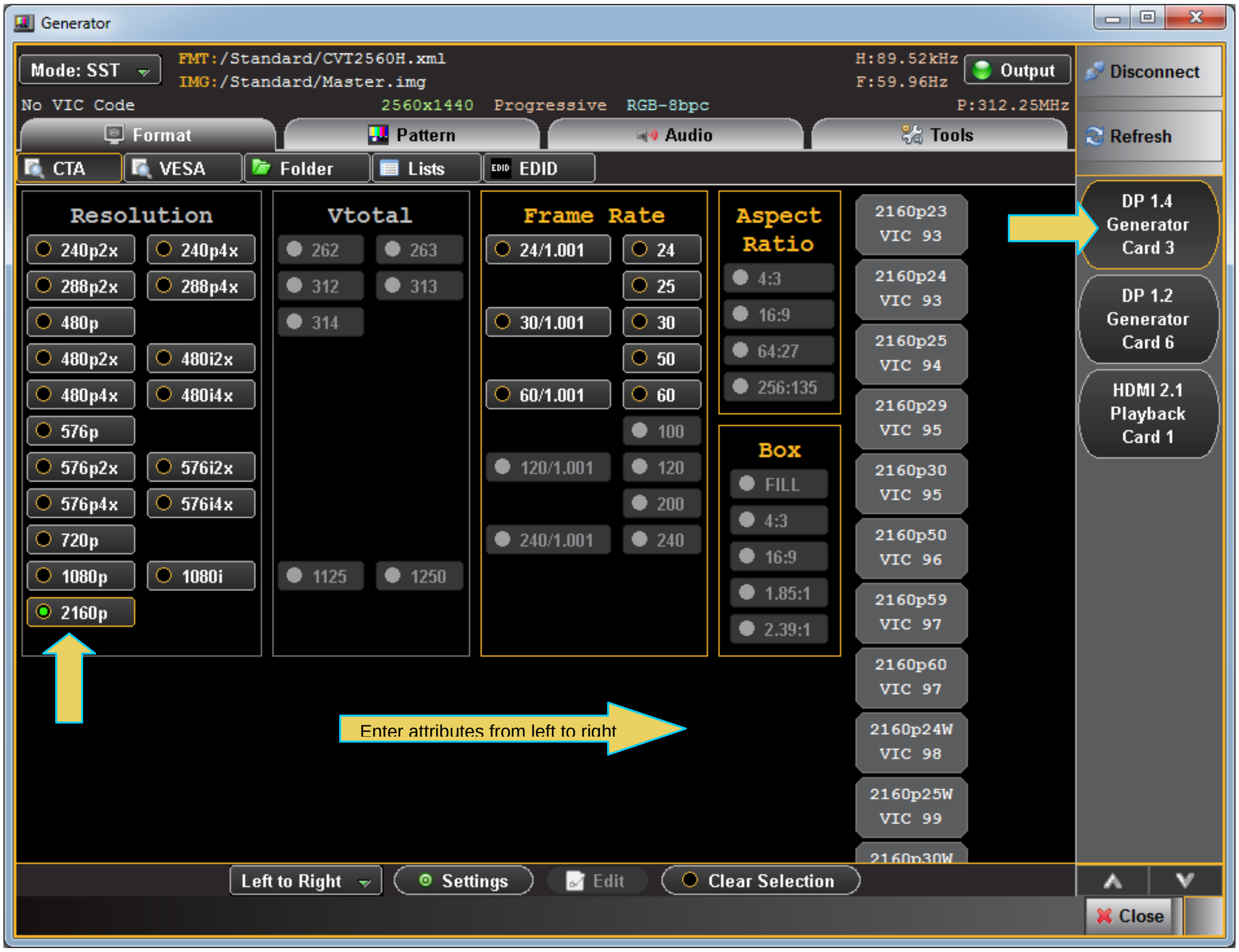
3.6.2 Selecting formats using the CEA smart filtering button

Use the following procedures to select a video resolution (format) using the CEA smart filtering button. The procedure assumes that you have already selected the DP interface.

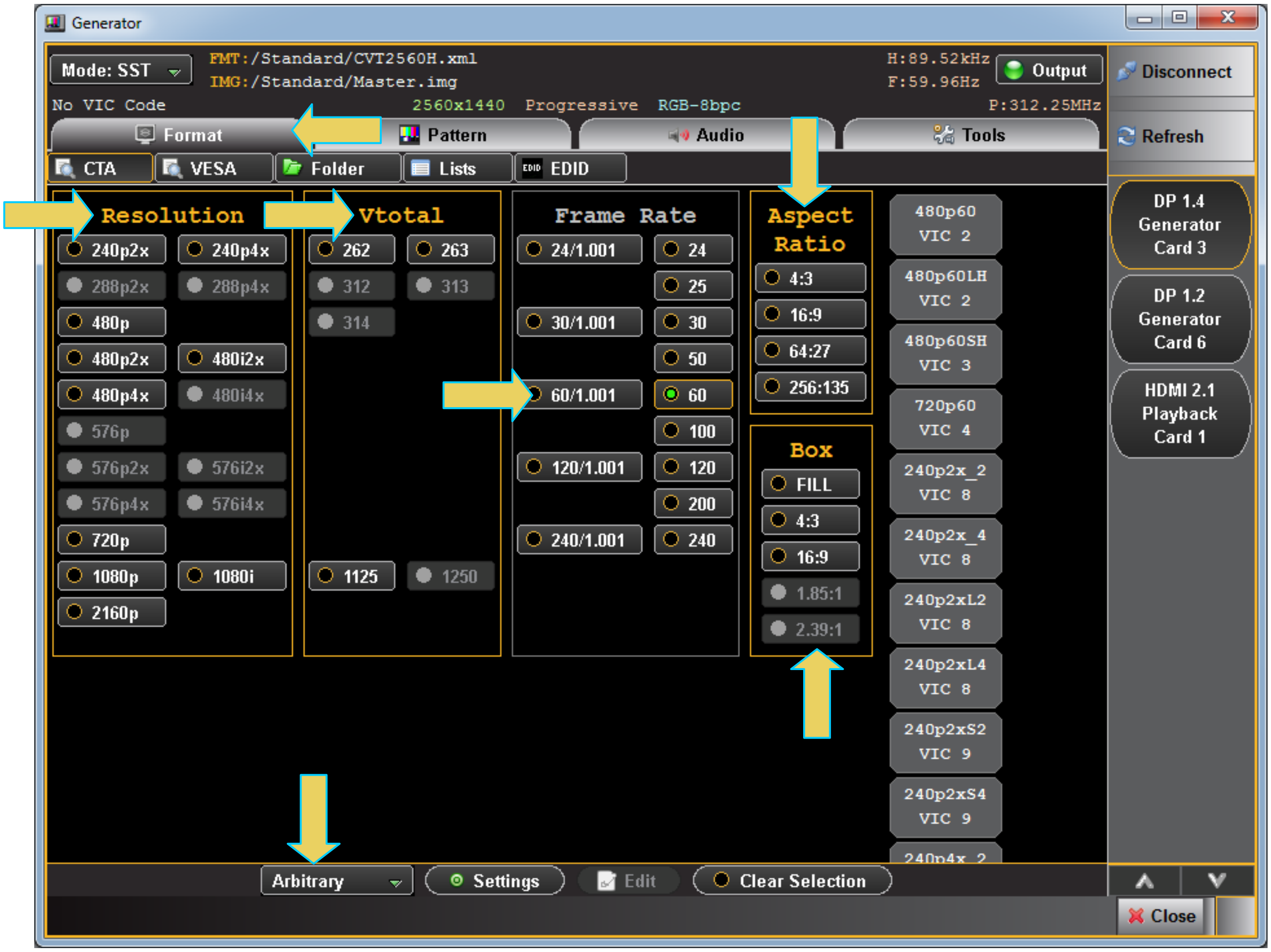
To select a format from the CEA smart filtering button:

1. From the main window of the 980 DP Video Generator / Analyzer module, click the **Format** tab.

   If the CEA button is not active, simply click on the **CEA** button on the upper left of the top panel (indicted in the screen shot below). The CEA smart filtering screen enables you to select CEA formats through filtering of various vide parameters such as Resolution, Vtotal, Frame Rate and Aspect Ratio. As you optionally move from left to right on the screen the list of available formats that meet the filtering criteria is shown on the right.



Alternatively you can select Arbitrary on the pull-down list on the lower control panel. The Arbitrary selection enables you to specify filtering criteria in any order. Refer to the example below.



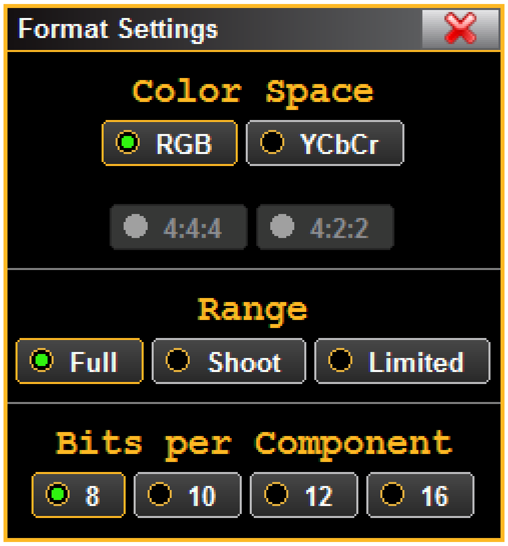
3.7 Configuring the format Settings

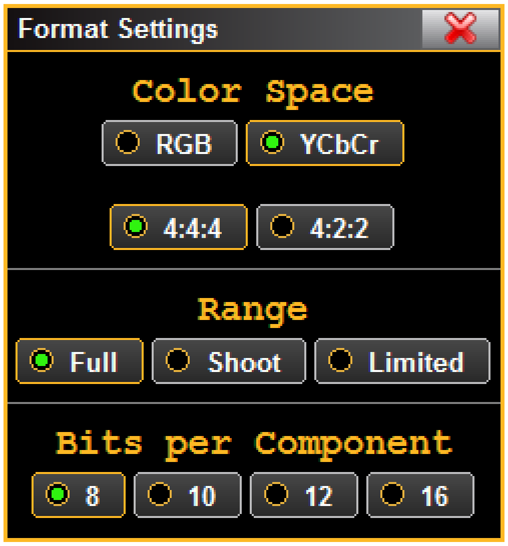
Use the following procedures to configure the format settings. The Settings dialog box enables you to configure the Color Space, Range and Bits per Component.

To select a format:

1. Specify the format settings by clicking on the **Settings** button on the lower center of the panel (indicated below).

The **Settings** dialog box appears as shown below. Two examples are shown below; the first with RGB selected and the second with YCbCr selected.





2. Select the Color Space, Range and Bits per Component from the **Format Settings** dialog box in accordance with your requirements.

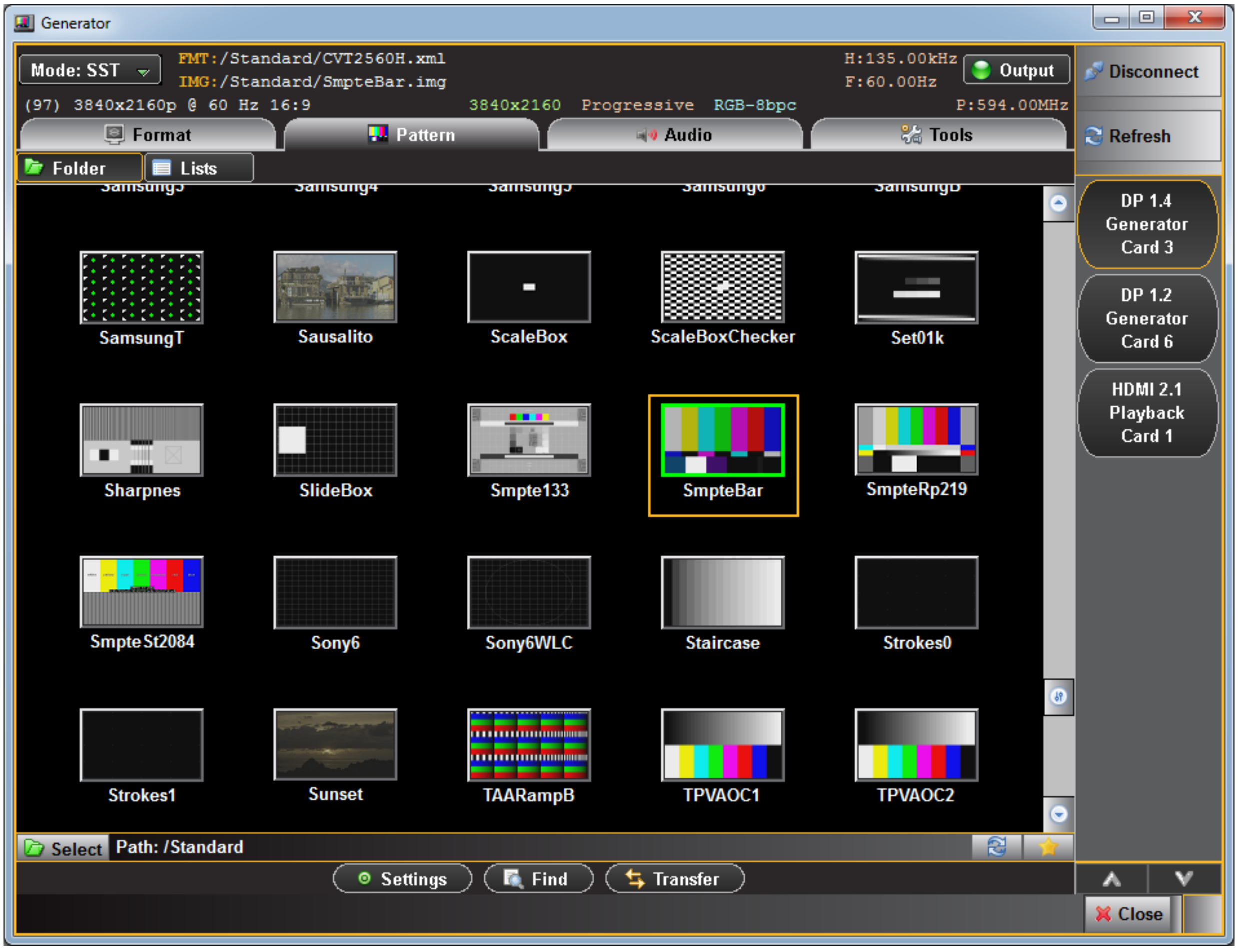
Format Settings		
Parameter	**Description**	**Options**
Color Space	Colorimetry and video pixel encoding settings.	• RGB – Uses 4:4:4 sampling. • YCbCr – Uses either 4:4:4, 4:2:2 sampling.
Range	These values are described in CEA-861E. They pertain to the number of levels for RGB and YCbCr mode.	• Limited – Use for CEA formats. Please refer to the specification section on Video Quantization Ranges for more details. • Shoot – for testing the undershoot/overshoot signal code margins. • Full - Use for PC formats. Please refer to the specification section on Video Quantization Ranges for more details.
Bits per Component	Color depth per component.	• 8 – Eight (8) bit per component (24 bit per pixel) color depth. • 10 – Ten (10) bit per component (30 bit per pixel) color depth; deep color. • 12 – Twelve (12) bit per component (36 bit per pixel) color depth; deep color. • 16 – Sixteen (16) bit per component (48 bit per pixel) color depth; deep color.

3.8 Selecting Test Patterns

Use the following procedures to select a test pattern.

To select a test pattern:

1. From the main window of the 980 DP Video Generator / Analyzer module, click the **Pattern** tab to access the list of test patterns.

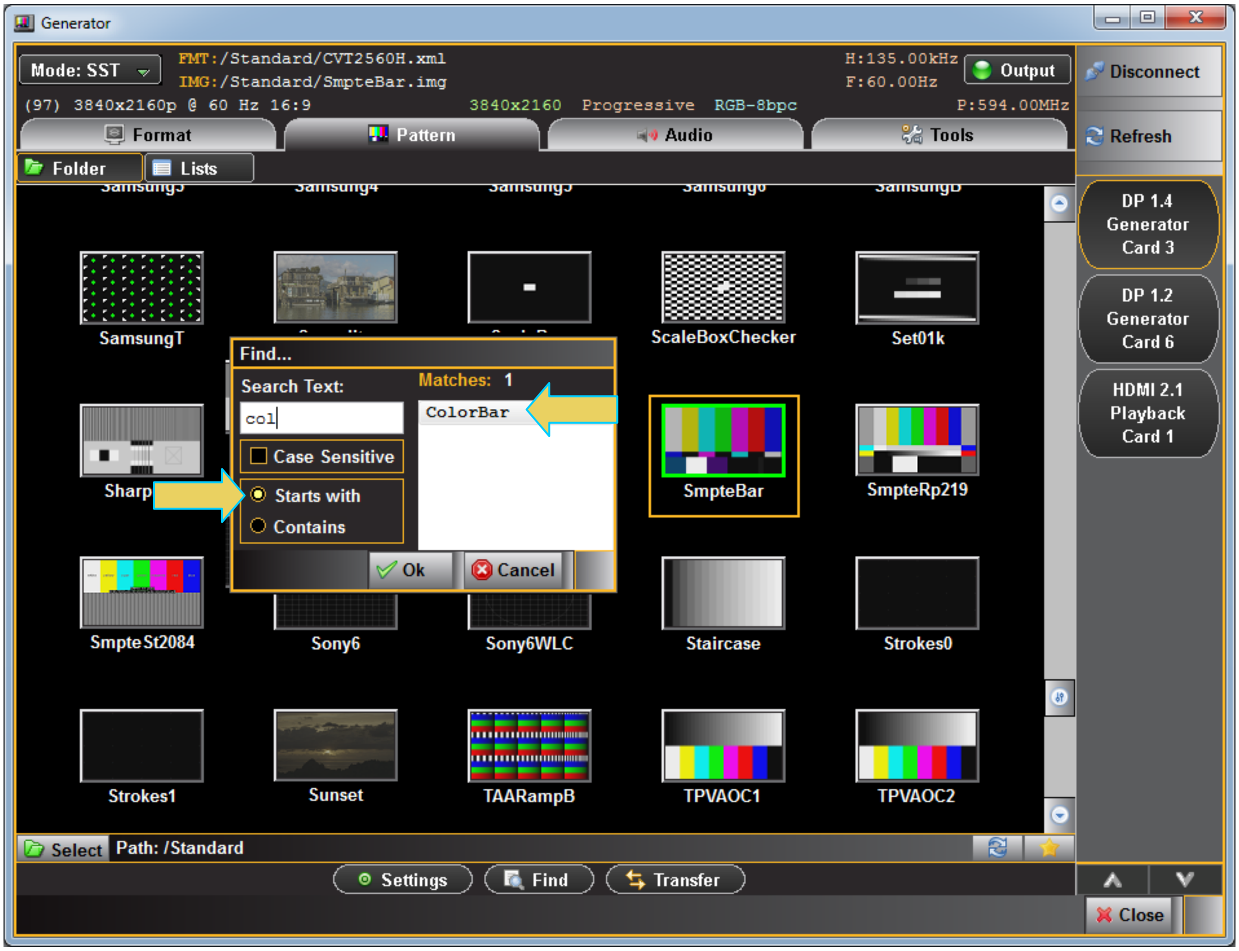


```
Mode: SST    FMT:/Standard/CVT2560H.xml                 H:135.00kHz
             IMG:/Standard/SmpteBar.img                 F:60.00Hz
(97) 3840x2160p @ 60 Hz 16:9   3840x2160  Progressive  RGB-8bpc   P:594.00MHz
```

Path: /Standard

2. Select a test pattern from the list by clicking or selecting it. There is a scroll bar on the right to allow access to the entire list by browsing.

   You can either scroll through the list of test patterns or use the **Find** feature to search for patterns. When you press the **Find** activation button, you are presented with a dialog window where you can search for a pattern by name using initial and mid string partial searches (below).



Mode: SST

FMT:/Standard/CVT2560H.xml

IMG:/Standard/SmpteBar.img

(97) 3840x2160p @ 60 Hz 16:9

3840x2160 Progressive RGB-8bpc

H:135.00kHz

F:60.00Hz

P:594.00MHz

Find...

Search Text: col

Matches: 1

ColorBar

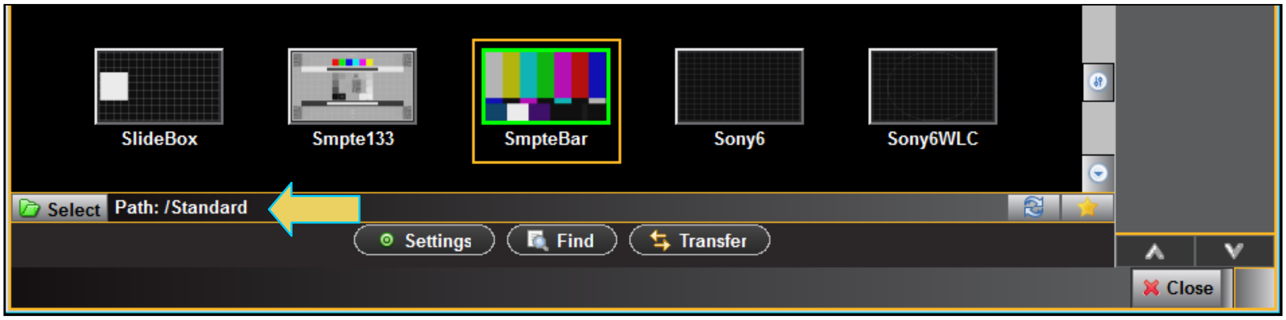
☐ Case Sensitive

● Starts with

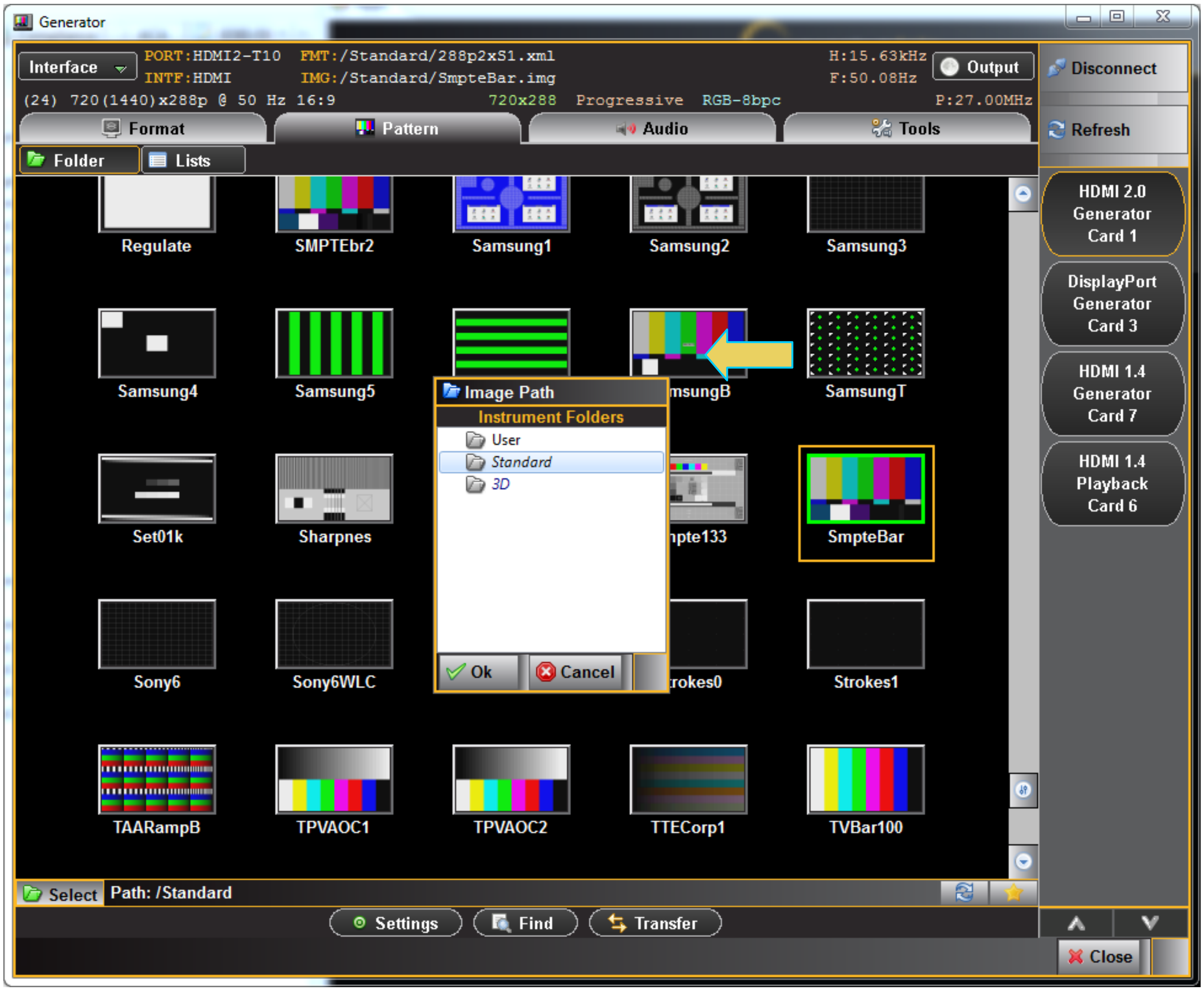
○ Contains

The directory whose images (patterns) are being displayed is listed in the lower panel as indicated below. In the example below, the path is set to Standard which will display the entire test pattern library and is the default path.

You might wish to change the directory path if you have added your own bitmap patterns and wanted to select them without scrolling through the complete list. You may also have created a custom Pattern List using the **Pattern List Editor**. Refer to Pattern List Editor for details on creating a custom Pattern List.



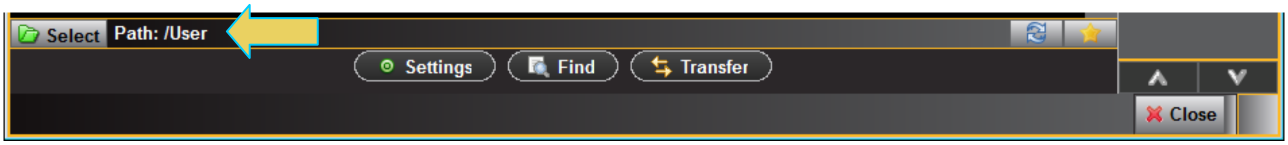
You can change the directory path with the directory icon Select. When you select the directory icon a dialog box will appear allowing you to select the alternative path such as the User path shown in the dialog box below.



```
PORT:HDMI2-T10   FMT:/Standard/288p2xS1.xml                H:15.63kHz
INTF:HDMI        IMG:/Standard/SmpteBar.img                F:50.08Hz
(24) 720(1440)x288p @ 50 Hz 16:9      720x288  Progressive  RGB-8bpc      P:27.00MHz
```

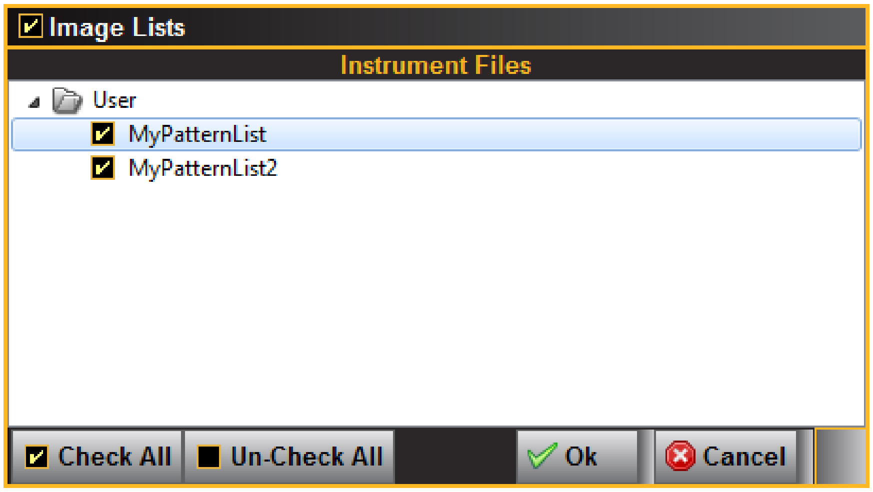
Path: /Standard

When you have changed the directory the User directory will be indicated on the lower panel beside the associated icon as shown below.

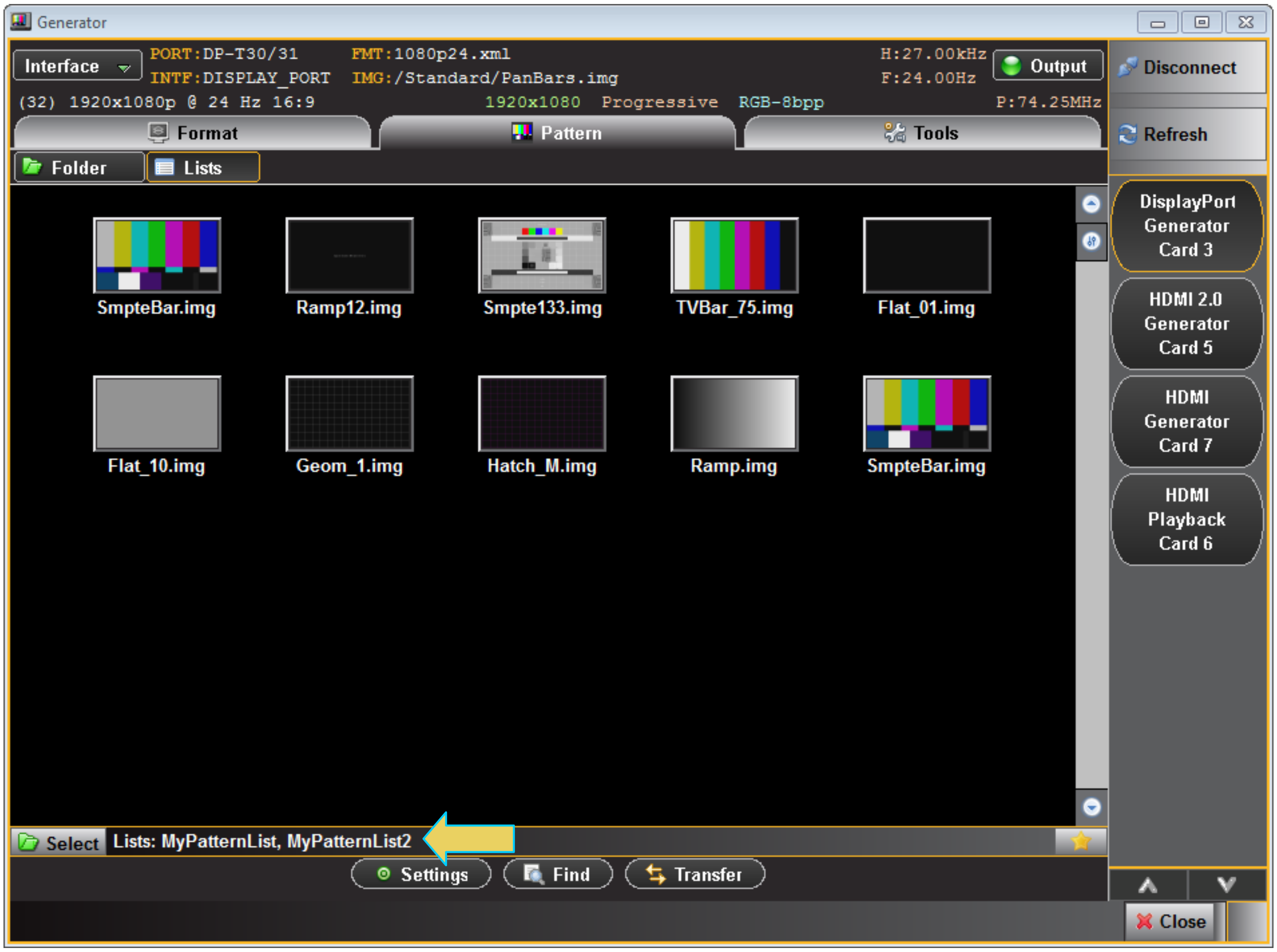


Path: /User

Now you can configure the list of patterns in accordance with a custom Pattern List by clicking on the associated icon **Select**. A dialog box will appear enabling you to select a custom image list (below).



You can select all or one custom Pattern List any combination if you have several defined. The example above shows selecting one Pattern List. The **Check All** and **Un-Check All** activation buttons allow convenient selection where you have many Pattern Lists to choose from. The result of selecting one custom Pattern List is shown in the screen example below. A limited set of patterns are displayed. The **Path** icon on the bottom status panel will display that new list (indicated below).



PORT:DP-T30/31 FMT:1080p24.xml H:27.00kHz
INTF:DISPLAY_PORT IMG:/Standard/PanBars.img F:24.00Hz
(32) 1920x1080p @ 24 Hz 16:9 1920x1080 Progressive RGB-8bpp P:74.25MHz

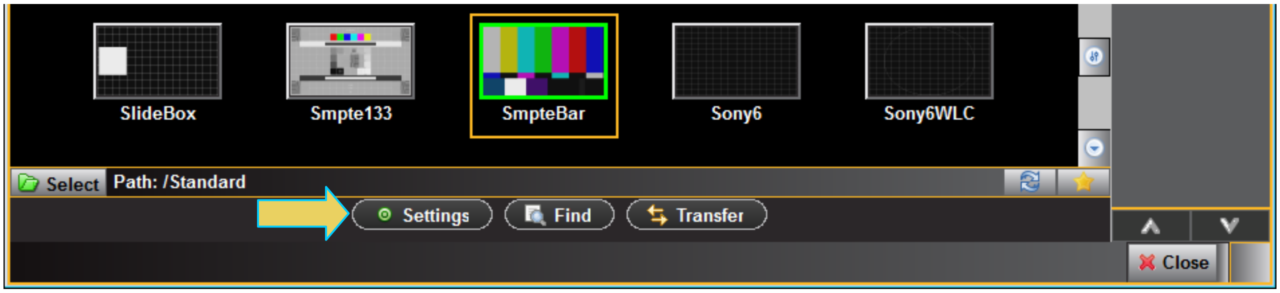
Lists: MyPatternList, MyPatternList2

3.9 Selecting Test Patterns Settings

Use the following procedures to select a test pattern.

To specify test pattern settings:

1. From the main window of the 980 DP Video Generator / Analyzer module, click the **Pattern** tab to access the list of test patterns.
2. Specify the image settings by clicking on the **Settings** button on the lower center of the panel.



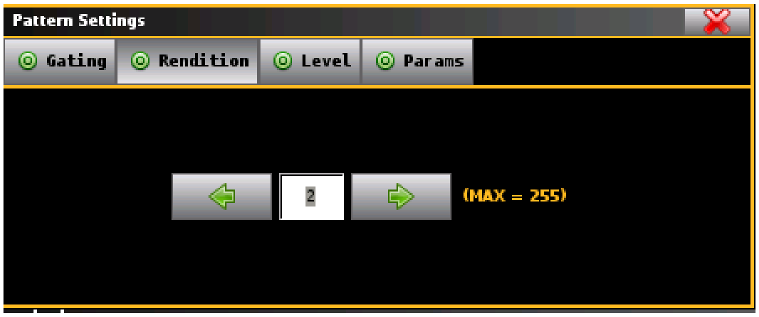
The **Settings** dialog box appears as shown below:

3. Enable and disable Gamma and Pseudo-random noise and set the gating as desired. Refer to the table below for details on these optional settings.

Pattern Settings - Gating	Description	Options
Gamma Correction	Enables or disables gamma correction which compensate for properties of human vision, to maximize the use of the bits or bandwidth relative to how humans perceive light and color.	• On • Off
Pseudo-Random Noise	Renders a test pattern with high level of volatility between adjacent pixels.	• On • Off
Component Gating	Turns on or off the three primary color components.	• Red • Green • Blue

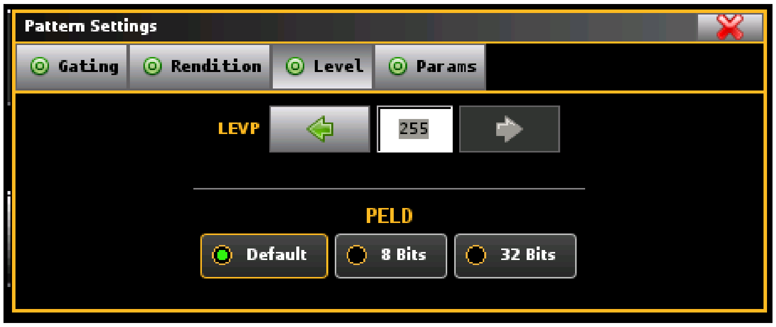
4. Select the rendition where applicable using the Rendition button. The associated dialog box is shown further below.

Some test patterns have multiple versions such as GraysAll. These multiple versions can be applied using the Rendition button and associated dialog box as shown below. There is a default that is iteration 0. In the example below iteration 2 is currently being rendered on the sink DUT.



5. Set the luminance level of the image with the Level button. The associated dialog box is shown further below.

   You can increment the color component values or can decrement the color component values for all pixels of any image through the front panel or the command line. This feature enables you to increment or decrement the values in increments (or decrements) of 1 throughout a range of 0 to 255. The LEVP feature increments or decrements all color component values (R,G,B) for each action by the use.



6. Set the pixel depth (PELD) if necessary through the Level button and associated dialog box shown above.

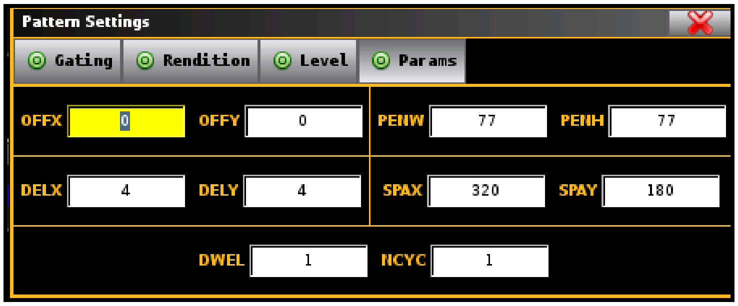
   PELD establishes the number of data bits that represent each active pixel in video memory (frame buffer). Parameter. The default setting and setting of 8 allows 256 colors on an image (test pattern) to be rendered. This is suitable for the majority of test patterns. However, some test patterns contain more colors and either require PELD 32 or look optimal only when PELD is set to 32. The test pattern will indicate when PELD 32 setting is required.

   - Default - uses the 980 video generator default
   - 8 - 8 bits-per-pixel (256 colors)
   - 24 - 24 bits-per-pixel (16,777,216 colors).

7. Set the pattern parameters if necessary through the **Params** button and associated dialog box shown below. The following table describes each parameter.

Pattern Settings - Parameters	Description
OFFX	Set horizontal offset for large patch of Regulate image
OFFY	Set vertical offset for large patch of Regulate image

Pattern Settings - Parameters	Description
DELX	Set horizontal shift for each step of SlideG/SlideRGB image
DELY	Set vertical shift for each step of SlideG/SlideRGB image
DWEL	Set number of frames for each step of SlideG/SlideRGB image
PENW	Set width variable for line thickness in EeRise, NAWC, and Slider images
PENH	Set height variable for line thickness in EeRise, NAWC, and Slider images
SPAX	Set horizontal spacing
SPAY	Set vertical spacing
NCYC	Internal use



OFFX 0
OFFY 0
PENW 77
PENH 77
DELX 4
DELY 4
SPAX 320
SPAY 180
DWEL 1
NCYC 1

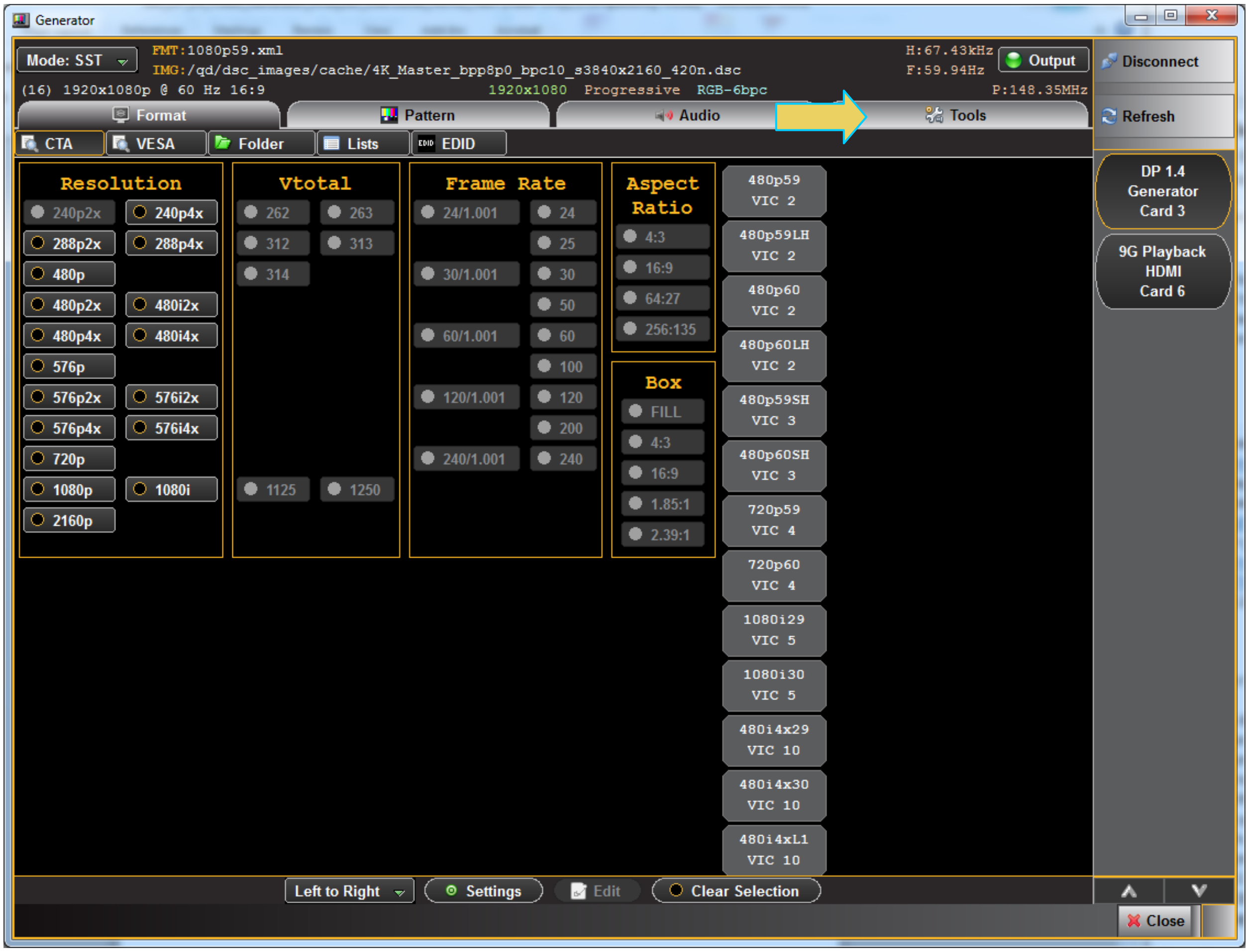
3.10 Testing Display Stream Compression (DSC) Displays

The 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module supports a DSC/FEC video generator function. You can output DSC/FEC streams with a user selectable slice configuration, various compression settings, bit depths, colorimetry etc. You can import your own configuration parameters from a Picture Parameter Set of values. You can select from a set of provided DSC images or import your own DPX images.

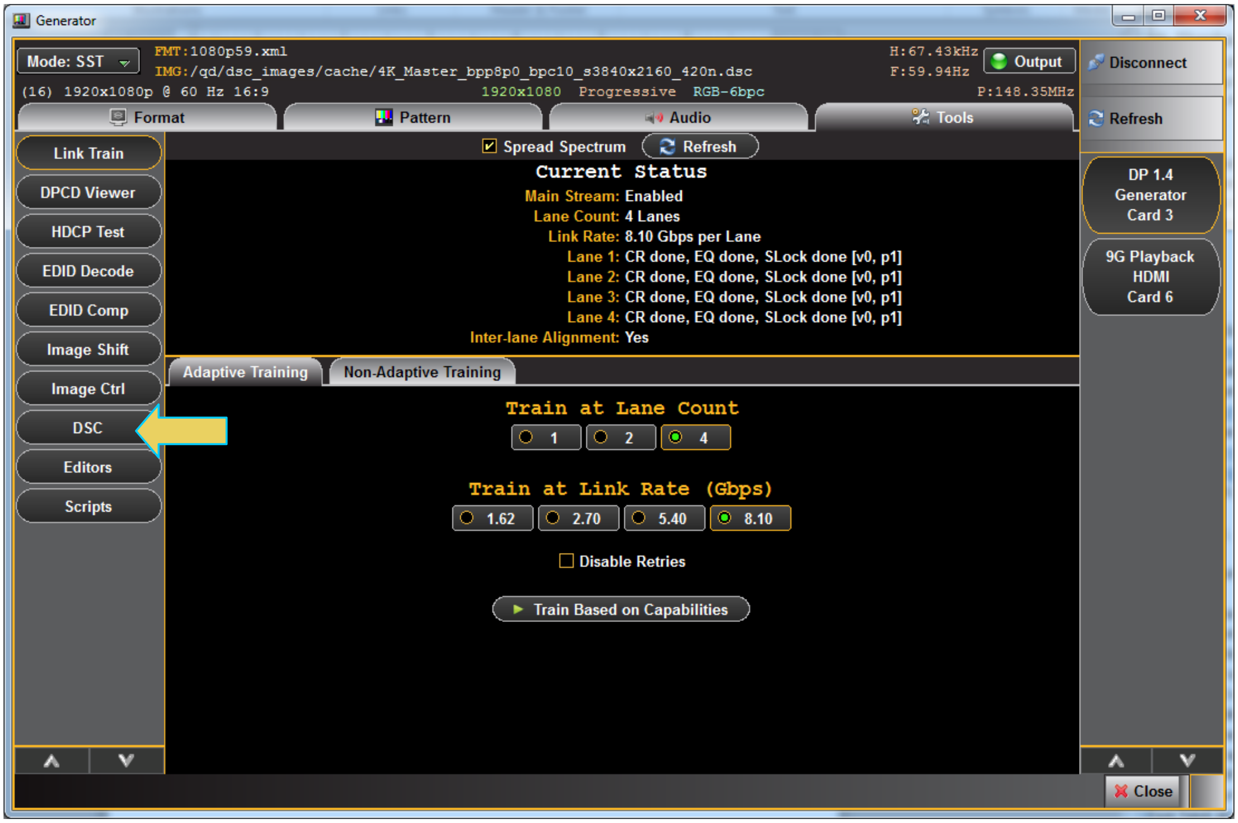
Display Stream Compression display testing is supported through the standard DP Tx port or the USB-C DP alt mode port.

To test a DSC/FEC-capable display device:

1. From the main window of the 980 DP Video Generator module, select the **Tools** tab.



Select the DSC tool as shown below.



```
FMT:1080p59.xml
IMG:/qd/dsc_images/cache/4K_Master_bpp8p0_bpc10_s3840x2160_420n.dsc
(16) 1920x1080p @ 60 Hz 16:9          1920x1080  Progressive  RGB-6bpc
H:67.43kHz
F:59.94Hz
P:148.35MHz
```

Current Status

Main Stream: Enabled
Lane Count: 4 Lanes
Link Rate: 8.10 Gbps per Lane
Lane 1: CR done, EQ done, SLock done [v0, p1]
Lane 2: CR done, EQ done, SLock done [v0, p1]
Lane 3: CR done, EQ done, SLock done [v0, p1]
Lane 4: CR done, EQ done, SLock done [v0, p1]
Inter-lane Alignment: Yes

Train at Lane Count: ○ 1 ○ 2 ● 4

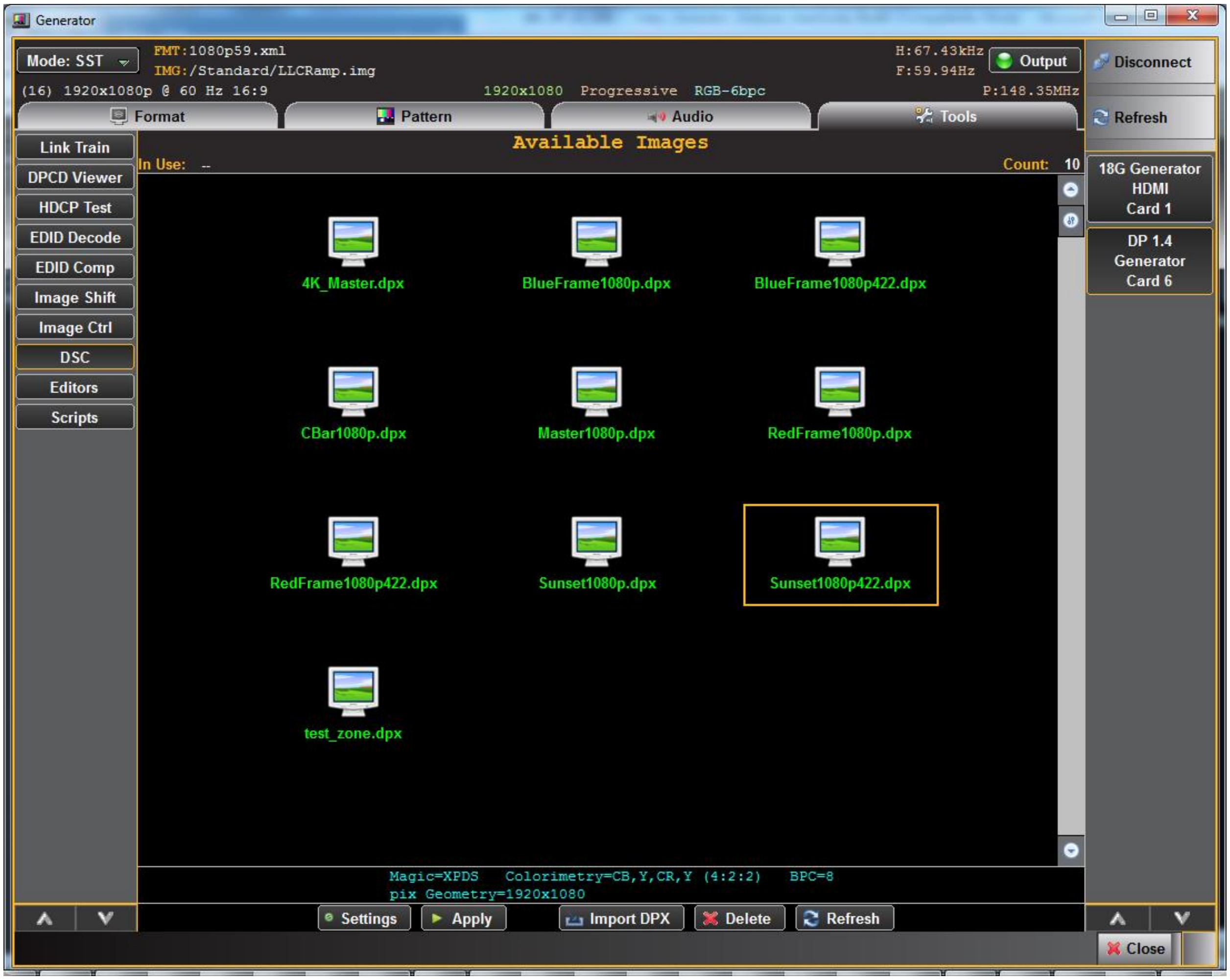
Train at Link Rate (Gbps): ○ 1.62 ○ 2.70 ○ 5.40 ● 8.10

☐ Disable Retries

☑ Spread Spectrum

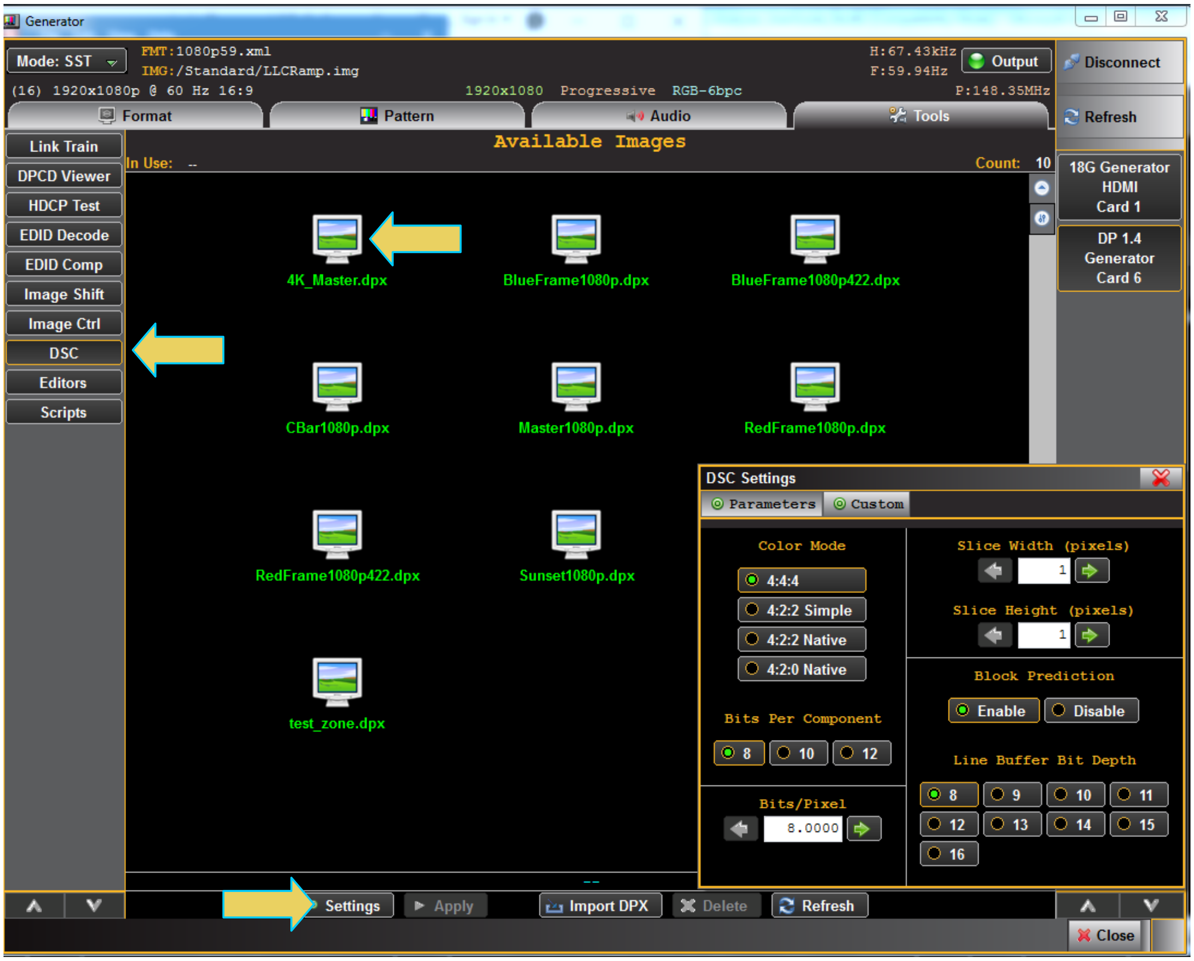
The DSC tools panel appears as shown below.

Select a file simply by clicking on it. Notice the selected file is listed on the upper part of the panel. The file name click on is shown below. The lower information panel shows the parameters of the selected video frame file.

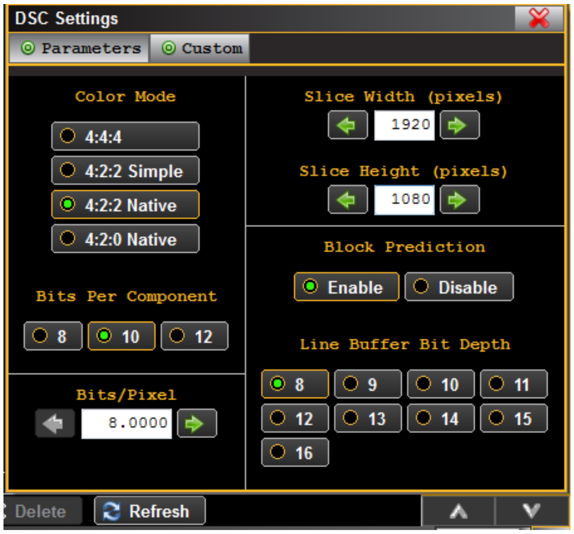


```
FMT:1080p59.xml                                              H:67.43kHz
IMG:/Standard/LLCRamp.img                                    F:59.94Hz
(16) 1920x1080p @ 60 Hz 16:9    1920x1080  Progressive  RGB-6bpc   P:148.35MHz
```

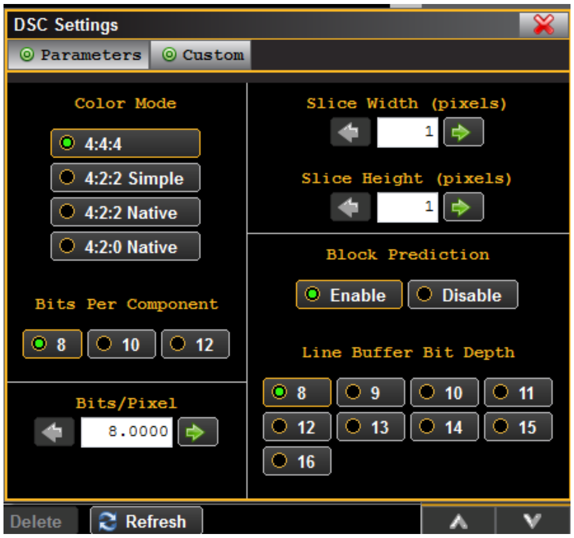
```
Magic=XPDS   Colorimetry=CB,Y,CR,Y (4:2:2)   BPC=8
pix Geometry=1920x1080
```



You can now select a DSC frame to output, import a custom DPX file, set the video parameters, compression, slice configuration and you can even import a custom set of PPS parameters from a text file. The Settings dialog box is shown below. The selections for the dialog box are described on the table that follows.



Another example is shown below:



Color Mode
● 4:4:4
○ 4:2:2 Simple
○ 4:2:2 Native
○ 4:2:0 Native

Bits Per Component
● 8 ○ 10 ○ 12

Bits/Pixel
8.0000

Slice Width (pixels)
1

Slice Height (pixels)
1

Block Prediction
● Enable ○ Disable

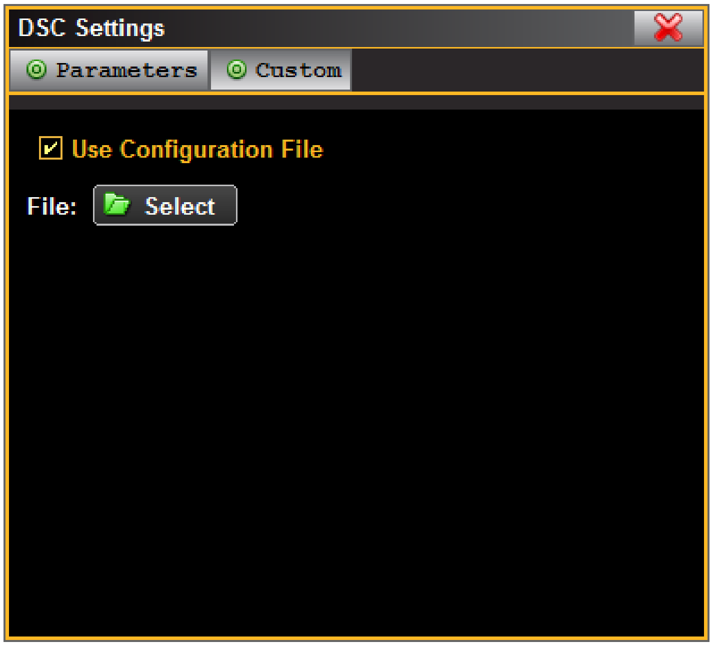
Line Buffer Bit Depth
● 8 ○ 9 ○ 10 ○ 11
○ 12 ○ 13 ○ 14 ○ 15
○ 16

The **Settings** dialog box parameters are described below:

DSC Video Generator Settings Dialog Box

Item	Parameters	Comments
Color Mode	Selections are: - 4:4:4 - 4:2:2 Simple - 4:2:2 Native - 4:2:0	
Bits Per Component	The color depth per component. Options are: - 8 - 10 -12	These selections would be 24, 30 or 36 respectively for color depth per pixel.
Bits/Pixel	This is the compression, i.e. the number of bits per pixels desired in the compressed output. Select throughout a range of 8 to 15.	The compression ratio can be calculated as Bits per Component x 3 / Bits per Pixel. Example: 8 bit color depth: 8 x 3 = 24 / 8 = 3:1 compression ratio.
Slice Width (pixels)	The Width in number of pixels across a slice.	All slices have to be the same size and they are all rectangular.
Slice Height (lines)	The Height in number of lines in a slice.	
Block Prediction	This selection indicates if the video generator will use Block Prediction.	Block prediction is an optional prediction method for the sink. You must be sure that the display you are testing supports Block Prediction.
Line Buffer Bit Depth	This is a Picture Parameter Set (PPS) parameter. It is the bitstream used to generate the bitstream. You can set this value or import this value as part of a Configuration File using the Custom tab.	You can import a text file to use.

To select a custom set of PPS parameters that you have stored on your host PC or on the 980 file system, click on the Custom button and hit the **Select** button.



Here is a sample of a Configuration File. Parameter name, space, value:

```
SRC_LIST /qd/dsc_images/cache/src_list.txt
FUNCTION 1
OUT_DIR /qd/dsc_images
DSC_VERSION_MINOR 32628
SLICE_WIDTH 3840
SLICE_HEIGHT 1080
INCLUDE   /qd/dsc_images/cfg/rc_8bpc_8bpp.cfg
DPX_FILE_OUTPUT 0
BLOCK_PRED_ENABLE 1
LINE_BUFFER_BPC 16
//  DPX read options (the following work well for most modes for GM/IM, some anomalies
are autodetected)
DPXR_PAD_ENDS     1   // Pad to 32-bit boundaries
DPXR_DATUM_ORDER  1
DPXR_FORCE_BE     0
SWAP_R_AND_B  1
//  DPX write options (the following work well for most modes for GM/IM)
DPXW_PAD_ENDS     1   // Required to output RGB to XNView 1.99 (but not YUV!)
DPXW_DATUM_ORDER   1
DPXW_FORCE_PACKING 1   // Method to use for 10 & 12-bit data
SWAP_R_AND_B_OUT   1
PPM_FILE_OUTPUT 0      // Output PPM files
```

3.11 Testing audio on an audio rendering device

The 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module supports audio testing for sink audio rendering devices. You can output LPCM audio over 8 channels at user selectable sampling rates, bits per sample. The audio signal is a sine wave. You can also specify the amplitude and the frequency of the sine wave. You can also specify the amplitude and frequency of each channel separately. Use the following procedures to test a DP audio rendering device.

Note: When testing MST-capable audio rendering devices, the audio signal that you specify will be transmitted to all downstream MST sinks.

To test an audio rendering device:

1. From the main window of the 980 DP Video Generator module, select the **Audio** tab.

The audio tab interface appears as shown below.

Mode: SST
FMT:/Standard/CVT2560H.xml
IMG:/Standard/Master.img
H:89.52kHz
F:59.96Hz
No VIC Code
2560x1440 Progressive RGB-8bpc
P:312.25MHz

Channels: 6.1
Sample Rate: 48 kHz
Bits/Sample: 24
☐ Mute Channel: 1
Level (dB): -48
Frequency (Hz): 1000

The table below summarizes the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer uncompressed LPCM programmable audio test tones.

LPCM Programmable Sine Wave options		
Parameter	**Description**	**Options**
Channels	This is the number of channels in the audio sine wave test tone.	• 2.1 • 2.1 • 5.1 • 6.1 • 7.1
Sampling Rate	This is the sampling rate of the audio sine wave test tone.	• 32kHz • 44.1kHz • 48kHz • 88.2kHz • 96kHz • 176.4kHz • 192kHz

LPCM Programmable Sine Wave options

Parameter	Description	Options
Bits per Sample	This is the number of bits per channel of the audio sine wave test tone.	• 16 • 20 • 24
Channel Selection	Indicates the channels that are active. Also indicates the channel that is configured for the Level, Mute and Frequency Parameters.	• FL – Front Left • FR – Front Right • LFE – Low Frequency Effects • FC – Front Center • RL – Rear Left • RR – Rear Right • RLC – Rear Left Center • RRC – Rear Right Center
Level (dB)	This is the amplitude of the audio sine wave test tone.	• Increments in 3dB throughout a range of – 0dB to -99dB (per channel).
Mute	Mutes or unmutes the audio for a particular channel.	• On • Off
Frequency (Hz)	The frequency of the audio sine wave test tone.	Programmable throughout a range of – -0.01kHz to 20kHz (per channel) in increments of: • 1Hz • 10Hz • 100Hz • 1kHz

3.12 Viewing the EDID of a connected display

Use the following procedures to select DP formats.

Note: When testing MST-capable sink devices, you can read the EDID of any specific downstream MST sink. This is addressed in Reading the EDID of a downstream MST node.

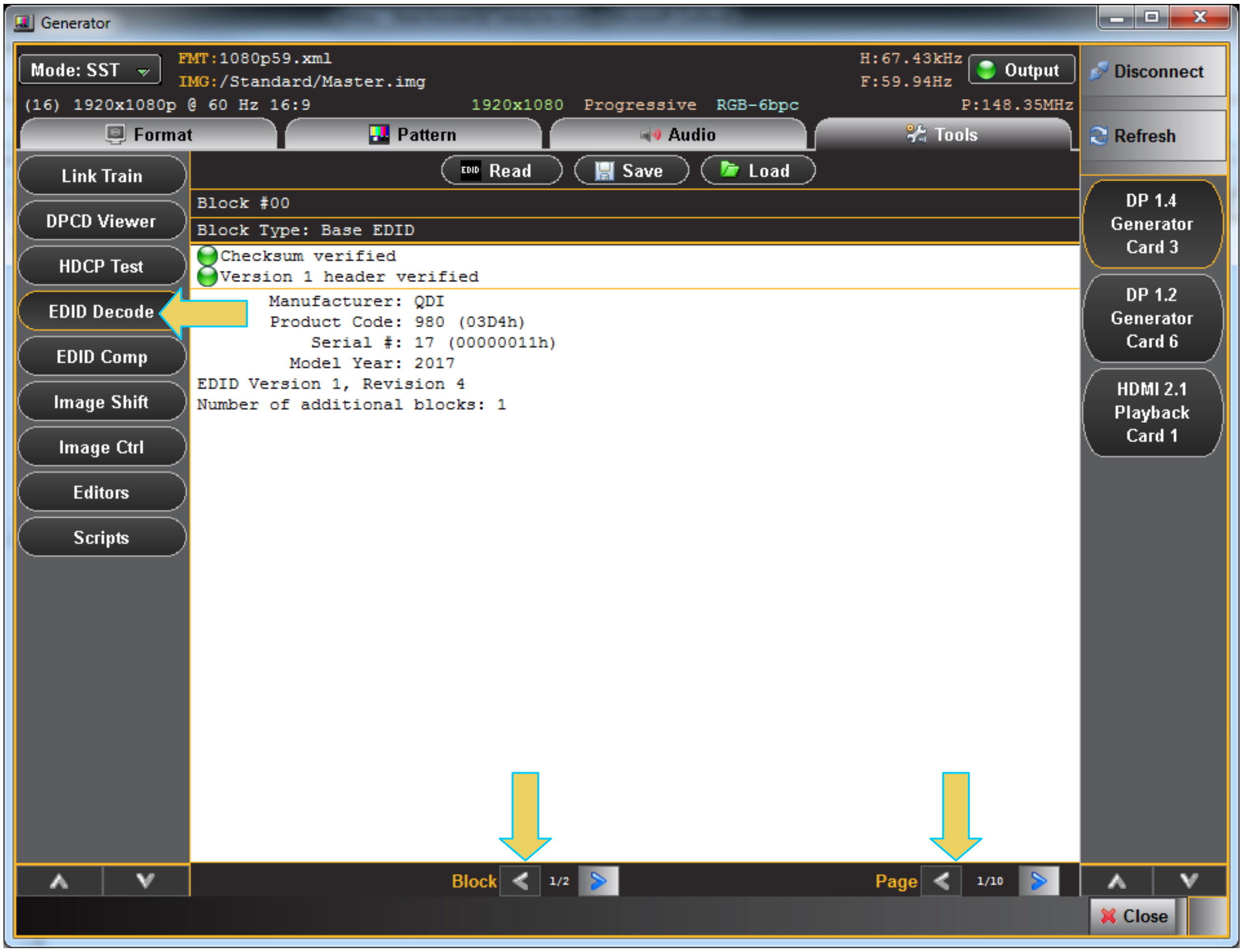
To view the EDID of a connected display:

1. From the main window of the 980 DP Video Generator / Analyzer module, select the **Tools** tab.

   Make sure the DP Generator Card is selected.

2. Activate the **EDID Decode** button on the upper left (indicated below).

   Contents of the initial data in the first block of the EDID will be displayed (below).

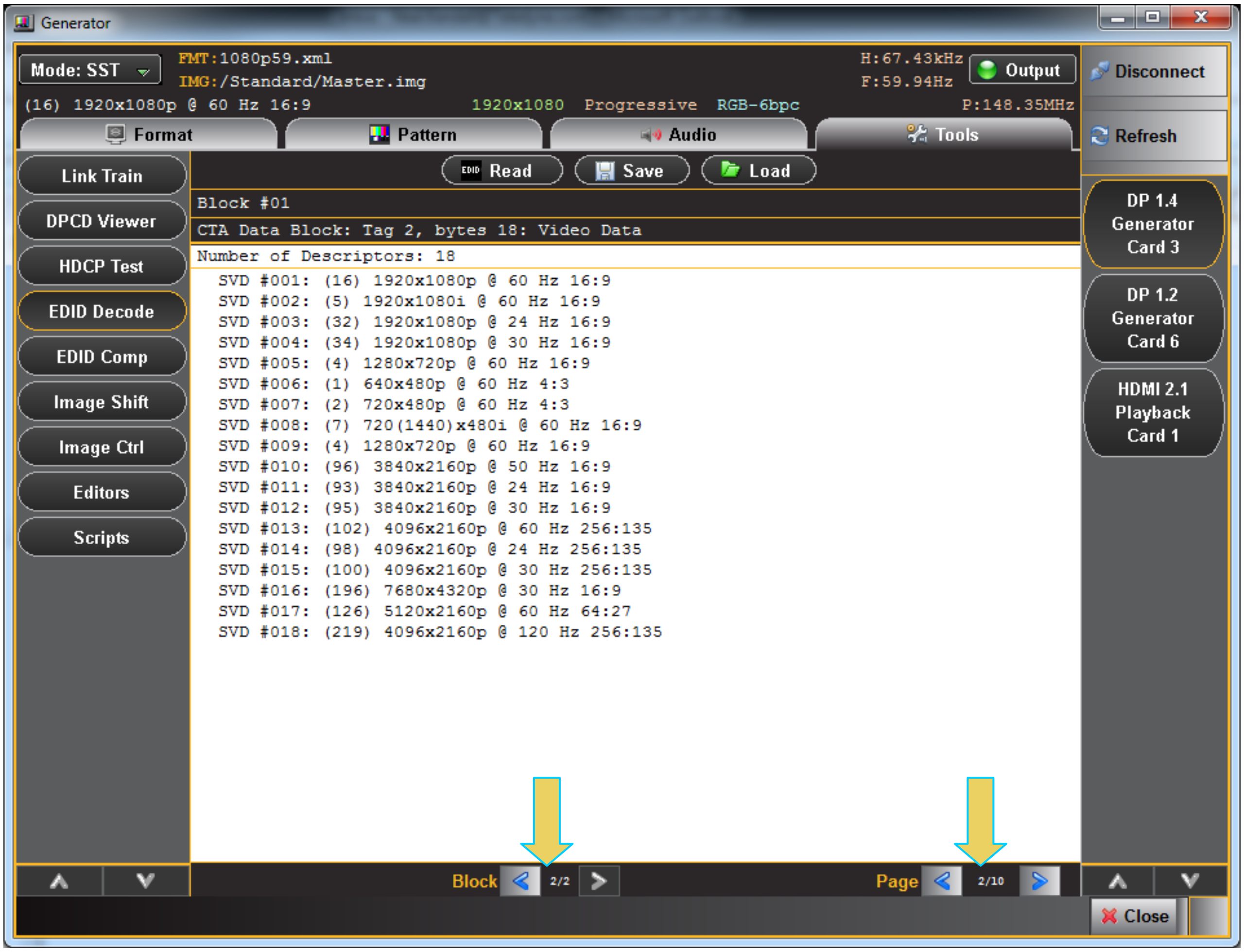


```
FMT:1080p59.xml                                              H:67.43kHz
IMG:/Standard/Master.img                                     F:59.94Hz
(16) 1920x1080p @ 60 Hz 16:9       1920x1080  Progressive  RGB-6bpc      P:148.35MHz
```

```
Block #00
Block Type: Base EDID
Checksum verified
Version 1 header verified
     Manufacturer: QDI
     Product Code: 980 (03D4h)
         Serial #: 17 (00000011h)
       Model Year: 2017
EDID Version 1, Revision 4
Number of additional blocks: 1
```

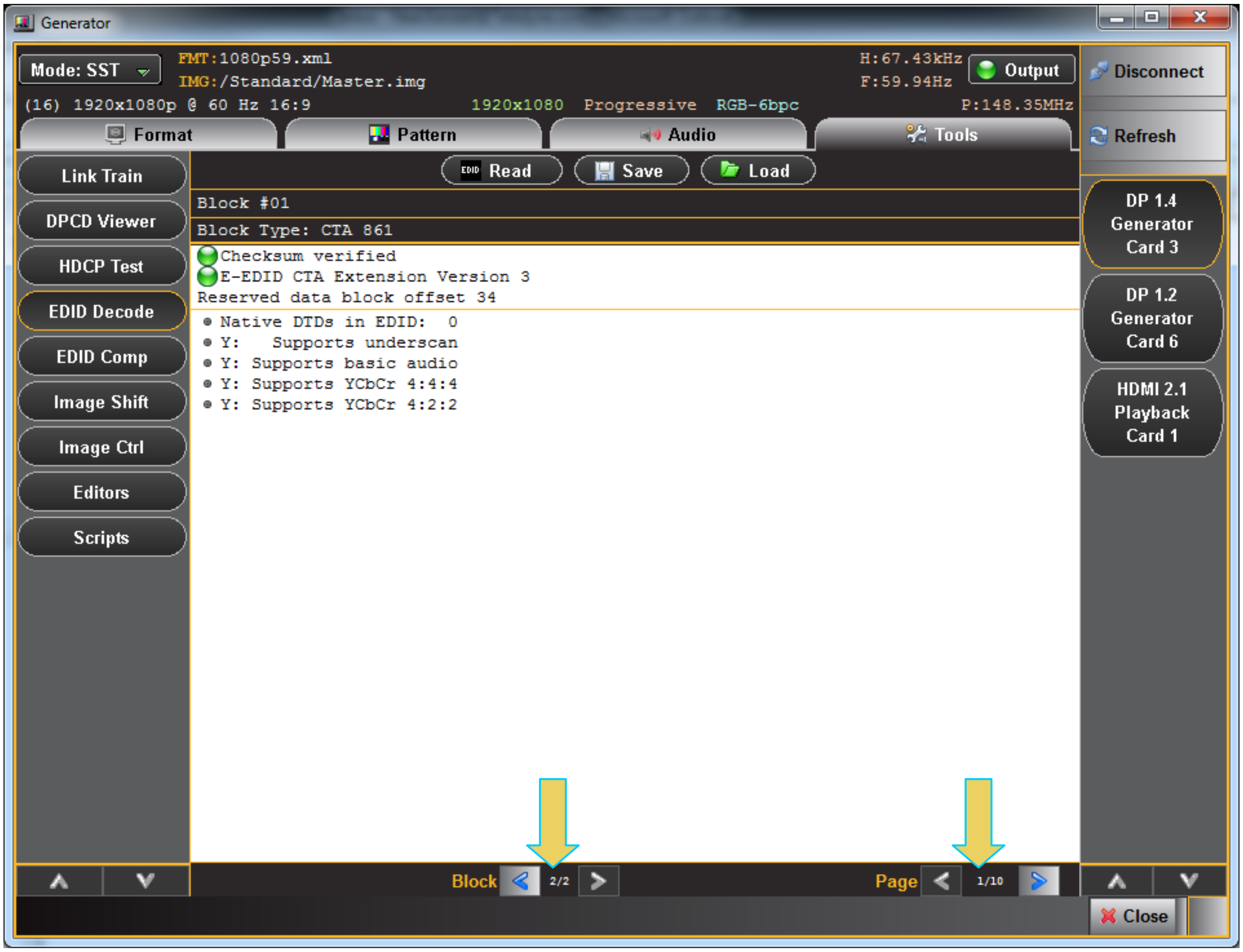
Navigate through the blocks and pages of the EDID using the arrow buttons on the lower panel (indicated above).

Examples of the **EDID Decode** content are shown in the following screens.



```
FMT:1080p59.xml                                              H:67.43kHz
IMG:/Standard/Master.img                                     F:59.94Hz
(16) 1920x1080p @ 60 Hz 16:9    1920x1080  Progressive  RGB-6bpc  P:148.35MHz
```

```
Block #01
CTA Data Block: Tag 2, bytes 18: Video Data
Number of Descriptors: 18
  SVD #001:  (16) 1920x1080p @ 60 Hz 16:9
  SVD #002:  (5) 1920x1080i @ 60 Hz 16:9
  SVD #003:  (32) 1920x1080p @ 24 Hz 16:9
  SVD #004:  (34) 1920x1080p @ 30 Hz 16:9
  SVD #005:  (4) 1280x720p @ 60 Hz 16:9
  SVD #006:  (1) 640x480p @ 60 Hz 4:3
  SVD #007:  (2) 720x480p @ 60 Hz 4:3
  SVD #008:  (7) 720(1440)x480i @ 60 Hz 16:9
  SVD #009:  (4) 1280x720p @ 60 Hz 16:9
  SVD #010:  (96) 3840x2160p @ 50 Hz 16:9
  SVD #011:  (93) 3840x2160p @ 24 Hz 16:9
  SVD #012:  (95) 3840x2160p @ 30 Hz 16:9
  SVD #013:  (102) 4096x2160p @ 60 Hz 256:135
  SVD #014:  (98) 4096x2160p @ 24 Hz 256:135
  SVD #015:  (100) 4096x2160p @ 30 Hz 256:135
  SVD #016:  (196) 7680x4320p @ 30 Hz 16:9
  SVD #017:  (126) 5120x2160p @ 60 Hz 64:27
  SVD #018:  (219) 4096x2160p @ 120 Hz 256:135
```



```
FMT:1080p59.xml                                            H:67.43kHz
IMG:/Standard/Master.img                                   F:59.94Hz
(16) 1920x1080p @ 60 Hz 16:9    1920x1080  Progressive  RGB-6bpc    P:148.35MHz
```

```
Block #01
Block Type: CTA 861
Checksum verified
E-EDID CTA Extension Version 3
Reserved data block offset 34
● Native DTDs in EDID:  0
● Y:   Supports underscan
● Y: Supports basic audio
● Y: Supports YCbCr 4:4:4
● Y: Supports YCbCr 4:2:2
```

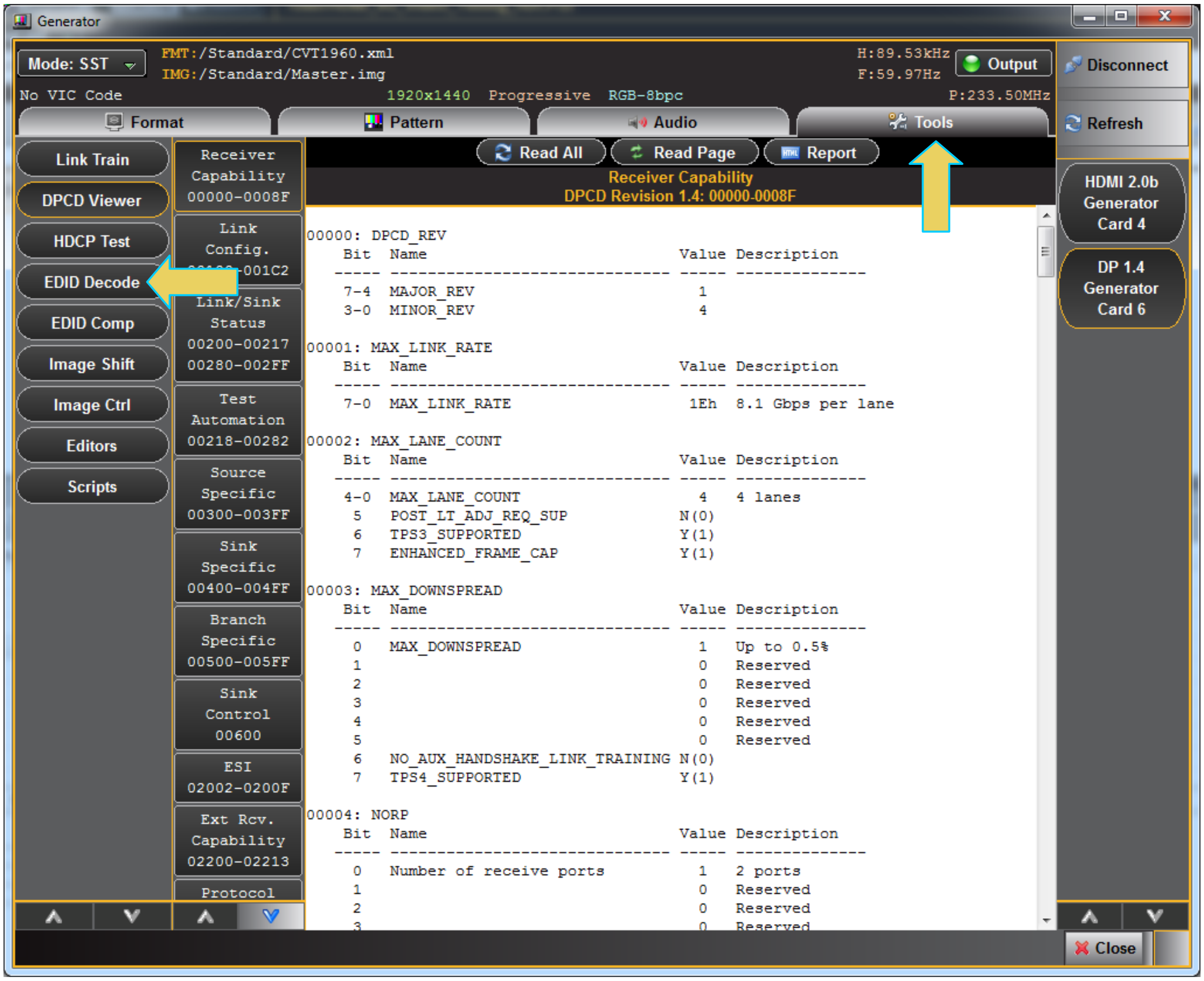
3.13 Viewing the DPCD of a connected display

Use the following procedures to view a displays DPCD registers.

Note: When testing MST-capable sink devices, you can read the EDID of any specific downstream MST sink. This is addressed in Reading the DPCD of a downstream MST node. You can also produce an HTML report of the DPCD registers.

To view the DPCD of a connected display:

1. From the main window of the 980 DP Video Generator / Analyzer module, select the **Tools** tab.



```
FMT:/Standard/CVT1960.xml                                    H:89.53kHz
IMG:/Standard/Master.img                                     F:59.97Hz
No VIC Code         1920x1440  Progressive  RGB-8bpc         P:233.50MHz
```

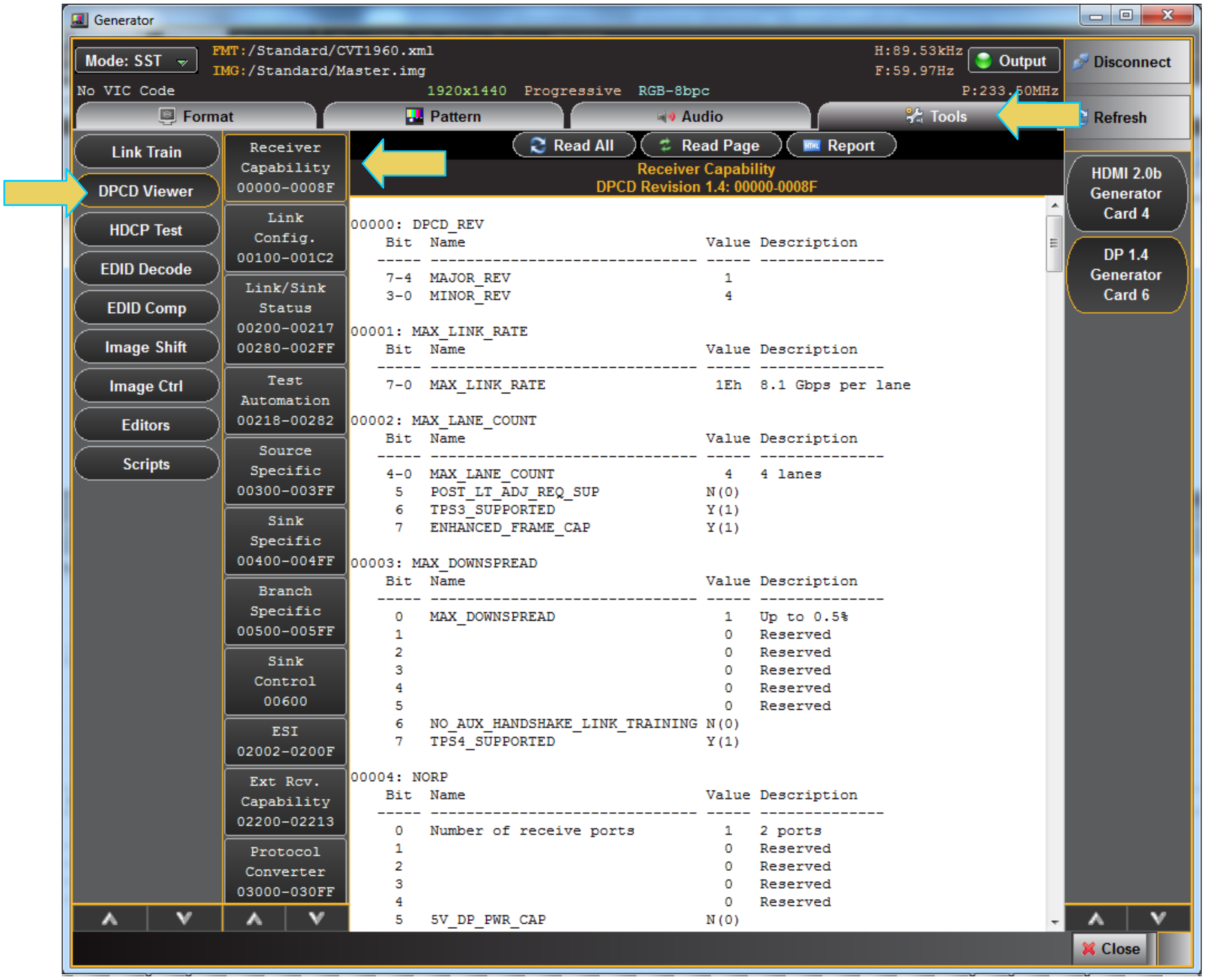
```
00000: DPCD_REV
    Bit   Name                           Value Description
   ----- ------------------------------ ----- -------------
    7-4   MAJOR_REV                        1
    3-0   MINOR_REV                        4

00001: MAX_LINK_RATE
    Bit   Name                           Value Description
   ----- ------------------------------ ----- -------------
    7-0   MAX_LINK_RATE                   1Eh  8.1 Gbps per lane

00002: MAX_LANE_COUNT
    Bit   Name                           Value Description
   ----- ------------------------------ ----- -------------
    4-0   MAX_LANE_COUNT                   4   4 lanes
     5    POST_LT_ADJ_REQ_SUP            N(0)
     6    TPS3_SUPPORTED                 Y(1)
     7    ENHANCED_FRAME_CAP             Y(1)

00003: MAX_DOWNSPREAD
    Bit   Name                           Value Description
   ----- ------------------------------ ----- -------------
     0    MAX_DOWNSPREAD                   1   Up to 0.5%
     1                                     0   Reserved
     2                                     0   Reserved
     3                                     0   Reserved
     4                                     0   Reserved
     5                                     0   Reserved
     6    NO_AUX_HANDSHAKE_LINK_TRAINING N(0)
     7    TPS4_SUPPORTED                 Y(1)

00004: NORP
    Bit   Name                           Value Description
   ----- ------------------------------ ----- -------------
     0    Number of receive ports          1   2 ports
     1                                     0   Reserved
     2                                     0   Reserved
     3                                     0   Reserved
```

Note: Make sure the DP Video Generator Card is selected.

2. Select the DP Tx port that is connected to the sink DUT from the pull-down menu provided (below). The naming convention used is:

3. **DP** is the interface selected, **T** indicates that it is a *Transmit* port (there will be a *Receiver* port on this module in the near future); **3** indicates the *Slot* number (starting at 1); 1 or 0 indicates the *Port* number (starting at 0).

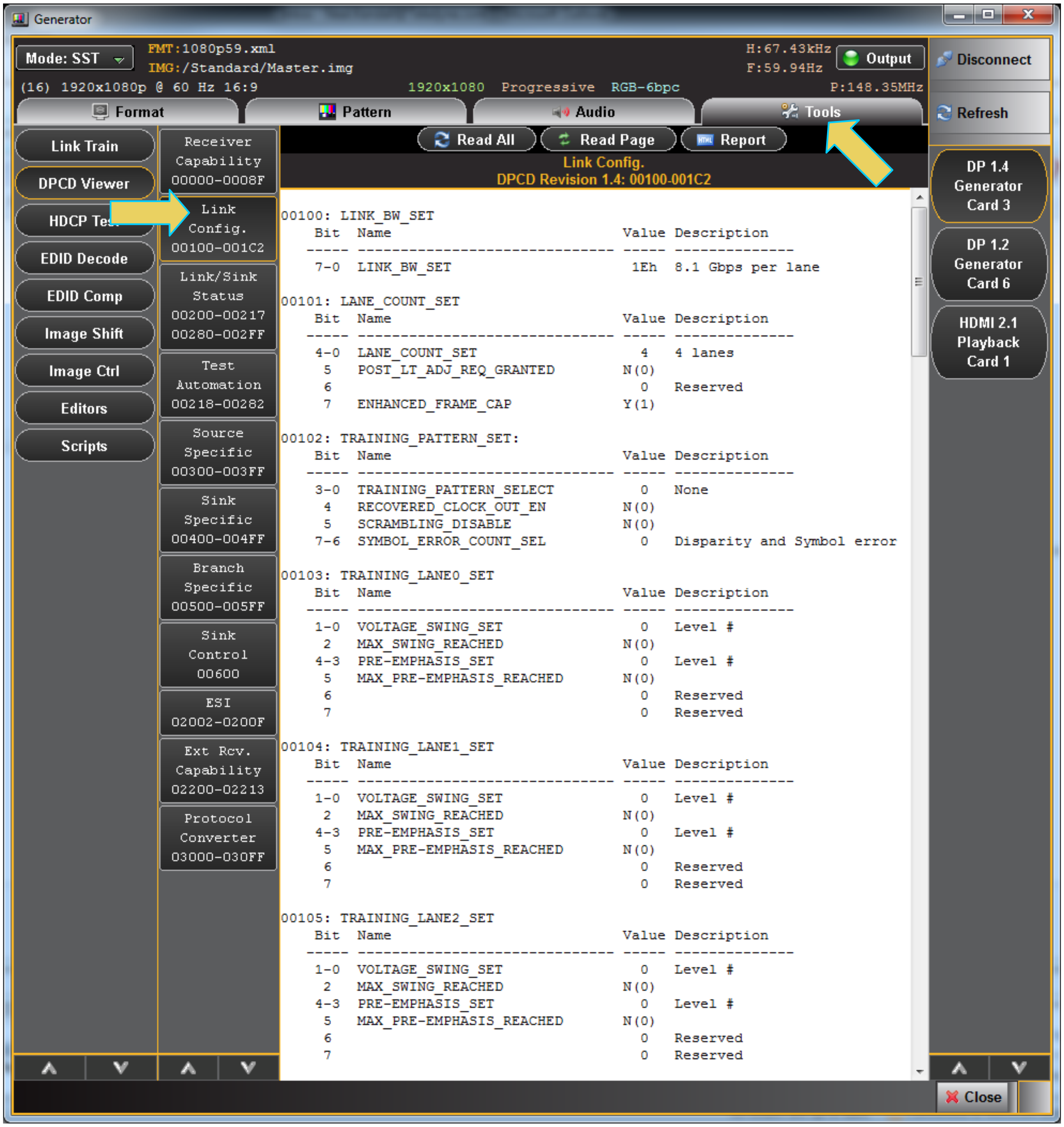
4. Activate the **DPCD Viewer** button on the upper left (indicated below).
5. Contents of the initial data in the first block of the DPCD will be displayed (below).



```
00000: DPCD_REV
    Bit  Name                           Value Description
   ----- ------------------------------ ----- --------------
    7-4  MAJOR_REV                        1
    3-0  MINOR_REV                        4

00001: MAX_LINK_RATE
    Bit  Name                           Value Description
   ----- ------------------------------ ----- --------------
    7-0  MAX_LINK_RATE                   1Eh  8.1 Gbps per lane

00002: MAX_LANE_COUNT
    Bit  Name                           Value Description
   ----- ------------------------------ ----- --------------
    4-0  MAX_LANE_COUNT                   4   4 lanes
     5   POST_LT_ADJ_REQ_SUP            N(0)
     6   TPS3_SUPPORTED                 Y(1)
     7   ENHANCED_FRAME_CAP             Y(1)

00003: MAX_DOWNSPREAD
    Bit  Name                           Value Description
   ----- ------------------------------ ----- --------------
     0   MAX_DOWNSPREAD                   1   Up to 0.5%
     1                                    0   Reserved
     2                                    0   Reserved
     3                                    0   Reserved
     4                                    0   Reserved
     5                                    0   Reserved
     6   NO_AUX_HANDSHAKE_LINK_TRAINING N(0)
     7   TPS4_SUPPORTED                 Y(1)

00004: NORP
    Bit  Name                           Value Description
   ----- ------------------------------ ----- --------------
     0   Number of receive ports          1   2 ports
     1                                    0   Reserved
     2                                    0   Reserved
     3                                    0   Reserved
     4                                    0   Reserved
     5   5V_DP_PWR_CAP                  N(0)
```

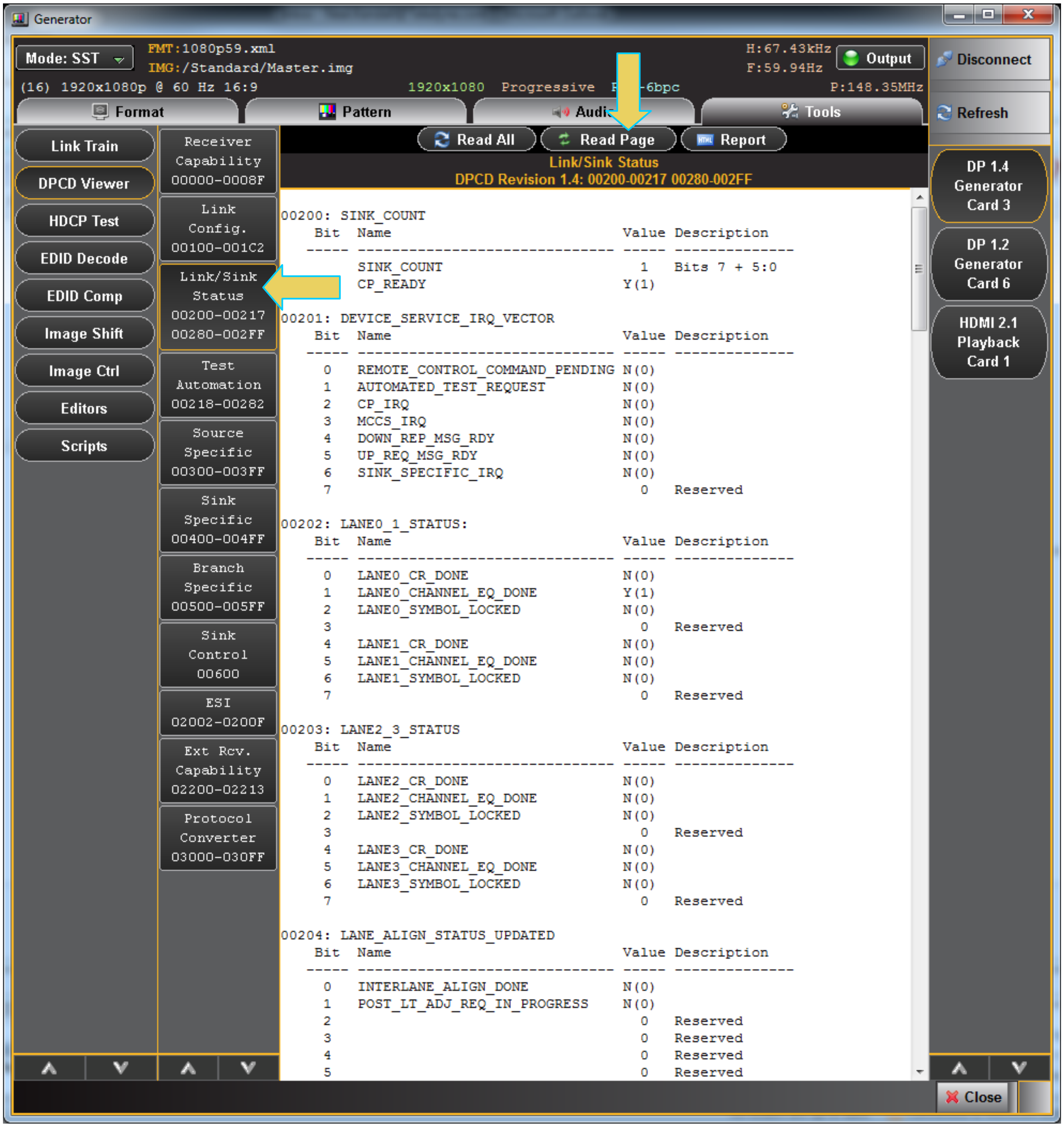
Navigate through the blocks and pages of the DPCD using the arrow buttons on the lower panel (indicated above).

6. Examples of the **DPCD Viewer** content are shown in the following screens.



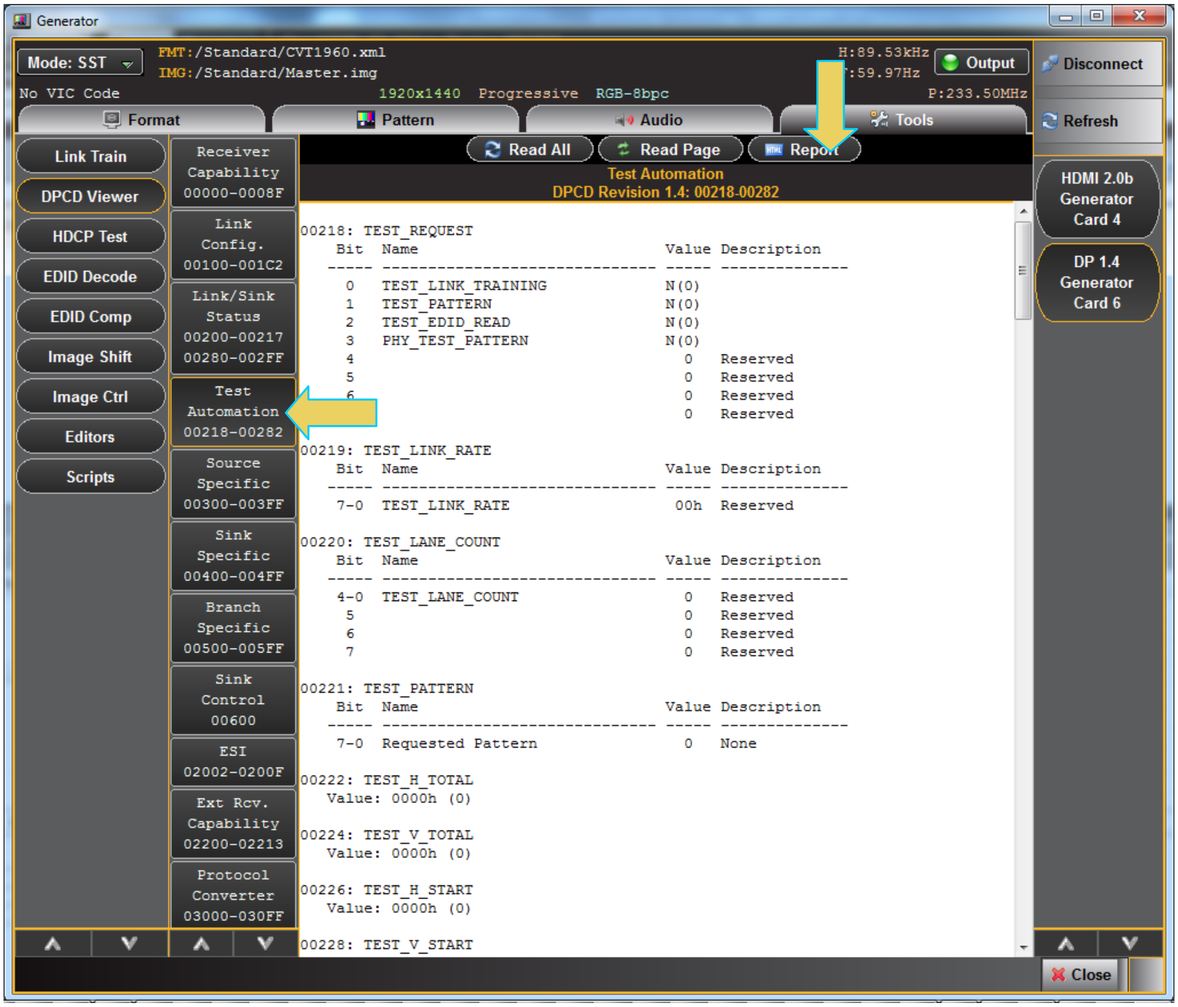
```
00100: LINK_BW_SET
   Bit  Name                            Value Description
  ----- ------------------------------ ----- --------------
   7-0  LINK_BW_SET                      1Eh  8.1 Gbps per lane

00101: LANE_COUNT_SET
   Bit  Name                            Value Description
  ----- ------------------------------ ----- --------------
   4-0  LANE_COUNT_SET                    4   4 lanes
    5   POST_LT_ADJ_REQ_GRANTED         N(0)
    6                                     0   Reserved
    7   ENHANCED_FRAME_CAP              Y(1)

00102: TRAINING_PATTERN_SET:
   Bit  Name                            Value Description
  ----- ------------------------------ ----- --------------
   3-0  TRAINING_PATTERN_SELECT           0   None
    4   RECOVERED_CLOCK_OUT_EN          N(0)
    5   SCRAMBLING_DISABLE              N(0)
   7-6  SYMBOL_ERROR_COUNT_SEL            0   Disparity and Symbol error

00103: TRAINING_LANE0_SET
   Bit  Name                            Value Description
  ----- ------------------------------ ----- --------------
   1-0  VOLTAGE_SWING_SET                 0   Level #
    2   MAX_SWING_REACHED               N(0)
   4-3  PRE-EMPHASIS_SET                  0   Level #
    5   MAX_PRE-EMPHASIS_REACHED        N(0)
    6                                     0   Reserved
    7                                     0   Reserved

00104: TRAINING_LANE1_SET
   Bit  Name                            Value Description
  ----- ------------------------------ ----- --------------
   1-0  VOLTAGE_SWING_SET                 0   Level #
    2   MAX_SWING_REACHED               N(0)
   4-3  PRE-EMPHASIS_SET                  0   Level #
    5   MAX_PRE-EMPHASIS_REACHED        N(0)
    6                                     0   Reserved
    7                                     0   Reserved

00105: TRAINING_LANE2_SET
   Bit  Name                            Value Description
  ----- ------------------------------ ----- --------------
   1-0  VOLTAGE_SWING_SET                 0   Level #
    2   MAX_SWING_REACHED               N(0)
   4-3  PRE-EMPHASIS_SET                  0   Level #
    5   MAX_PRE-EMPHASIS_REACHED        N(0)
    6                                     0   Reserved
    7                                     0   Reserved
```

View the Link/Sink Status registers.



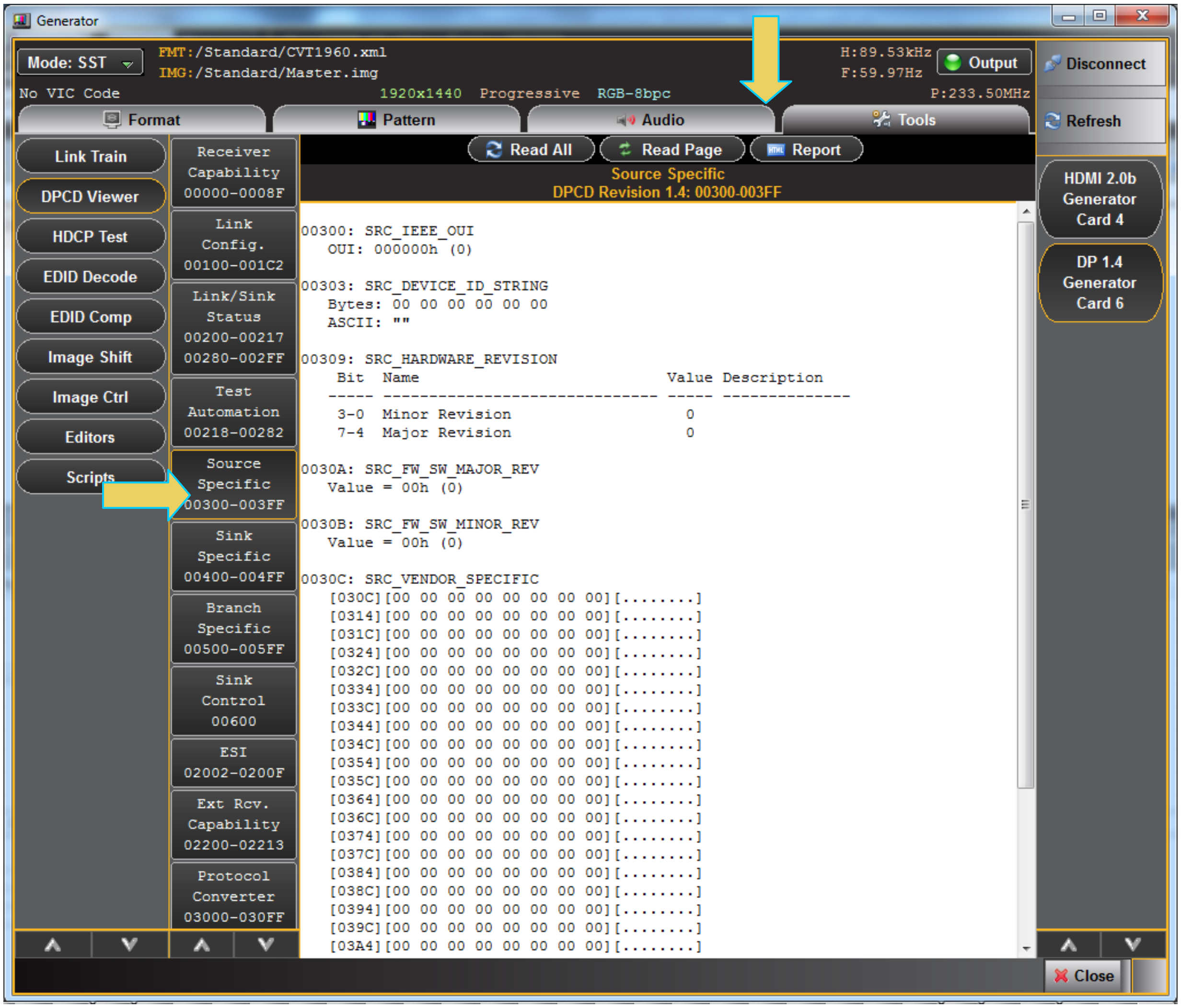
```
00200: SINK_COUNT
    Bit  Name                            Value Description
    ----- ------------------------------ ----- --------------
         SINK_COUNT                       1    Bits 7 + 5:0
         CP_READY                        Y(1)

00201: DEVICE_SERVICE_IRQ_VECTOR
    Bit  Name                            Value Description
    ----- ------------------------------ ----- --------------
      0  REMOTE_CONTROL_COMMAND_PENDING  N(0)
      1  AUTOMATED_TEST_REQUEST          N(0)
      2  CP_IRQ                          N(0)
      3  MCCS_IRQ                        N(0)
      4  DOWN_REP_MSG_RDY                N(0)
      5  UP_REQ_MSG_RDY                  N(0)
      6  SINK_SPECIFIC_IRQ               N(0)
      7                                   0    Reserved

00202: LANE0_1_STATUS:
    Bit  Name                            Value Description
    ----- ------------------------------ ----- --------------
      0  LANE0_CR_DONE                   N(0)
      1  LANE0_CHANNEL_EQ_DONE           Y(1)
      2  LANE0_SYMBOL_LOCKED             N(0)
      3                                   0    Reserved
      4  LANE1_CR_DONE                   N(0)
      5  LANE1_CHANNEL_EQ_DONE           N(0)
      6  LANE1_SYMBOL_LOCKED             N(0)
      7                                   0    Reserved

00203: LANE2_3_STATUS
    Bit  Name                            Value Description
    ----- ------------------------------ ----- --------------
      0  LANE2_CR_DONE                   N(0)
      1  LANE2_CHANNEL_EQ_DONE           N(0)
      2  LANE2_SYMBOL_LOCKED             N(0)
      3                                   0    Reserved
      4  LANE3_CR_DONE                   N(0)
      5  LANE3_CHANNEL_EQ_DONE           N(0)
      6  LANE3_SYMBOL_LOCKED             N(0)
      7                                   0    Reserved

00204: LANE_ALIGN_STATUS_UPDATED
    Bit  Name                            Value Description
    ----- ------------------------------ ----- --------------
      0  INTERLANE_ALIGN_DONE            N(0)
      1  POST_LT_ADJ_REQ_IN_PROGRESS     N(0)
      2                                   0    Reserved
      3                                   0    Reserved
      4                                   0    Reserved
      5                                   0    Reserved
```

View the Test Automation registers.



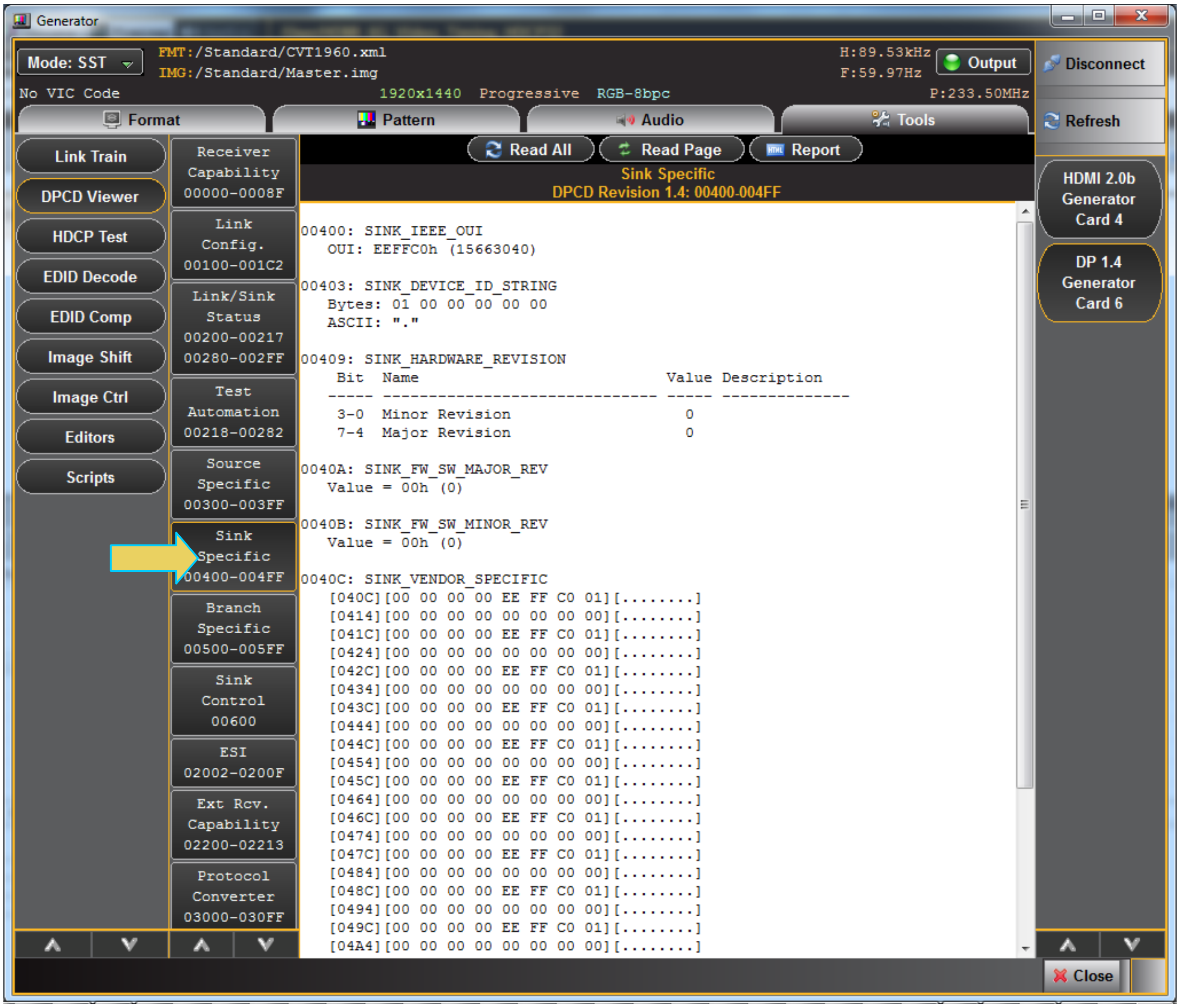
```
00218: TEST_REQUEST
   Bit  Name                              Value Description
  ----- ------------------------------    ----- --------------
    0   TEST_LINK_TRAINING                N(0)
    1   TEST_PATTERN                      N(0)
    2   TEST_EDID_READ                    N(0)
    3   PHY_TEST_PATTERN                  N(0)
    4                                       0   Reserved
    5                                       0   Reserved
    6                                       0   Reserved
                                            0   Reserved

00219: TEST_LINK_RATE
   Bit  Name                              Value Description
  ----- ------------------------------    ----- --------------
   7-0  TEST_LINK_RATE                     00h  Reserved

00220: TEST_LANE_COUNT
   Bit  Name                              Value Description
  ----- ------------------------------    ----- --------------
   4-0  TEST_LANE_COUNT                     0   Reserved
    5                                       0   Reserved
    6                                       0   Reserved
    7                                       0   Reserved

00221: TEST_PATTERN
   Bit  Name                              Value Description
  ----- ------------------------------    ----- --------------
   7-0  Requested Pattern                   0   None

00222: TEST_H_TOTAL
  Value: 0000h (0)

00224: TEST_V_TOTAL
  Value: 0000h (0)

00226: TEST_H_START
  Value: 0000h (0)

00228: TEST_V_START
```

View the Source Specific registers.



```
00300: SRC_IEEE_OUI
   OUI: 000000h (0)

00303: SRC_DEVICE_ID_STRING
   Bytes: 00 00 00 00 00 00
   ASCII: ""

00309: SRC_HARDWARE_REVISION
    Bit  Name                           Value Description
   ----- ------------------------------ ----- --------------
    3-0  Minor Revision                   0
    7-4  Major Revision                   0

0030A: SRC_FW_SW_MAJOR_REV
   Value = 00h (0)

0030B: SRC_FW_SW_MINOR_REV
   Value = 00h (0)

0030C: SRC_VENDOR_SPECIFIC
   [030C][00 00 00 00 00 00 00 00][........]
   [0314][00 00 00 00 00 00 00 00][........]
   [031C][00 00 00 00 00 00 00 00][........]
   [0324][00 00 00 00 00 00 00 00][........]
   [032C][00 00 00 00 00 00 00 00][........]
   [0334][00 00 00 00 00 00 00 00][........]
   [033C][00 00 00 00 00 00 00 00][........]
   [0344][00 00 00 00 00 00 00 00][........]
   [034C][00 00 00 00 00 00 00 00][........]
   [0354][00 00 00 00 00 00 00 00][........]
   [035C][00 00 00 00 00 00 00 00][........]
   [0364][00 00 00 00 00 00 00 00][........]
   [036C][00 00 00 00 00 00 00 00][........]
   [0374][00 00 00 00 00 00 00 00][........]
   [037C][00 00 00 00 00 00 00 00][........]
   [0384][00 00 00 00 00 00 00 00][........]
   [038C][00 00 00 00 00 00 00 00][........]
   [0394][00 00 00 00 00 00 00 00][........]
   [039C][00 00 00 00 00 00 00 00][........]
   [03A4][00 00 00 00 00 00 00 00][........]
```

View the Sink Specific registers.

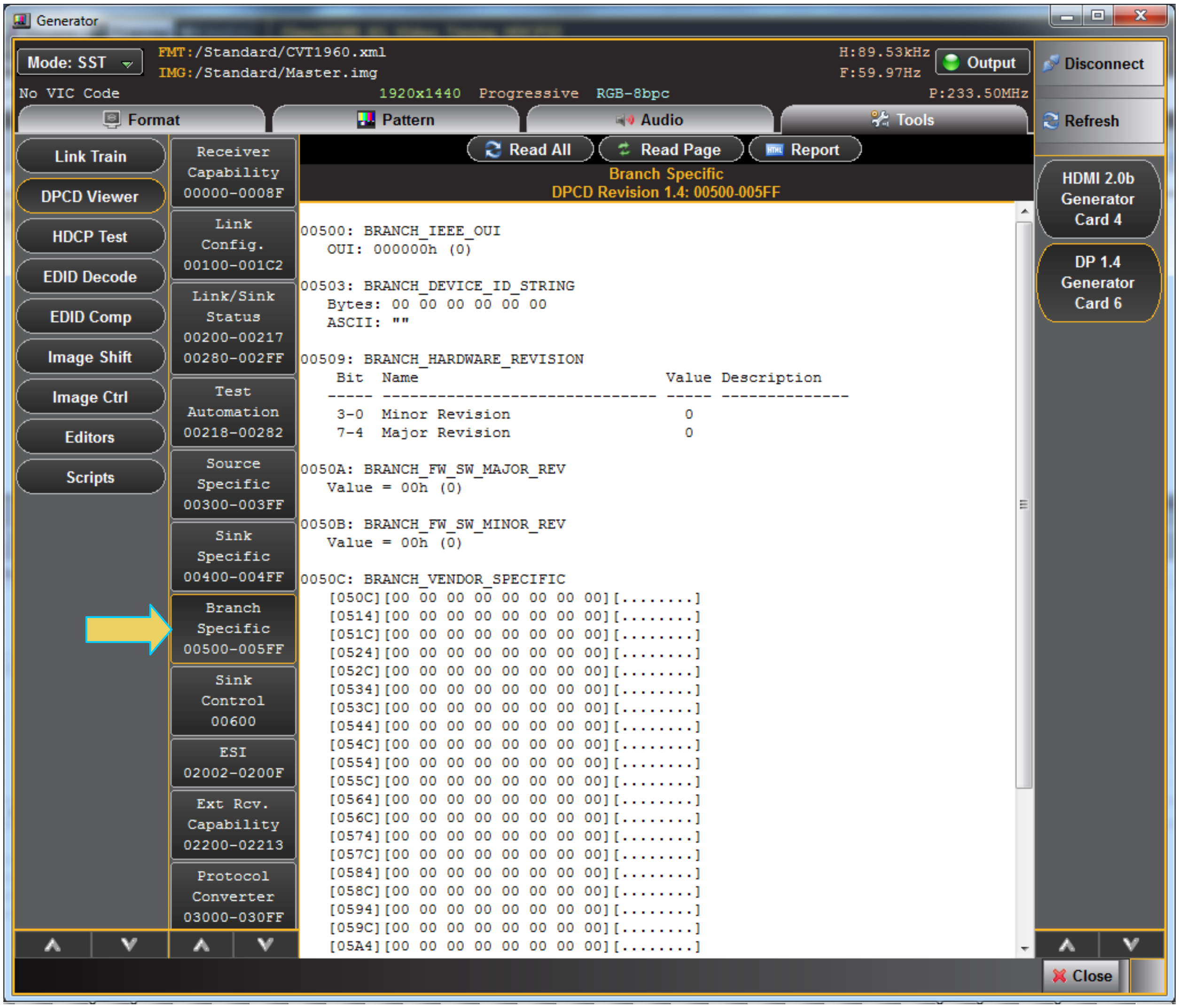


Mode: SST
FMT:/Standard/CVT1960.xml
IMG:/Standard/Master.img
No VIC Code
1920x1440 Progressive RGB-8bpc
H:89.53kHz
F:59.97Hz
P:233.50MHz

Sink Specific
DPCD Revision 1.4: 00400-004FF

```
00400: SINK_IEEE_OUI
   OUI: EEFFC0h (15663040)

00403: SINK_DEVICE_ID_STRING
   Bytes: 01 00 00 00 00 00
   ASCII: "."

00409: SINK_HARDWARE_REVISION
    Bit  Name                           Value Description
   ----- ------------------------------ ----- --------------
    3-0  Minor Revision                   0
    7-4  Major Revision                   0

0040A: SINK_FW_SW_MAJOR_REV
   Value = 00h (0)

0040B: SINK_FW_SW_MINOR_REV
   Value = 00h (0)

0040C: SINK_VENDOR_SPECIFIC
   [040C][00 00 00 00 EE FF C0 01][........]
   [0414][00 00 00 00 00 00 00 00][........]
   [041C][00 00 00 00 EE FF C0 01][........]
   [0424][00 00 00 00 00 00 00 00][........]
   [042C][00 00 00 00 EE FF C0 01][........]
   [0434][00 00 00 00 00 00 00 00][........]
   [043C][00 00 00 00 EE FF C0 01][........]
   [0444][00 00 00 00 00 00 00 00][........]
   [044C][00 00 00 00 EE FF C0 01][........]
   [0454][00 00 00 00 00 00 00 00][........]
   [045C][00 00 00 00 EE FF C0 01][........]
   [0464][00 00 00 00 00 00 00 00][........]
   [046C][00 00 00 00 EE FF C0 01][........]
   [0474][00 00 00 00 00 00 00 00][........]
   [047C][00 00 00 00 EE FF C0 01][........]
   [0484][00 00 00 00 00 00 00 00][........]
   [048C][00 00 00 00 EE FF C0 01][........]
   [0494][00 00 00 00 00 00 00 00][........]
   [049C][00 00 00 00 EE FF C0 01][........]
   [04A4][00 00 00 00 00 00 00 00][........]
```

View the Branch Specific register.

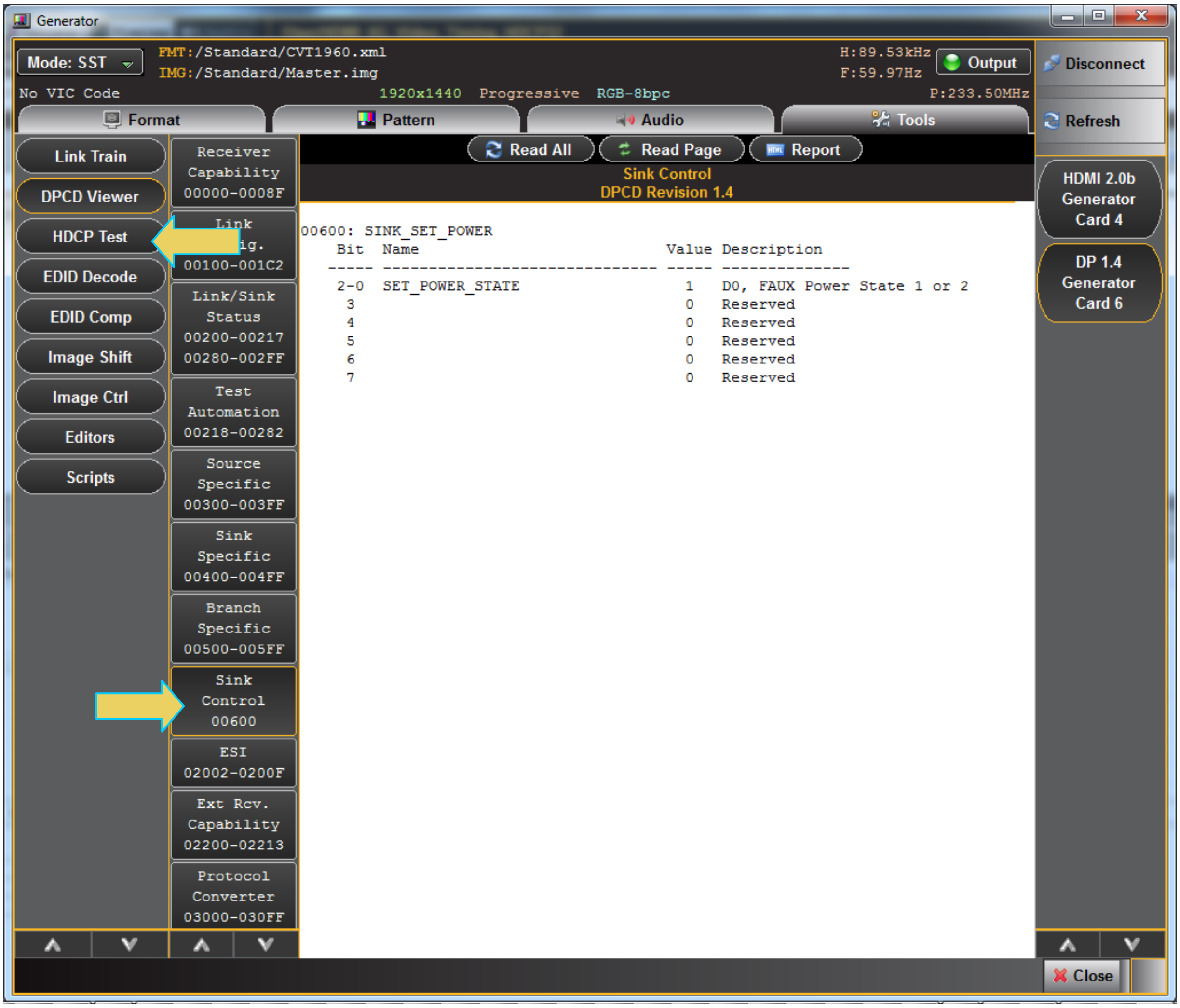


```
FMT:/Standard/CVT1960.xml                                    H:89.53kHz
IMG:/Standard/Master.img                                     F:59.97Hz
No VIC Code              1920x1440  Progressive  RGB-8bpc    P:233.50MHz
```

Branch Specific
DPCD Revision 1.4: 00500-005FF

```
00500: BRANCH_IEEE_OUI
   OUI: 000000h (0)

00503: BRANCH_DEVICE_ID_STRING
   Bytes: 00 00 00 00 00 00
   ASCII: ""

00509: BRANCH_HARDWARE_REVISION
    Bit  Name                           Value Description
   ----- ------------------------------ ----- --------------
    3-0  Minor Revision                   0
    7-4  Major Revision                   0

0050A: BRANCH_FW_SW_MAJOR_REV
   Value = 00h (0)

0050B: BRANCH_FW_SW_MINOR_REV
   Value = 00h (0)

0050C: BRANCH_VENDOR_SPECIFIC
   [050C][00 00 00 00 00 00 00 00][........]
   [0514][00 00 00 00 00 00 00 00][........]
   [051C][00 00 00 00 00 00 00 00][........]
   [0524][00 00 00 00 00 00 00 00][........]
   [052C][00 00 00 00 00 00 00 00][........]
   [0534][00 00 00 00 00 00 00 00][........]
   [053C][00 00 00 00 00 00 00 00][........]
   [0544][00 00 00 00 00 00 00 00][........]
   [054C][00 00 00 00 00 00 00 00][........]
   [0554][00 00 00 00 00 00 00 00][........]
   [055C][00 00 00 00 00 00 00 00][........]
   [0564][00 00 00 00 00 00 00 00][........]
   [056C][00 00 00 00 00 00 00 00][........]
   [0574][00 00 00 00 00 00 00 00][........]
   [057C][00 00 00 00 00 00 00 00][........]
   [0584][00 00 00 00 00 00 00 00][........]
   [058C][00 00 00 00 00 00 00 00][........]
   [0594][00 00 00 00 00 00 00 00][........]
   [059C][00 00 00 00 00 00 00 00][........]
   [05A4][00 00 00 00 00 00 00 00][........]
```

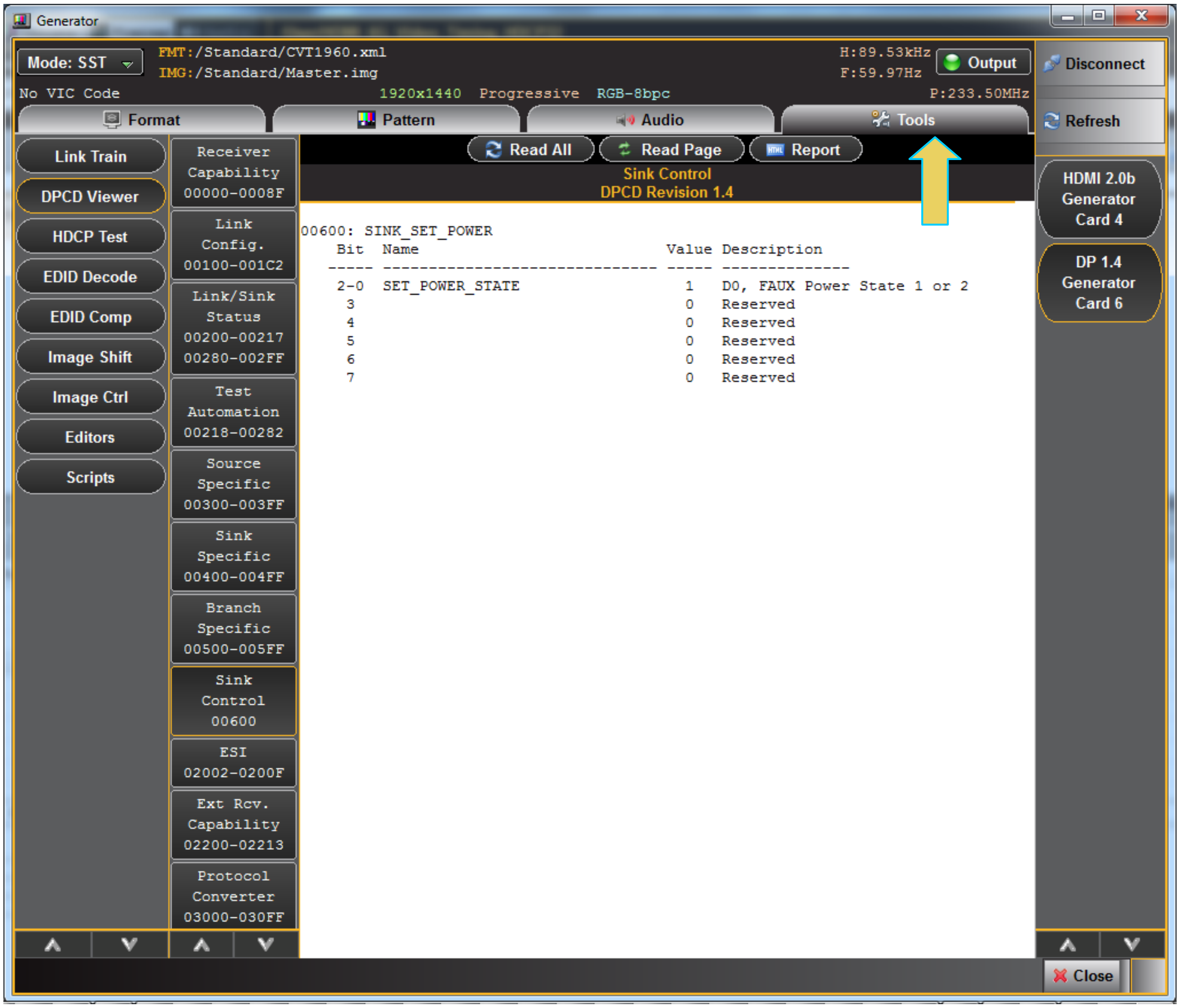
View the Sink Control registers.



```
00600: SINK_SET_POWER
    Bit  Name                              Value Description
   ----- --------------------------------- ----- --------------
    2-0  SET_POWER_STATE                       1  D0, FAUX Power State 1 or 2
     3                                         0  Reserved
     4                                         0  Reserved
     5                                         0  Reserved
     6                                         0  Reserved
     7                                         0  Reserved
```

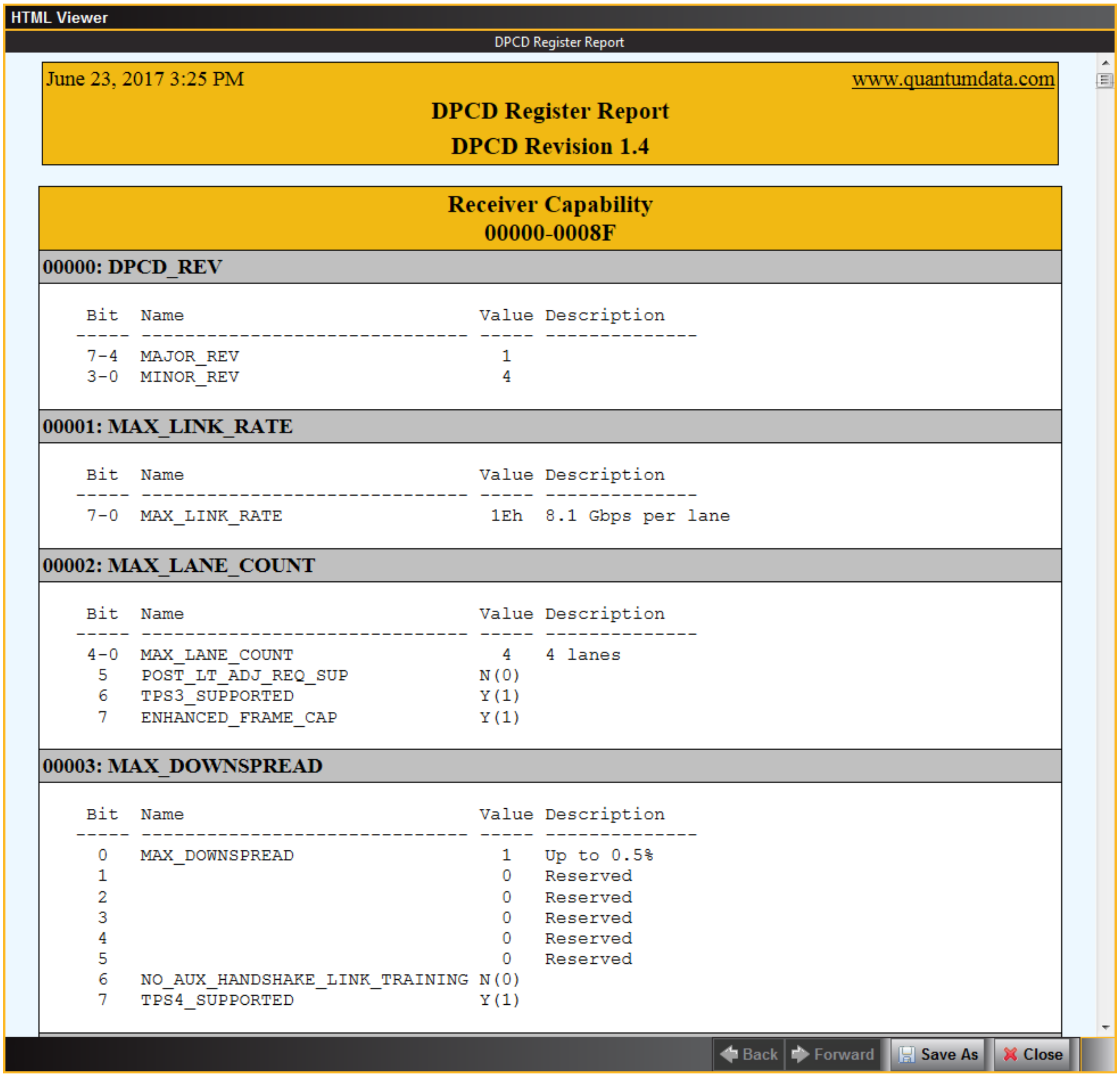
To view the DPCD of a connected display:

1. From the **DPCD Tool** select **Report** on the upper right.



```
00600: SINK_SET_POWER
    Bit  Name                           Value Description
   ----- ------------------------------ ----- --------------
    2-0  SET_POWER_STATE                  1   D0, FAUX Power State 1 or 2
    3                                     0   Reserved
    4                                     0   Reserved
    5                                     0   Reserved
    6                                     0   Reserved
    7                                     0   Reserved
```

The following are sample screen shots from the DPCD HTML report.



June 23, 2017 3:25 PM www.quantumdata.com

DPCD Register Report

DPCD Revision 1.4

Receiver Capability
00000-0008F

00000: DPCD_REV

```
 Bit  Name                           Value Description
----- ------------------------------ ----- --------------
 7-4  MAJOR_REV                        1
 3-0  MINOR_REV                        4
```

00001: MAX_LINK_RATE

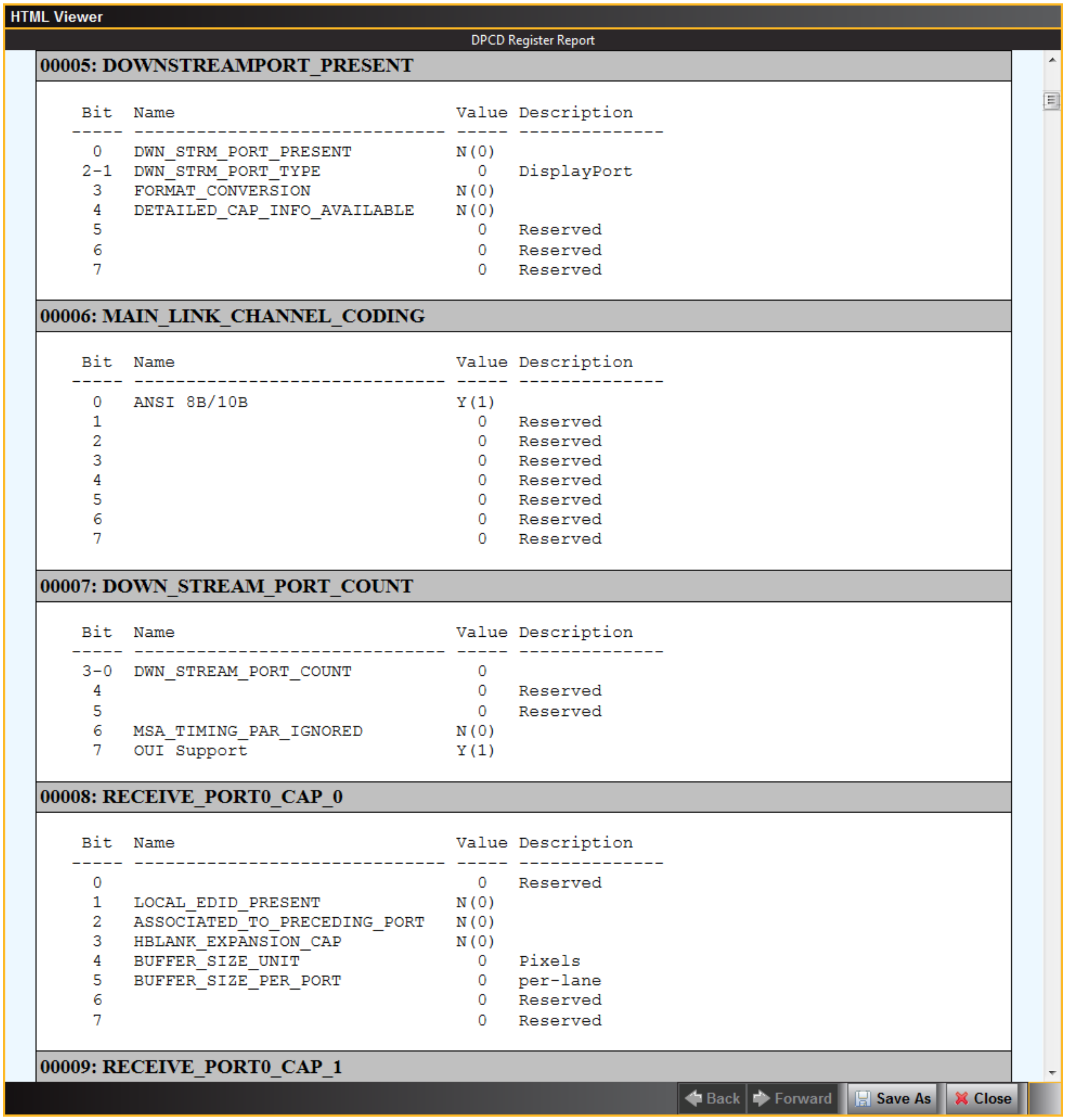
```
 Bit  Name                           Value Description
----- ------------------------------ ----- --------------
 7-0  MAX_LINK_RATE                   1Eh  8.1 Gbps per lane
```

00002: MAX_LANE_COUNT

```
 Bit  Name                           Value Description
----- ------------------------------ ----- --------------
 4-0  MAX_LANE_COUNT                   4   4 lanes
  5   POST_LT_ADJ_REQ_SUP            N(0)
  6   TPS3_SUPPORTED                 Y(1)
  7   ENHANCED_FRAME_CAP             Y(1)
```

00003: MAX_DOWNSPREAD

```
 Bit  Name                           Value Description
----- ------------------------------ ----- --------------
  0   MAX_DOWNSPREAD                   1   Up to 0.5%
  1                                    0   Reserved
  2                                    0   Reserved
  3                                    0   Reserved
  4                                    0   Reserved
  5                                    0   Reserved
  6   NO_AUX_HANDSHAKE_LINK_TRAINING N(0)
  7   TPS4_SUPPORTED                 Y(1)
```



00005: DOWNSTREAMPORT_PRESENT

```
 Bit  Name                           Value Description
----- ------------------------------ ----- --------------
  0   DWN_STRM_PORT_PRESENT          N(0)
 2-1  DWN_STRM_PORT_TYPE               0   DisplayPort
  3   FORMAT_CONVERSION              N(0)
  4   DETAILED_CAP_INFO_AVAILABLE    N(0)
  5                                    0   Reserved
  6                                    0   Reserved
  7                                    0   Reserved
```

00006: MAIN_LINK_CHANNEL_CODING

```
 Bit  Name                           Value Description
----- ------------------------------ ----- --------------
  0   ANSI 8B/10B                    Y(1)
  1                                    0   Reserved
  2                                    0   Reserved
  3                                    0   Reserved
  4                                    0   Reserved
  5                                    0   Reserved
  6                                    0   Reserved
  7                                    0   Reserved
```

00007: DOWN_STREAM_PORT_COUNT

```
 Bit  Name                           Value Description
----- ------------------------------ ----- --------------
 3-0  DWN_STREAM_PORT_COUNT            0
  4                                    0   Reserved
  5                                    0   Reserved
  6   MSA_TIMING_PAR_IGNORED         N(0)
  7   OUI Support                    Y(1)
```

00008: RECEIVE_PORT0_CAP_0

```
 Bit  Name                           Value Description
----- ------------------------------ ----- --------------
  0                                    0   Reserved
  1   LOCAL_EDID_PRESENT             N(0)
  2   ASSOCIATED_TO_PRECEDING_PORT   N(0)
  3   HBLANK_EXPANSION_CAP           N(0)
  4   BUFFER_SIZE_UNIT                 0   Pixels
  5   BUFFER_SIZE_PER_PORT             0   per-lane
  6                                    0   Reserved
  7                                    0   Reserved
```

00009: RECEIVE_PORT0_CAP_1

3.14 Testing HDCP on a connected display

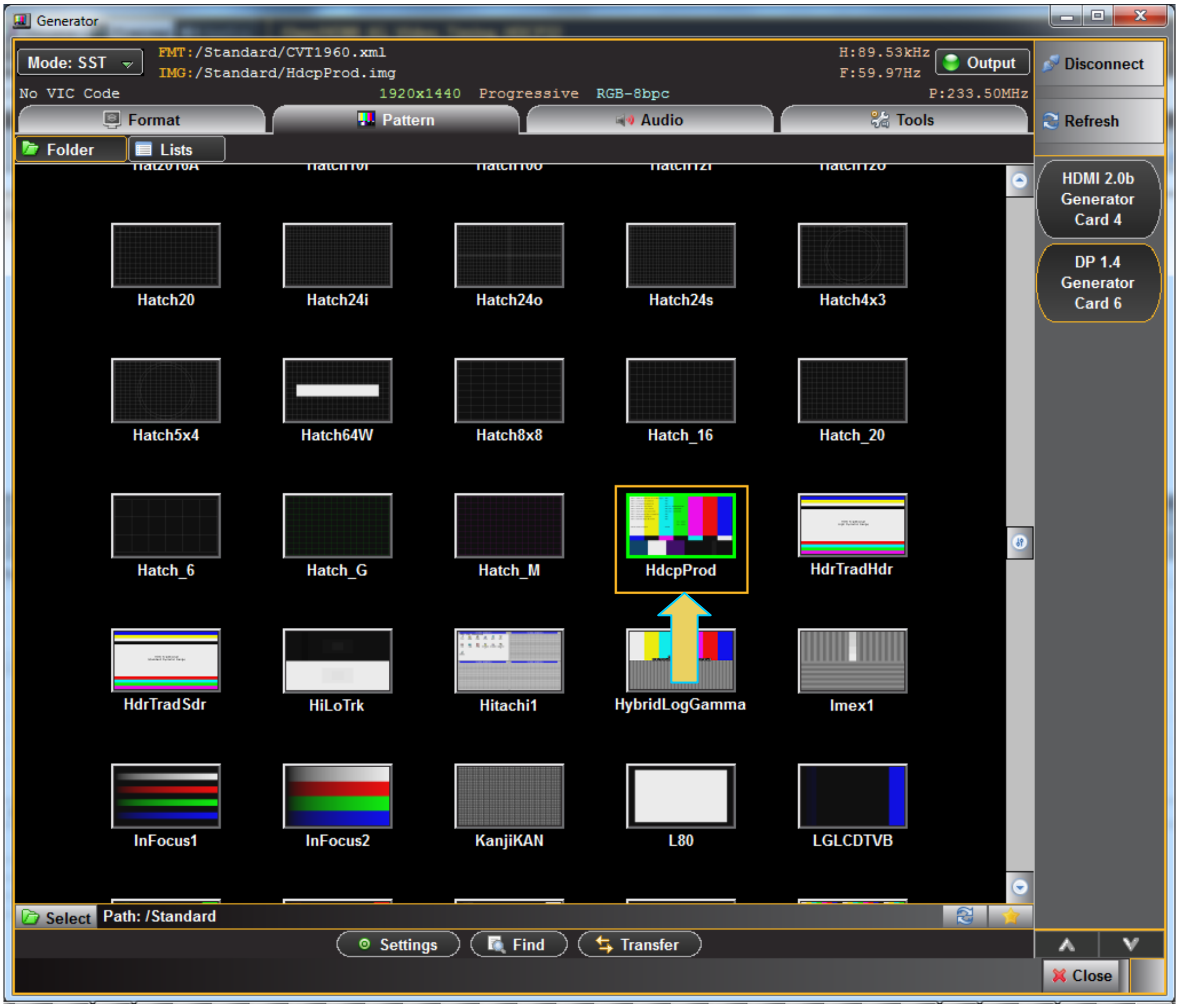
Use the following procedures to test HDCP 1.3 authentication on a connected display. HDPC is tested using a special test image called HDCPProd and HDCP2. You can also run the HDCP test using the HDCP test utility. When running the test with the HDCPprod test image you can view the results of the test on the connected DP display. These test images are selectable through the **Pattern** tab.

3.14.1 Running the HDCP test using the HDCPprod test image

Use the procedures below to run an HDCP test on a connected display using the HDCPprod test image.

To test HDCP on a connected display:

1. Access the **Pattern** tab to view the test patterns and select HDCPprod test image.



The results and status of the test can be viewed in the connected DP display.

A typical result is shown below.

```
STEP  1: Reset the transmitter                               - PASS
STEP  2: Initialize the transmitter                          - PASS
STEP  3: At transmitter generate An                          - PASS
STEP  4: Write An to the receiver                            - PASS
STEP  5: Write the transmitter KSV to the receiver           - PASS, Aksv = 0x91584AD36F
STEP  6: Read and verify the receiver KSV                    - PASS, Bksv = 0x9C116E35EA
STEP  7: Write receiver KSV to transmitter                   - PASS
STEP  8: Ri ready at transmitter                             - PASS
STEP  9: Read and compare transmitter Ri with receiver Ri    - PASS
                                       RiTX = 0xA543
                                       RiRX = 0xA543
STEP 10: Generate authentication                             - PASS
STEP 11: Transmitting encrypted data                         - TESTING

          HDCP test passed as long as you can read this.
                           RiTX = 0x73C7
                           RiRX = 0x73C7
PASS                             4
```

2. Select the HdcpProd test image if your sink device under test is connected to Port 0 (Tx1); select Hdcp2 if your sink device under test is connected to Port 1 (Tx2).

To test HDCP on a connected display using the Tools HDCP utility:

1. Access the **HDCP Test** through the **Tools** tab as shown below.

```
FMT:/Standard/CVT2560H.xml                H:135.00kHz
IMG:/Standard/SmpteBar.img                F:60.00Hz
(97) 3840x2160p @ 60 Hz 16:9    3840x2160  Progressive  RGB-8bpc    P:594.00MHz
```

HDCP Mode

○ None ○ 1.3 ● 2.2

Key Type

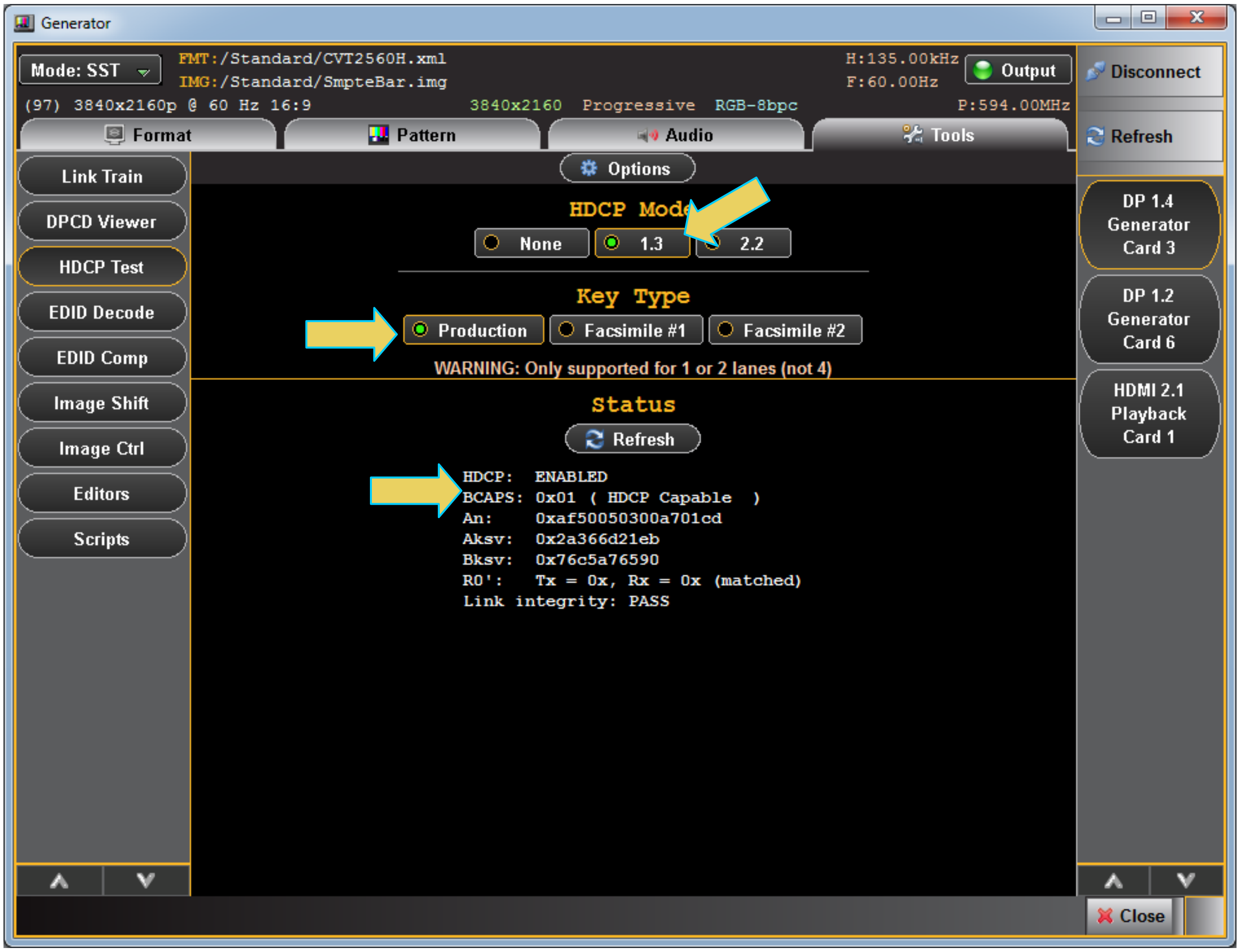
● Production ○ Facsimile #1

Status

Refresh

```
HDCP2ENABLED  :YES
RXHDCP2ENABLED:YES
RCV ID        :0 0 0 0 0
RXCAPS        :0 0 0
AKE_INIT      :SND_VALID
RX_CERT       :RCVD_INVALID
STORED_KM     :NOT_RCVD
NO_STORED_KM  :NOT_RCVD
HPRIME        :NOT_RCVD
PAIRING       :NOT_RCVD
LC_INIT       :NOT_RCVD
LPRIME        :NOT_RCVD
SKE           :NOT_RCVD
AUTHENTICATED :NO
REPAUTH_RCVIDLST:NOT_RCVD
RCVIDLST_ACK  :MSG_NOT_SND
STRM_MGMT     :MSG_NOT_SND
STRM_RDY      :NOT_RCVD
STRM_TYP      :0
DEPTH         :0
DEV_COUNT     :0
```

2. Enable HDCP using the **Enable** radio button. Then hit the **Refresh** button. View the results and status of the test through the HDCP Test screen as shown below.



```
HDCP:  ENABLED
BCAPS: 0x01 ( HDCP Capable  )
An:    0xaf50050300a701cd
Aksv:  0x2a366d21eb
Bksv:  0x76c5a76590
R0':   Tx = 0x, Rx = 0x (matched)
Link integrity: PASS
```

3.14.2 Understanding the HDCP test

The DP HDCP test sequence performed by the 980 DP Video Generator is listed below.

1. Reset the transmitter HDCP engine.
2. Initialize the transmitter.
3. Check Bcaps over the DDC bus to determine if the sink is a receiver or a repeater and generate a new An value (8 byte random session number) in the transmitter.
4. Transmitter writes An to the receiver using the DDC bus.
5. Transmitter writes Aksv to the receiver using the DDC bus.
6. Read Bksv from the receiver over the DDC bus and validate that it has exactly 20 zeroes and 20 ones in it. You can query this value with the following command:
7. The display may return a value such as the following which is:

   07BE05CEA9

8. The value in binary is 0000011110111110000001011100111010101001 which contains 20 zeros and 20 ones.
9. Write the Bksv value to the transmitter to trigger calculation of R0.
10. Wait for the R0 calculation in the transmitter to complete.
11. Wait for at least 100 milliseconds and then read the R0' value out of the receiver over the DDC bus and compare the value with the R0 calculation in the transmitter. If this step fails, then go to step 1.
12. Enable encryption and read Ri' from the receiver over the DDC bus every 128 frames and compare it to the Ri value calculated in the transmitter. As long as the Ri value matches the Ri' value from the receiver continue to check these every 128 frames.

4 HDCP 2.2 Tests

This chapter describes how to use the 980 DisplayPort Video Generator / Analyzer module to test your DisplayPort 1.2 source, sink or repeater for proper HDCP 2.2 authentication. The HDCP 2.2 functional tests are optional features and require the purchase of a license to run.

The module's DisplayPort 1.4 Tx port emulates a DisplayPort 1.4 source device with HDCP 2.2 capabilities. The module's DisplayPort Rx port emulates either a DisplayPort 1.4 sink device with HDCP 2.2 capabilities or a repeater device to test a source against an HDCP 2.2 repeater functionality.

The solutions enable you to quickly verify the HDCP authentication function of your HDCP 2.2-capable DisplayPort 1.4 device. Functional testing early in the development cycle is important for assessing and ensuring basic functionality. You can view a summary of the authentication status at a glance from the dialog boxes and from the Real Time status bar at the top of the 980 GUI window.

Whether testing a source, sink or repeater you can view the HDCP 2.2 authentication transactions in real time using the Auxiliary Channel Analyzer (ACA) utility. You can save the ACA trace records and disseminate them to subject matter experts for further analysis.

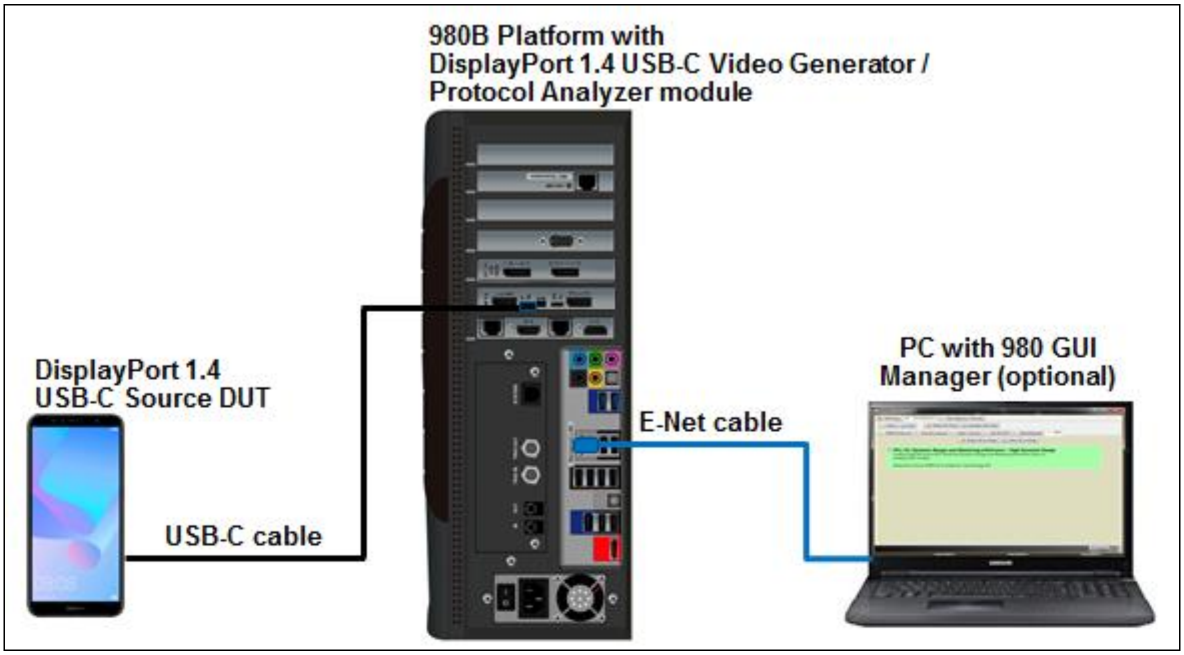
4.1 Running an HDCP 2.2 source test

The procedures below describe how to run the HDCP 2.2 authentication on a DisplayPort source device.

To run the HDCP 2.2 authentication test on a source:

1. Connect the DP source device to the DP module's Rx Analyzer port as shown below.

   Note the PC shown is used for the external 980 GUI Manager application. In this case you will use the embedded 980 GUI Manager application on the 980 Test Platform.

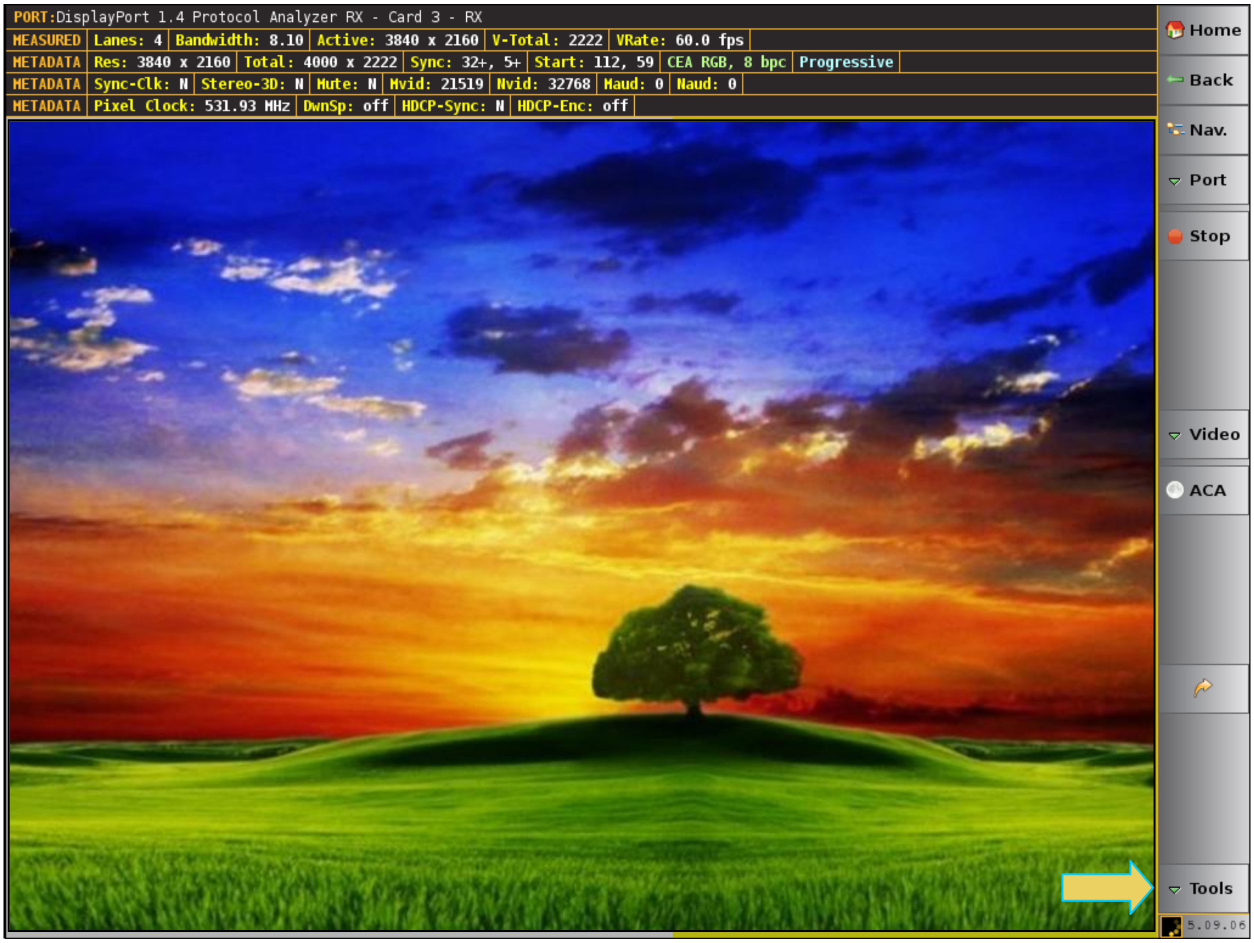


2. Enable HDCP 2.2 on the source device under test. Note that you can either enable HDCP 2.2 prior to enabling HDCP 2.2 on the 980 Video Generator / Analyzer module's Rx card or you can enable HDCP on the source after you enable HDCP on the DP module.

3. Touch select the **DP RX** icon on the **Card Control** page of the **Apps** panel on the *embedded* 980 GUI Manager (see below).

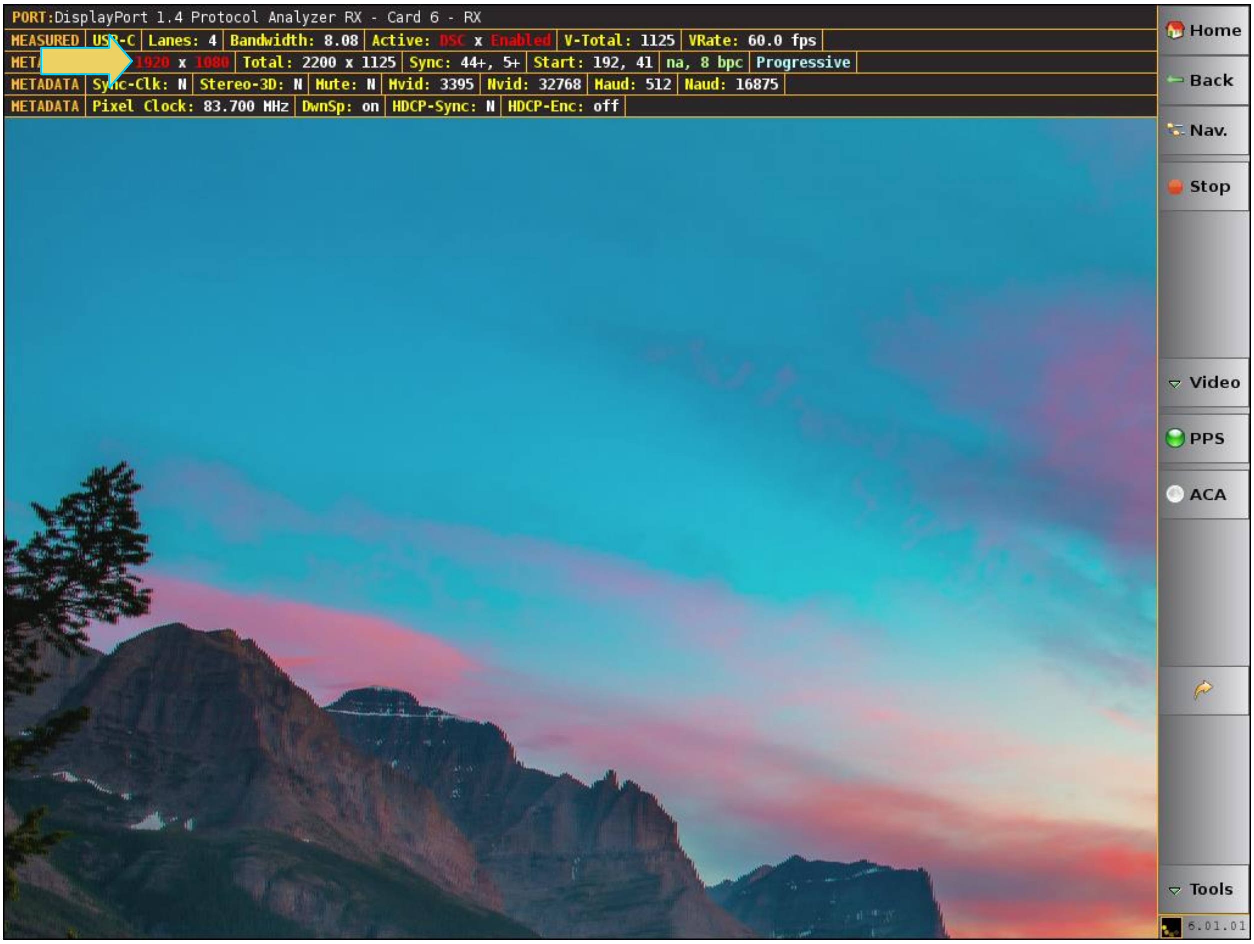
   Note: The Real Time viewing windows are not available on the PC-based external GUI Manager. Therefore to enable HDCP 2.2 on the DP module's Rx port, please use the 980's embedded touch screen.

The Receiver "Real Time" panel appears as shown below. There are a few examples showing DSC and USB-C ports used as the inputs.



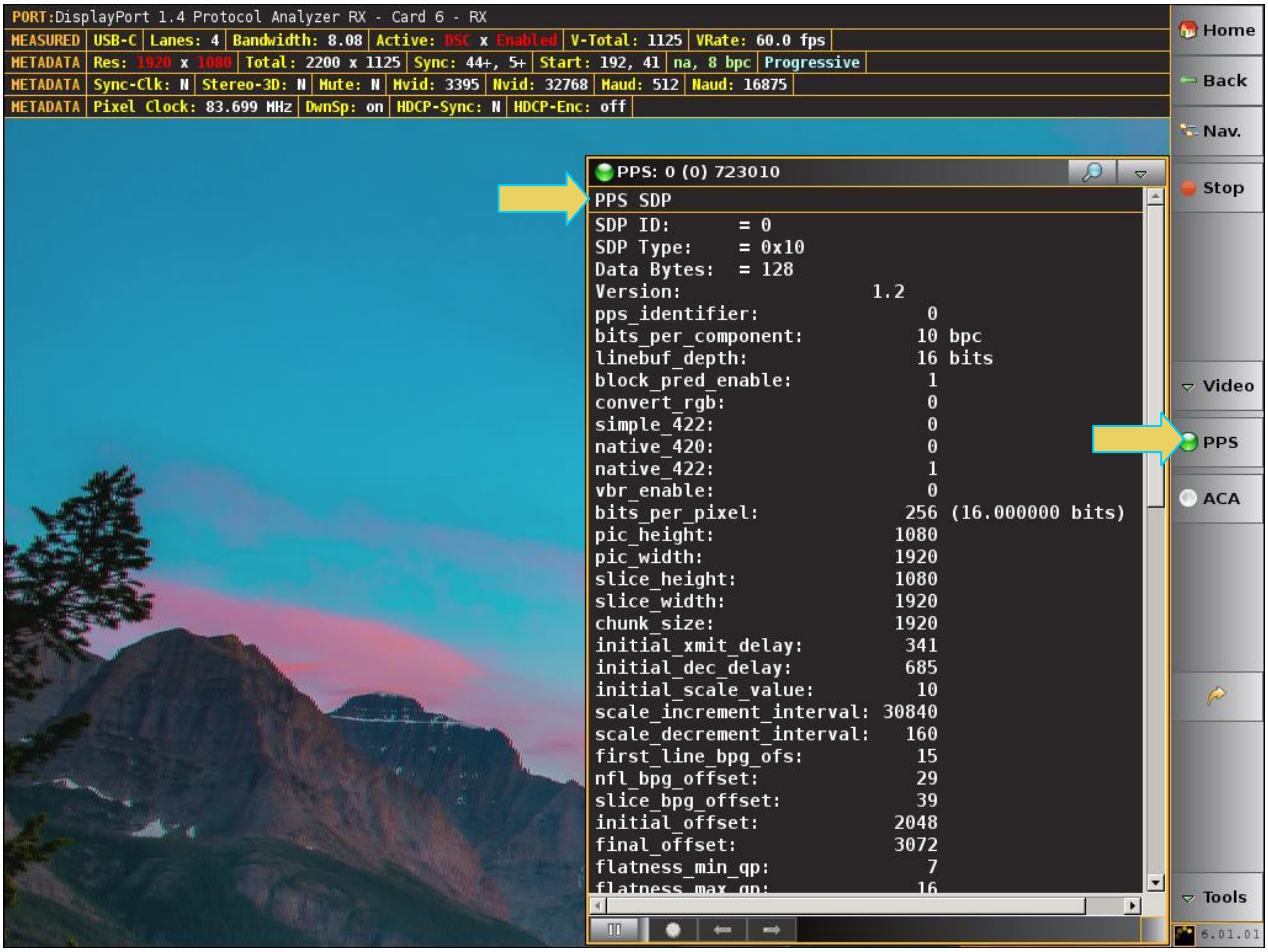
```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 3 - RX
MEASURED | Lanes: 4 | Bandwidth: 8.10 | Active: 3840 x 2160 | V-Total: 2222 | VRate: 60.0 fps
METADATA | Res: 3840 x 2160 | Total: 4000 x 2222 | Sync: 32+, 5+ | Start: 112, 59 | CEA RGB, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 21519 | Nvid: 32768 | Maud: 0 | Naud: 0
METADATA | Pixel Clock: 531.93 MHz | DwnSp: off | HDCP-Sync: N | HDCP-Enc: off
```

Example below shows a DSC input real time input.



```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 6 - RX
MEASURED | USB-C | Lanes: 4 | Bandwidth: 8.08 | Active: DSC x Enabled | V-Total: 1125 | VRate: 60.0 fps
META 1920 x 1080 | Total: 2200 x 1125 | Sync: 44+, 5+ | Start: 192, 41 | na, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 3395 | Nvid: 32768 | Maud: 512 | Naud: 16875
METADATA | Pixel Clock: 83.700 MHz | DwnSp: on | HDCP-Sync: N | HDCP-Enc: off
```

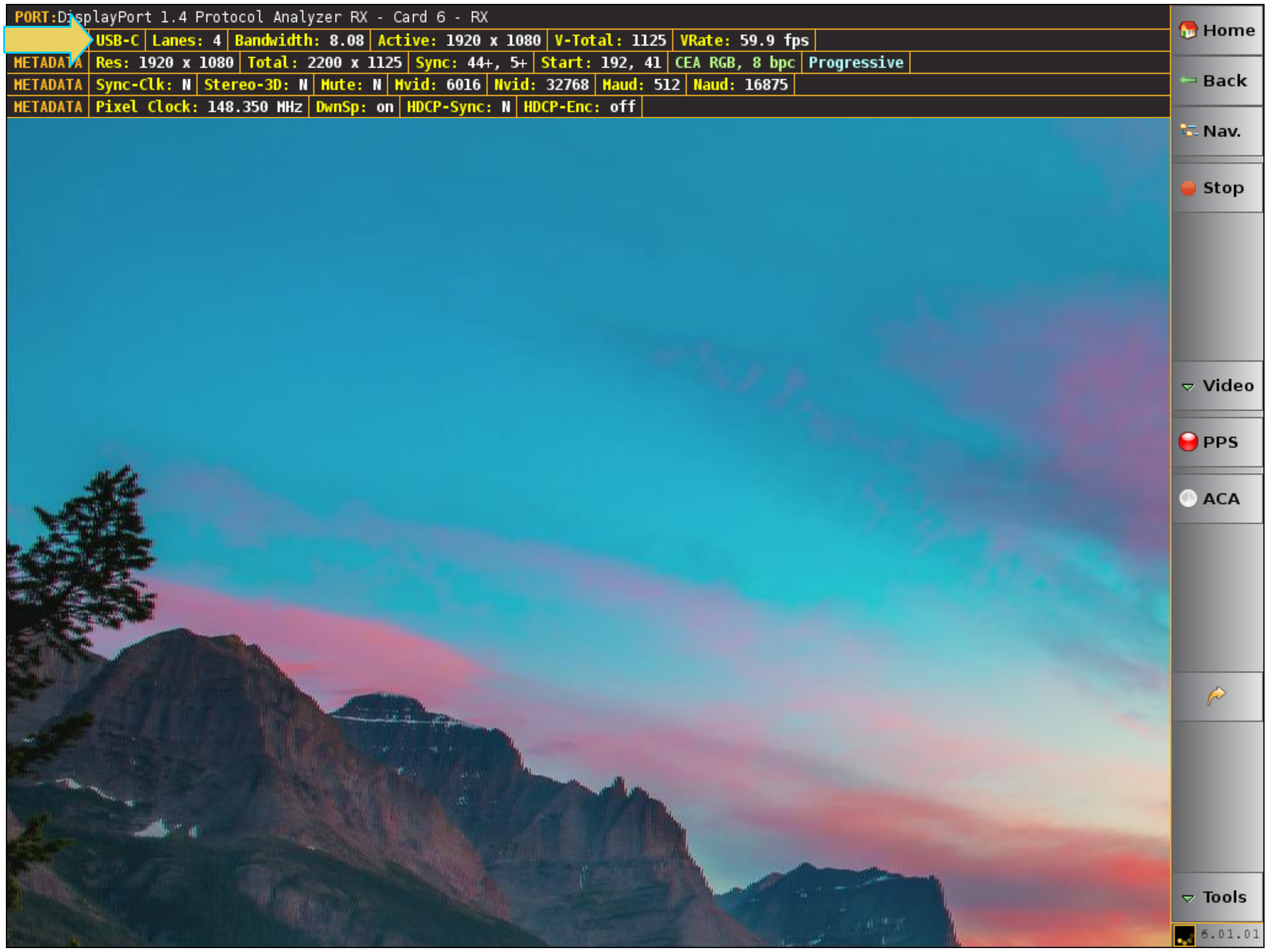
And below with the DSC Picture Parameter Set (PPS) panel shown.



```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 6 - RX
MEASURED | USB-C | Lanes: 4 | Bandwidth: 8.08 | Active: DSC x Enabled | V-Total: 1125 | VRate: 60.0 fps
METADATA | Res: 1920 x 1080 | Total: 2200 x 1125 | Sync: 44+, 5+ | Start: 192, 41 | na, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 3395 | Nvid: 32768 | Maud: 512 | Naud: 16875
METADATA | Pixel Clock: 83.699 MHz | DwnSp: on | HDCP-Sync: N | HDCP-Enc: off
```

```
PPS: 0 (0) 723010
PPS SDP
SDP ID:       = 0
SDP Type:     = 0x10
Data Bytes:   = 128
Version:                   1.2
pps_identifier:               0
bits_per_component:          10 bpc
linebuf_depth:               16 bits
block_pred_enable:            1
convert_rgb:                  0
simple_422:                   0
native_420:                   0
native_422:                   1
vbr_enable:                   0
bits_per_pixel:             256 (16.000000 bits)
pic_height:                1080
pic_width:                 1920
slice_height:              1080
slice_width:               1920
chunk_size:                1920
initial_xmit_delay:         341
initial_dec_delay:          685
initial_scale_value:         10
scale_increment_interval: 30840
scale_decrement_interval:   160
first_line_bpg_ofs:          15
nfl_bpg_offset:              29
slice_bpg_offset:            39
initial_offset:            2048
final_offset:              3072
flatness_min_qp:              7
flatness_max_qp:             16
```

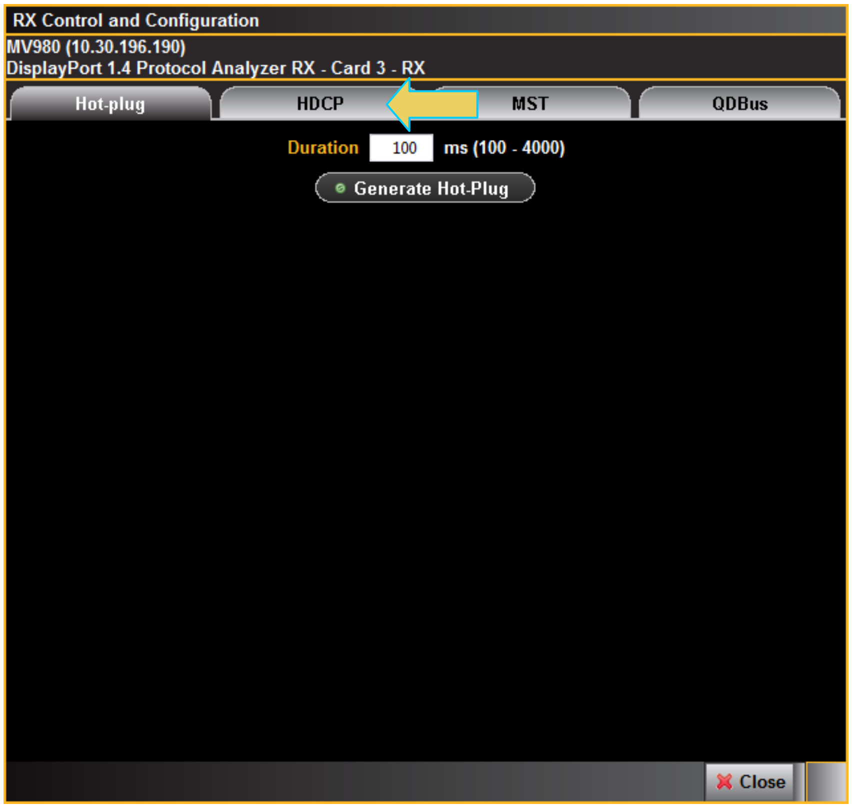
Example below shows a USB-C input real time input.



```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 6 - RX
USB-C | Lanes: 4 | Bandwidth: 8.08 | Active: 1920 x 1080 | V-Total: 1125 | VRate: 59.9 fps
METADATA | Res: 1920 x 1080 | Total: 2200 x 1125 | Sync: 44+, 5+ | Start: 192, 41 | CEA RGB, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 6016 | Nvid: 32768 | Maud: 512 | Naud: 16875
METADATA | Pixel Clock: 148.350 MHz | DwnSp: on | HDCP-Sync: N | HDCP-Enc: off
```

4. Access the **RX Control and Configuration** dialog box to enable HDCP 2.2 on the DisplayPort Rx port. You access this dialog box through the **Tools** flyout menu (indicated by the arrow in the screen shot above).

   The **Rx Control and Configuration** dialog box appears as shown below.



Duration 100 ms (100 - 4000)

5. Select the HDCP tab and choose either 1.3 or 2.2. Then click on the **Refresh** button.

○ None ○ 1.3 ● 2.2

Key Type

● Production ○ Facsimile #1

Repeater

☑ Enabled

Depth 0

Device Count 0

```
HDCP2ENABLED    :YES
RTX             :2b 2c a6 4c 8c 75 10 d0
TXCAPS          :2 0 0
AKE_INIT        :RCVD_VALID
RX_CERT         :SND_VALID
STORED_KM       :NOT_RCVD
NO_STORED_KM    :RCVD_VALID
HPRIME          :SND_VALID
PAIRING         :SND_VALID
LC_INIT         :RCVD_VALID
LPRIME          :SND_VALID
SKE             :RCVD_VALID
AUTHENTICATED   :YES
REPAUTH_RCVIDLST:MSG_NOT_SND
RCVIDLST_ACK    :NOT_RCVD
STRM_MGMT       :NOT_RCVD
STRM_RDY        :MSG_NOT_SND
STRM_TYP        :0
```

Note: If you are testing a source device by emulating a repeater function you will have to enable the repeater using the **Repeater** enable checkbox and then enter in the depth and the downstream device count using the **Depth** and **Device Count** pop up menus.

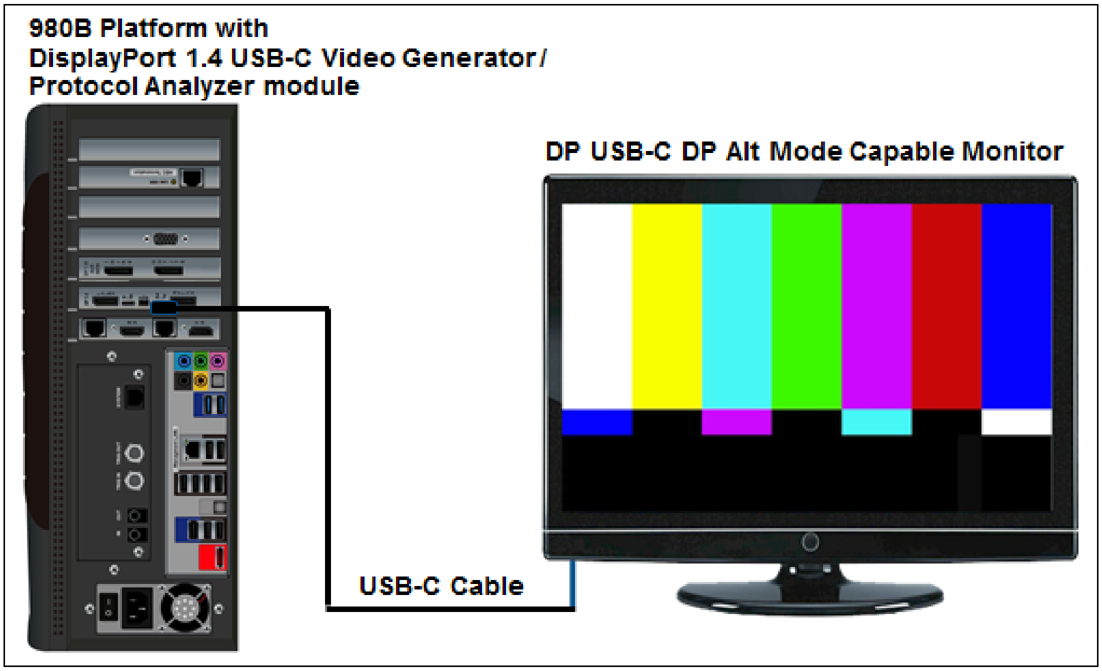
```
HDCP2ENABLED   :YES
RTX            :2b 2c a6 4c 8c 75 10 d0
TXCAPS         :2 0 0
AKE_INIT       :RCVD_VALID
RX_CERT        :SND_VALID
STORED_KM      :NOT_RCVD
NO_STORED_KM   :RCVD_VALID
HPRIME         :SND_VALID
    RING       :SND_VALID
    INIT       :RCVD_VALID
    IME        :SND_VALID
               :RCVD_VALID
    HENTICATED :YES
    AUTH_RCVIDLST:MSG_NOT_SND
    IDLST_ACK  :NOT_RCVD
    M_MGMT     :NOT_RCVD
    M_RDY      :MSG_NOT_SND
STRM_TYP       :0
```

4.2 Running an HDCP 2.2 Sink test

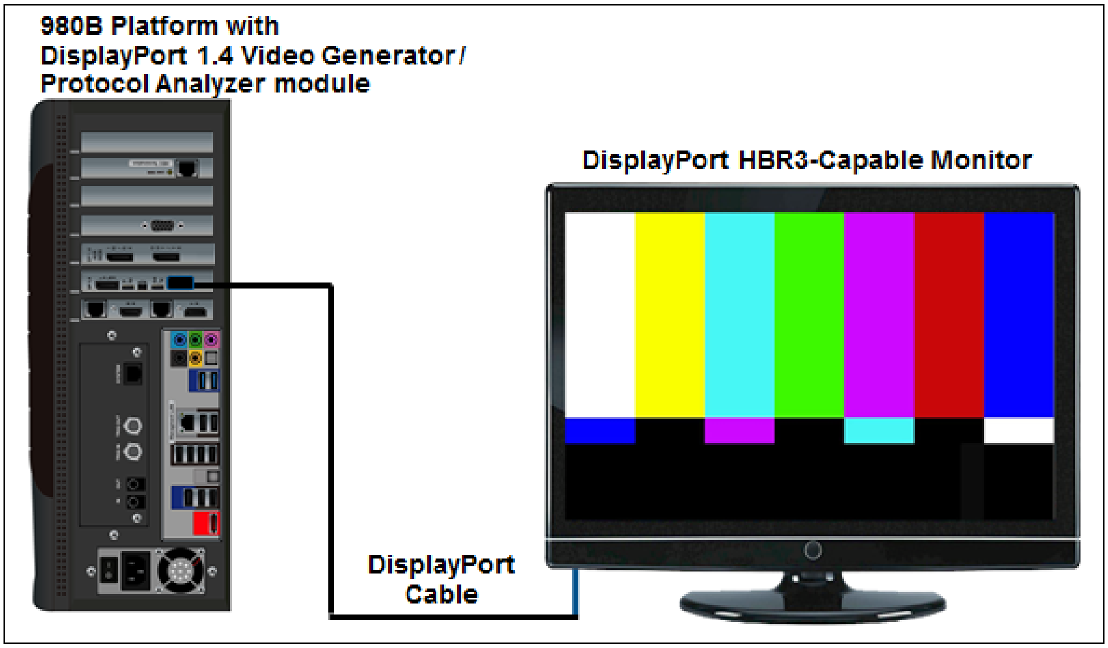
The procedures below describe how to run the HDCP 2.2 authentication on a DP 1.4 sink device. For testing DisplayPort display devices (sinks), the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module emulates an HDCP 2.2-capable DisplayPort source device. You can either verify the simple case with the module acting as a source to test a display or you can test the input of an HDCP 2.2-capable DisplayPort repeater device to verify its handling of downstream display devices. You can optionally view the HDCP 2.2 authentication transactions over the DDC using the Auxiliary Channel Analyzer (ACA) utility. Procedures for monitoring the HDCP 2.2 transactions through the ACA are in the next section.

To run the HDCP 2.2 authentication test on a sink:

1. Connect the DP sink device to one of the DP module's Tx Analyzer ports as shown below.



USB-C Connection



Standard DP Connection

2. Touch select the DP **Generator** icon on the **Card Control** page 1 of the **Apps** panel on the embedded 980 GUI Manager:

Note: The **Generator** window appear as shown below.

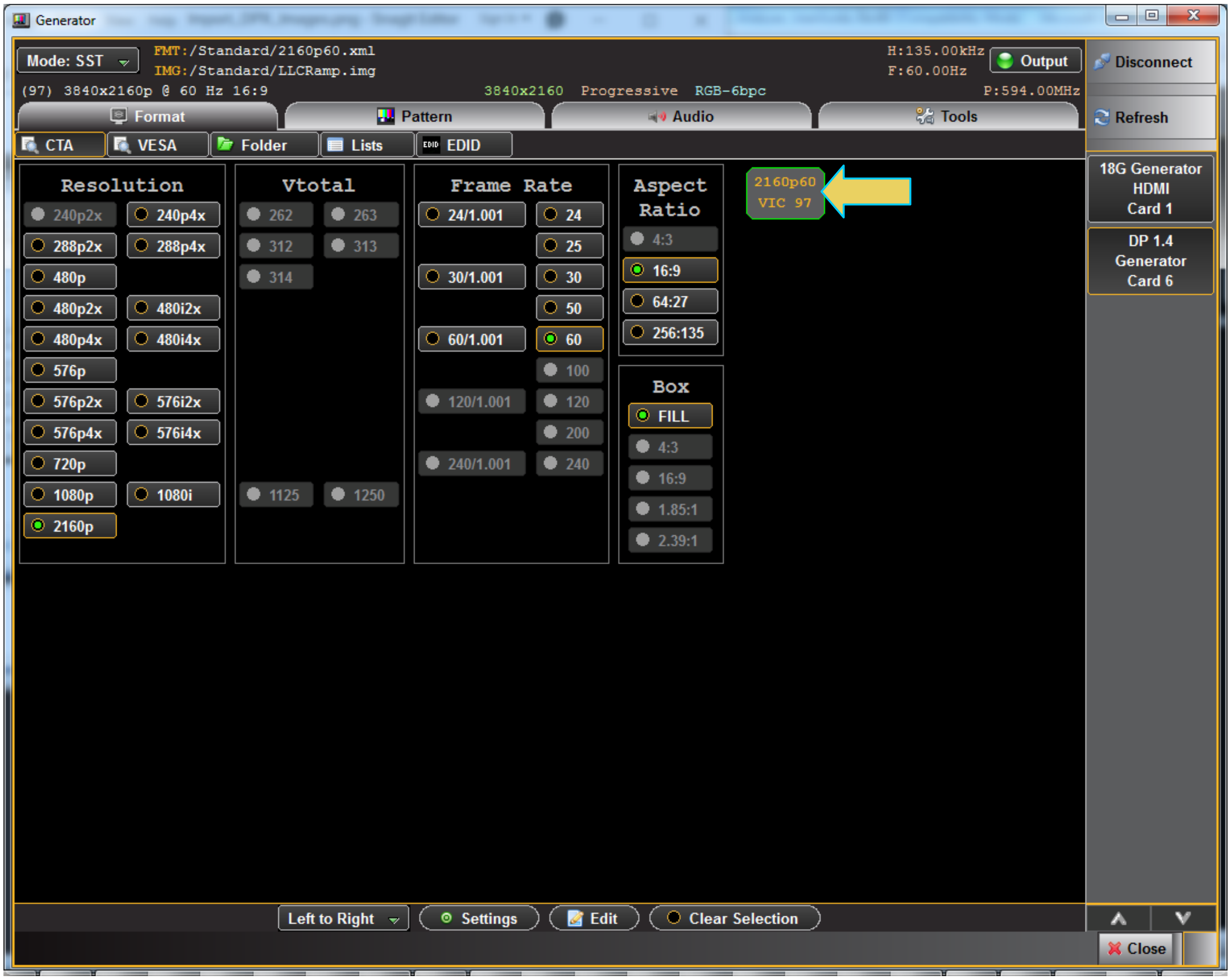
DHCP: 192.168.254.151 ATP Version: 4.14.19 (4 cards detected)

Note: The Generator window appears as shown below.

3. Select the **Format** tab. Make sure that the DisplayPort module is selected as the active card in the Generator window. Use the selection items on the right. Refer to the following screen example. In this case the DisplayPort module is in slot 3.

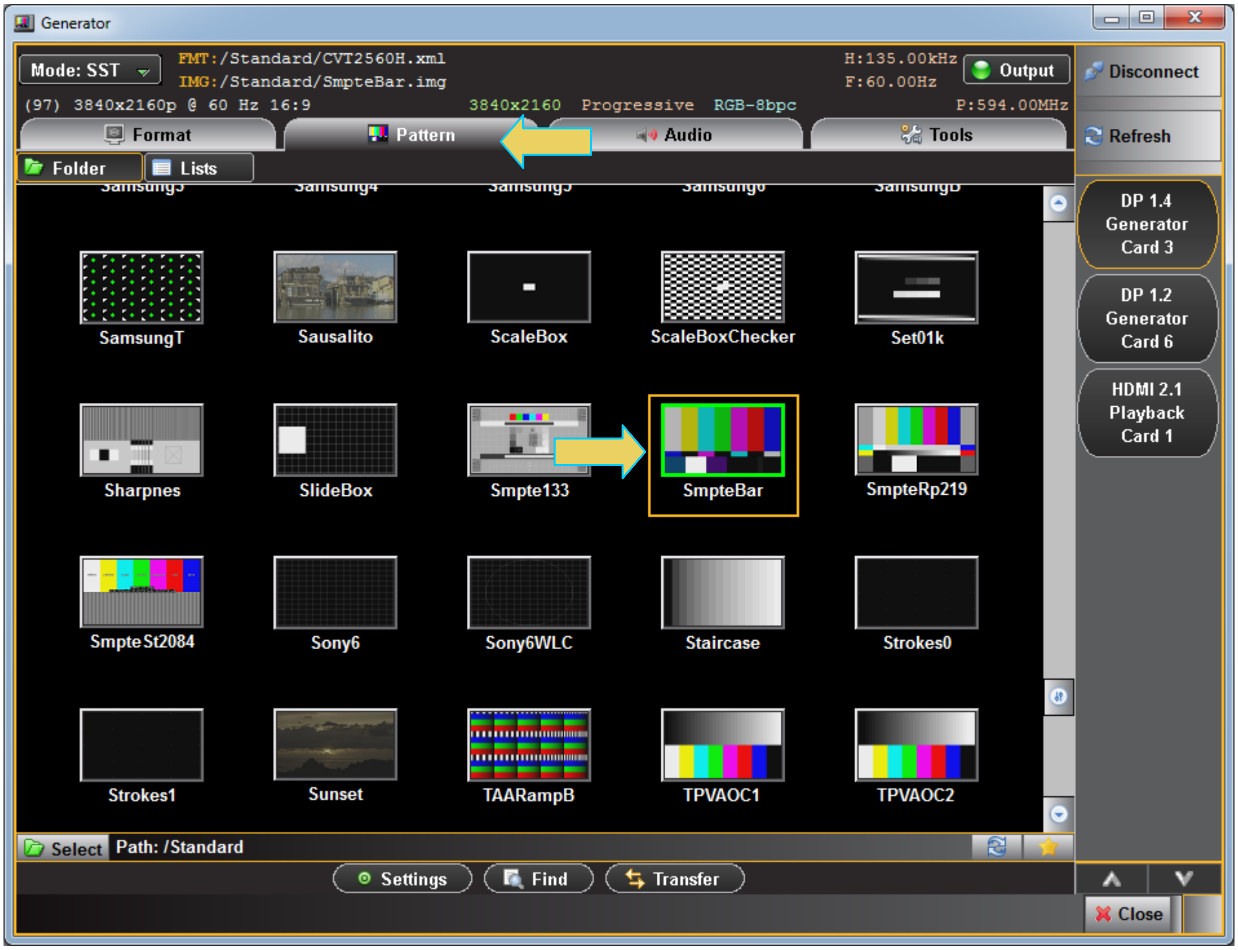
Mode: SST
FMT:1080p59.xml
IMG:/Standard/LLCRamp.img
(16) 1920x1080p @ 60 Hz 16:9
1920x1080 Progressive RGB-6bpc
H:67.43kHz
F:59.94Hz
P:148.35MHz

4. Select the video format timing using the **Format** tab shown below. The format timing does not matter for the HDCP 2.2 test.



```
Mode: SST      FMT:/Standard/2160p60.xml                          H:135.00kHz
               IMG:/Standard/LLCRamp.img                          F:60.00Hz
(97) 3840x2160p @ 60 Hz 16:9       3840x2160  Progressive  RGB-6bpc   P:594.00MHz
```

5. Select the video test pattern using the **Pattern** tab shown below (SMPTEBar shown in the example). It does not matter which test pattern you use when HDCP 2.2 testing.



Mode: SST
FMT:/Standard/CVT2560H.xml
IMG:/Standard/SmpteBar.img
H:135.00kHz
F:60.00Hz
(97) 3840x2160p @ 60 Hz 16:9
3840x2160 Progressive RGB-8bpc
P:594.00MHz
Path: /Standard

6. Select the **HDCP Test** button from **Tools** tab as shown below.

```
FMT:/Standard/CVT2560H.xml                H:135.00kHz
IMG:/Standard/SmpteBar.img                F:60.00Hz
(97) 3840x2160p @ 60 Hz 16:9   3840x2160  Progressive  RGB-8bpc   P:594.00MHz
```

HDCP Mode

○ None ○ 1.3 ● 2.2

Key Type

● Production ○ Facsimile #1

Status

```
HDCP2ENABLED   :YES
RXHDCP2ENABLED:YES
RCV ID         :0 0 0 0 0
RXCAPS         :0 0 0
AKE_INIT       :SND_VALID
RX_CERT        :RCVD_INVALID
STORED_KM      :NOT_RCVD
NO_STORED_KM   :NOT_RCVD
HPRIME         :NOT_RCVD
PAIRING        :NOT_RCVD
LC_INIT        :NOT_RCVD
LPRIME         :NOT_RCVD
SKE            :NOT_RCVD
AUTHENTICATED  :NO
REPAUTH_RCVIDLST:NOT_RCVD
RCVIDLST_ACK   :MSG_NOT_SND
STRM_MGMT      :MSG_NOT_SND
STRM_RDY       :NOT_RCVD
STRM_TYP       :0
DEPTH          :0
DEV_COUNT      :0
```

7. Enable HDCP 2.2 authentication using the **HDCP Mode Enable** radio button as shown below. Note that status is shown in the tab below the control buttons but you need to hit the **Refresh** button.

```
FMT:1080p59.xml                                                    H:67.43kHz
IMG:/Standard/SmpteBar.img                                         F:59.94Hz
(16) 1920x1080p @ 60 Hz 16:9     1920x1080  Progressive  RGB-6bpc  P:148.35MHz
```

HDCP Mode

○ None ○ 1.3 ● 2.2

Key Type

● Production ○ Facsimile #1

Status

Refresh

```
HDCP2ENABLED   :YES
RXHDCP2ENABLED:YES
RCV ID         :e1 bc 68 5c 47
RXCAPS         :2 0 2
AKE_INIT       :SND_VALID
RX_CERT        :RCVD_VALID
STORED_KM      :NOT_RCVD
NO_STORED_KM   :SND_VALID
HPRIME         :RCVD_VALID
PAIRING        :RCVD_VALID
LC_INIT        :SND_VALID
LPRIME         :RCVD_VALID
SKE            :SND_VALID
AUTHENTICATED  :YES
REPAUTH_RCVIDLST:NOT_RCVD
RCVIDLST_ACK   :MSG_NOT_SND
STRM_MGMT      :MSG_NOT_SND
STRM_RDY       :NOT_RCVD
STRM_TYP       :0
DEPTH          :0
DEV_COUNT      :0
```

8. Disable HDCP when done testing. Refer to the screen example below.

HDCP Mode

○ None ○ 1.3 ● 2.2

Key Type

● Production ○ Facsimile #1

Status

Refresh

```
HDCP2ENABLED    :YES
RXHDCP2ENABLED:YES
RCV ID          :0 0 0 0 0
RXCAPS          :0 0 0
AKE_INIT        :SND_VALID
RX_CERT         :RCVD_INVALID
STORED_KM       :NOT_RCVD
NO_STORED_KM    :NOT_RCVD
HPRIME          :NOT_RCVD
PAIRING         :NOT_RCVD
LC_INIT         :NOT_RCVD
LPRIME          :NOT_RCVD
SKE             :NOT_RCVD
AUTHENTICATED :NO
REPAUTH_RCVIDLST:NOT_RCVD
RCVIDLST_ACK    :MSG_NOT_SND
STRM_MGMT       :MSG_NOT_SND
STRM_RDY        :NOT_RCVD
STRM_TYP        :0
DEPTH           :0
DEV_COUNT       :0
```

4.3 Viewing the HDCP 2.2 authentication transaction using the Auxiliary Channel Analyzer (ACA) utility

The following procedures describe how to view the HDCP 2.2 authentication transactions over the DisplayPort Aux Channel using the Auxiliary Channel Analyzer (ACA) utility. You can view the HDCP 2.2 authentication transactions either while testing a DP HDCP 2.2 source or sink; the general operation is the same. The following example describes how to view the transactions with the 980 DP module emulating an HDCP 2.2 Receiver.

Note: For detailed operating instructions on the ACA utility please refer to Auxiliary Channel Analyzer (ACA) Utilities.

5 DP Link Training Control

The 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module enables you to control the link training with a DisplayPort sink device. There are two modes: 1) Adaptive Training and 2) Non Adaptive training.

Adaptive Training enables you to train based on Lane Count and Link Rates capabilities that you define in the application. When you set the Lane Count and Link Rate in the Adaptive training mode you are emulating a DP source with those capabilities. The link will be established with the appropriate voltage swing level and pre-emphasis necessary to establish a proper link.

In the Non-Adaptive mode, you are forcing the Lane Count and Link Rate as well as the voltage swing level and pre-emphasis and bypassing the typical link training function.

Note: You can monitor the link training transactions with the Auxiliary Channel Analyzer (ACA) if desired.

5.1 Accessing the Link Training Control application

Use the following procedure to test link training with your DP display device. This procedure assumes that you have already selected a DP VESA format and a test pattern to meet your test application requirements.

1. Access the **Link Train** control application through the **Tools** tab on the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module interface as shown below.

FMT:1080p59.xml
IMG:/Standard/Master.img
(16) 1920x1080p @ 60 Hz 16:9
1920x1080 Progressive RGB-6bpc
H:67.43kHz
F:59.94Hz
P:148.35MHz

Current Status
Main Stream: Enabled
Lane Count: 2 Lanes
Link Rate: 8.10 Gbps per Lane
Lane 1: CR done, EQ done, SLock done [v0, p0]
Lane 2: CR done, EQ done, SLock done [v0, p0]
Lane 3: --
Lane 4: --
Inter-lane Alignment: Yes

Lane Count: ○ 1 ● 2 ○ 4
Link Rate (Gbps): ○ 1.62 ○ 2.70 ○ 5.40 ● 8.10
Voltage Swing Level: ● 0 ○ 1 ○ 2 ○ 3
Pre-emphasis Level: ● 0 ○ 1 ○ 2 ○ 3
☐ Disable Retries

2. Select the link training mode tab (Adaptive or Non-Adapative) in accordance with your requirements. Adaptive selection shown in the screen below.

Mode: SST

FMT:/Standard/2160p60.xml
IMG:/Standard/Master.img
(97) 3840x2160p @ 60 Hz 16:9
3840x2160 Progressive RGB-8bpc
H:135.00kHz
F:60.00Hz
P:594.00MHz

Current Status

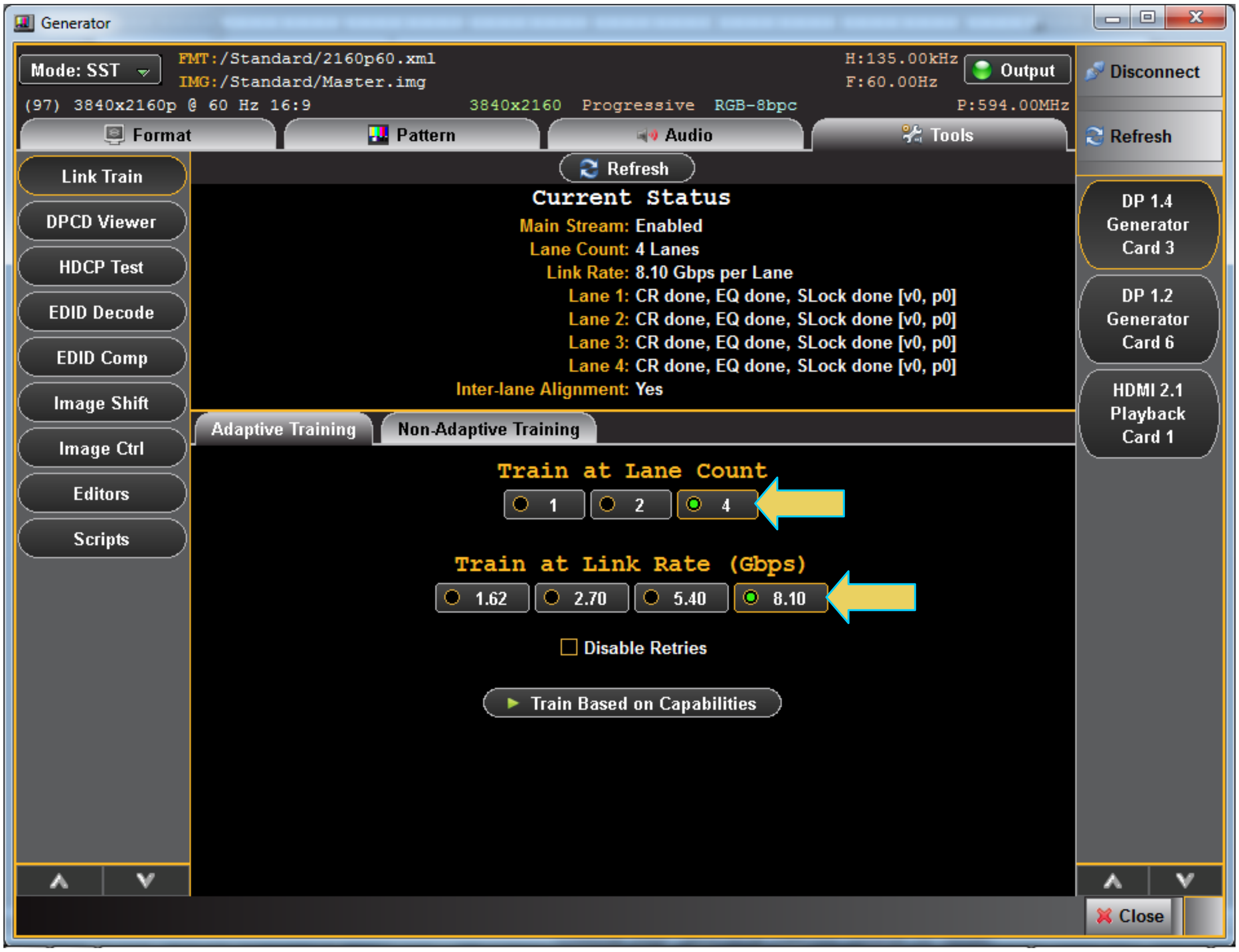
Main Stream: Enabled
Lane Count: 4 Lanes
Link Rate: 8.10 Gbps per Lane
Lane 1: CR done, EQ done, SLock done [v0, p0]
Lane 2: CR done, EQ done, SLock done [v0, p0]
Lane 3: CR done, EQ done, SLock done [v0, p0]
Lane 4: CR done, EQ done, SLock done [v0, p0]
Inter-lane Alignment: Yes

Train at Lane Count
○ 1 ○ 2 ● 4

Train at Link Rate (Gbps)
○ 1.62 ○ 2.70 ○ 5.40 ● 8.10

☐ Disable Retries

3. Select the **Train at Lane Count** and **Train at Link Rate** parameters using the radio buttons provided (4 lanes and 8.1Gbps link rate shown in the example below).



```
FMT:/Standard/2160p60.xml                         H:135.00kHz
IMG:/Standard/Master.img                          F:60.00Hz
(97) 3840x2160p @ 60 Hz 16:9   3840x2160  Progressive  RGB-8bpc   P:594.00MHz
```

```
Current Status
Main Stream: Enabled
Lane Count: 4 Lanes
Link Rate: 8.10 Gbps per Lane
Lane 1: CR done, EQ done, SLock done [v0, p0]
Lane 2: CR done, EQ done, SLock done [v0, p0]
Lane 3: CR done, EQ done, SLock done [v0, p0]
Lane 4: CR done, EQ done, SLock done [v0, p0]
Inter-lane Alignment: Yes
```

Train at Lane Count: ○ 1 ○ 2 ● 4

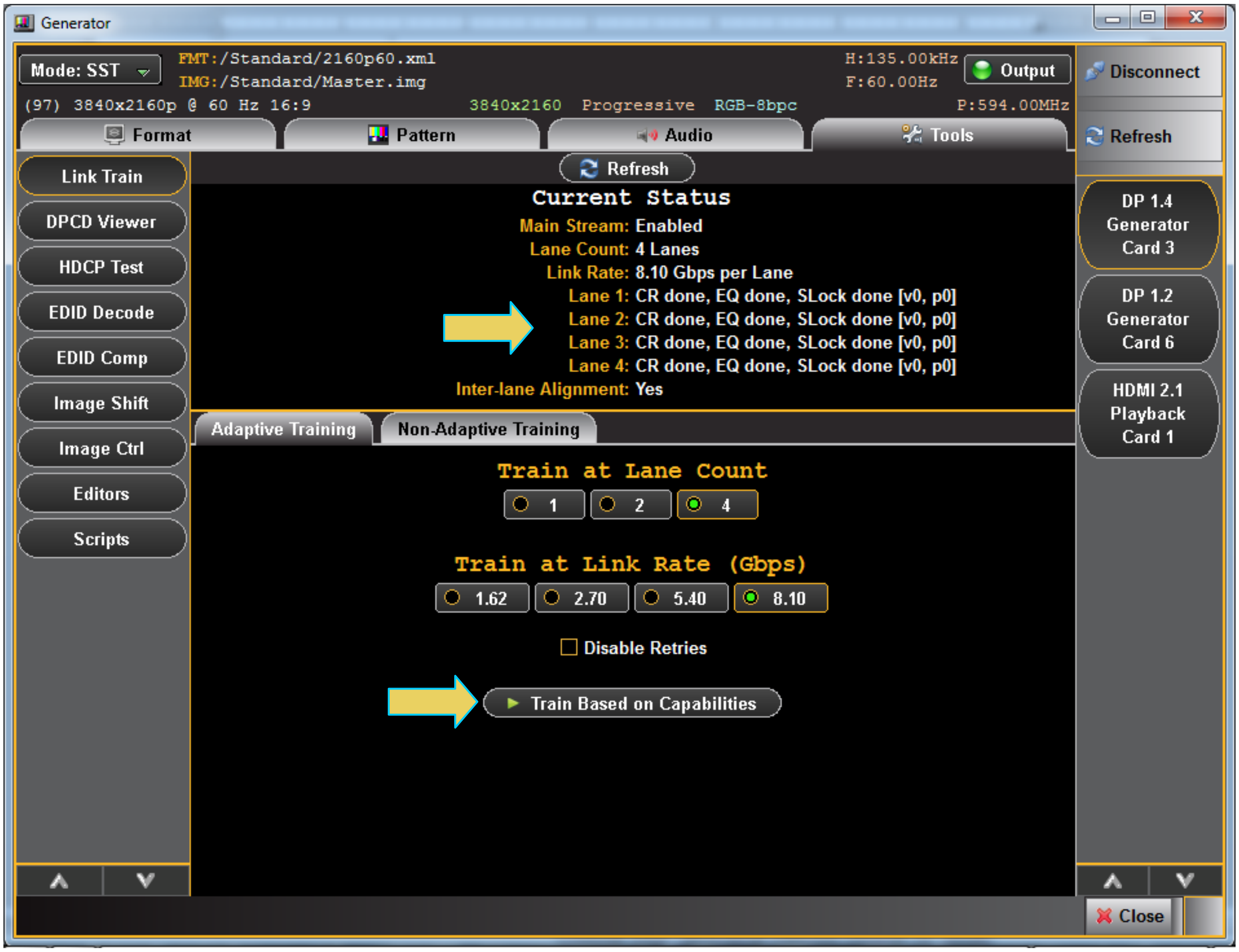
Train at Link Rate (Gbps): ○ 1.62 ○ 2.70 ○ 5.40 ● 8.10

☐ Disable Retries

4. Click on the **Train Based on Capabilities** activation button to initiate the link training.

   The results and status of the link training will be shown on the Link Train application screen as shown below.

   Note: You can monitor the link training transactions with the Auxiliary Channel Analyzer (ACA) if desired.



FMT:/Standard/2160p60.xml
IMG:/Standard/Master.img
(97) 3840x2160p @ 60 Hz 16:9
3840x2160 Progressive RGB-8bpc
H:135.00kHz
F:60.00Hz
P:594.00MHz

Current Status

Main Stream: Enabled
Lane Count: 4 Lanes
Link Rate: 8.10 Gbps per Lane
Lane 1: CR done, EQ done, SLock done [v0, p0]
Lane 2: CR done, EQ done, SLock done [v0, p0]
Lane 3: CR done, EQ done, SLock done [v0, p0]
Lane 4: CR done, EQ done, SLock done [v0, p0]
Inter-lane Alignment: Yes

Train at Lane Count

○ 1 ○ 2 ● 4

Train at Link Rate (Gbps)

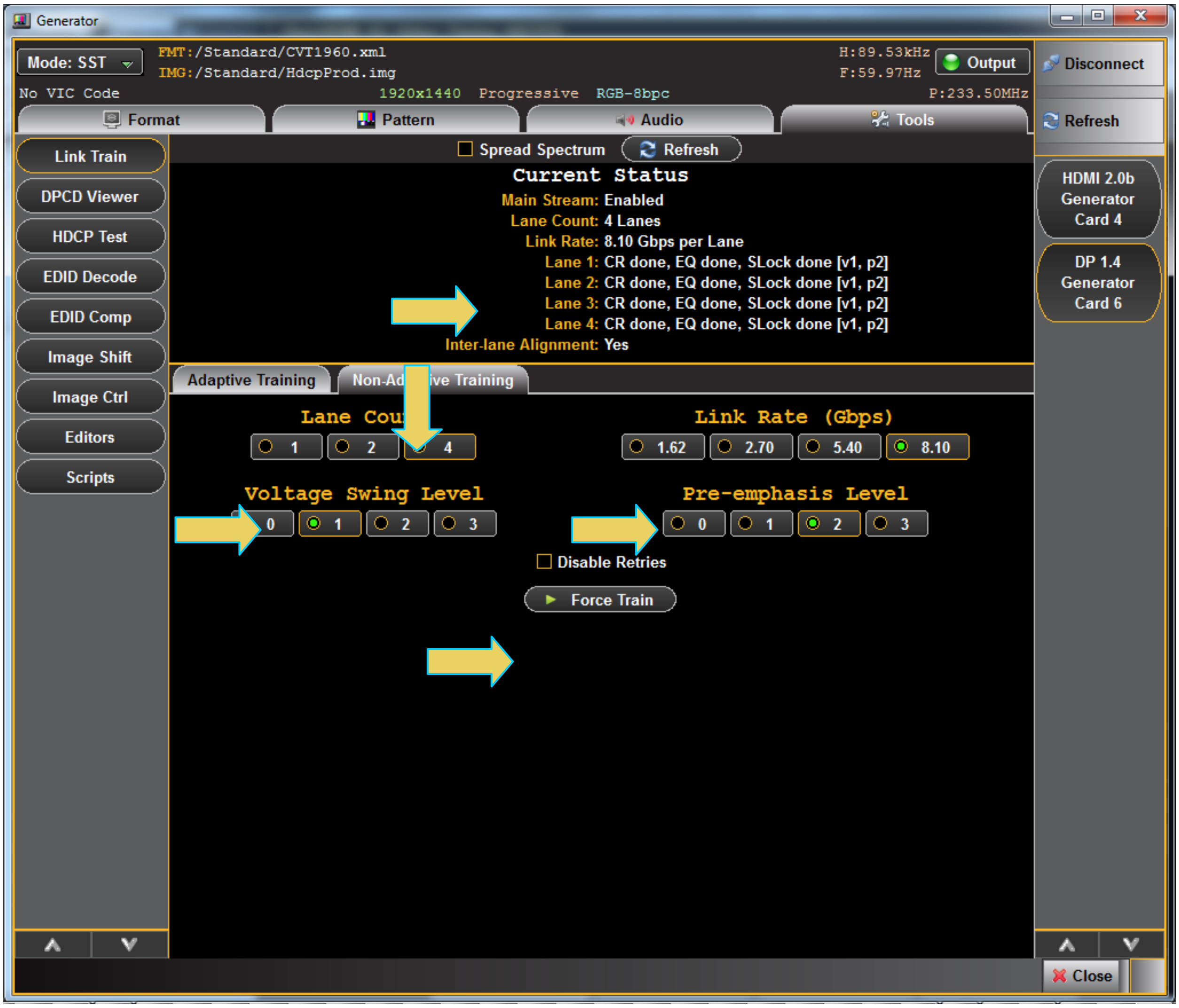
○ 1.62 ○ 2.70 ○ 5.40 ● 8.10

☐ Disable Retries

5. Optionally, select the **Non-Adapative** link training mode using the tab provided.
6. Specify the **Lane Count**, **Link Rate**, **Voltage Swing Level** and **Pre-emphasis** level parameters.
7. Click on the **Force Train** activation button to initiate the link establishment using the parameters you have specified.

   Note: You can monitor the link training transactions with the Auxiliary Channel Analyzer (ACA) if desired.

   A few examples are shown below with various settings and the resulting status.



```
FMT:/Standard/CVT1960.xml                                   H:89.53kHz
IMG:/Standard/HdcpProd.img                                  F:59.97Hz
No VIC Code          1920x1440  Progressive  RGB-8bpc       P:233.50MHz
```

Current Status

Main Stream: Enabled
Lane Count: 4 Lanes
Link Rate: 8.10 Gbps per Lane
Lane 1: CR done, EQ done, SLock done [v1, p2]
Lane 2: CR done, EQ done, SLock done [v1, p2]
Lane 3: CR done, EQ done, SLock done [v1, p2]
Lane 4: CR done, EQ done, SLock done [v1, p2]
Inter-lane Alignment: Yes

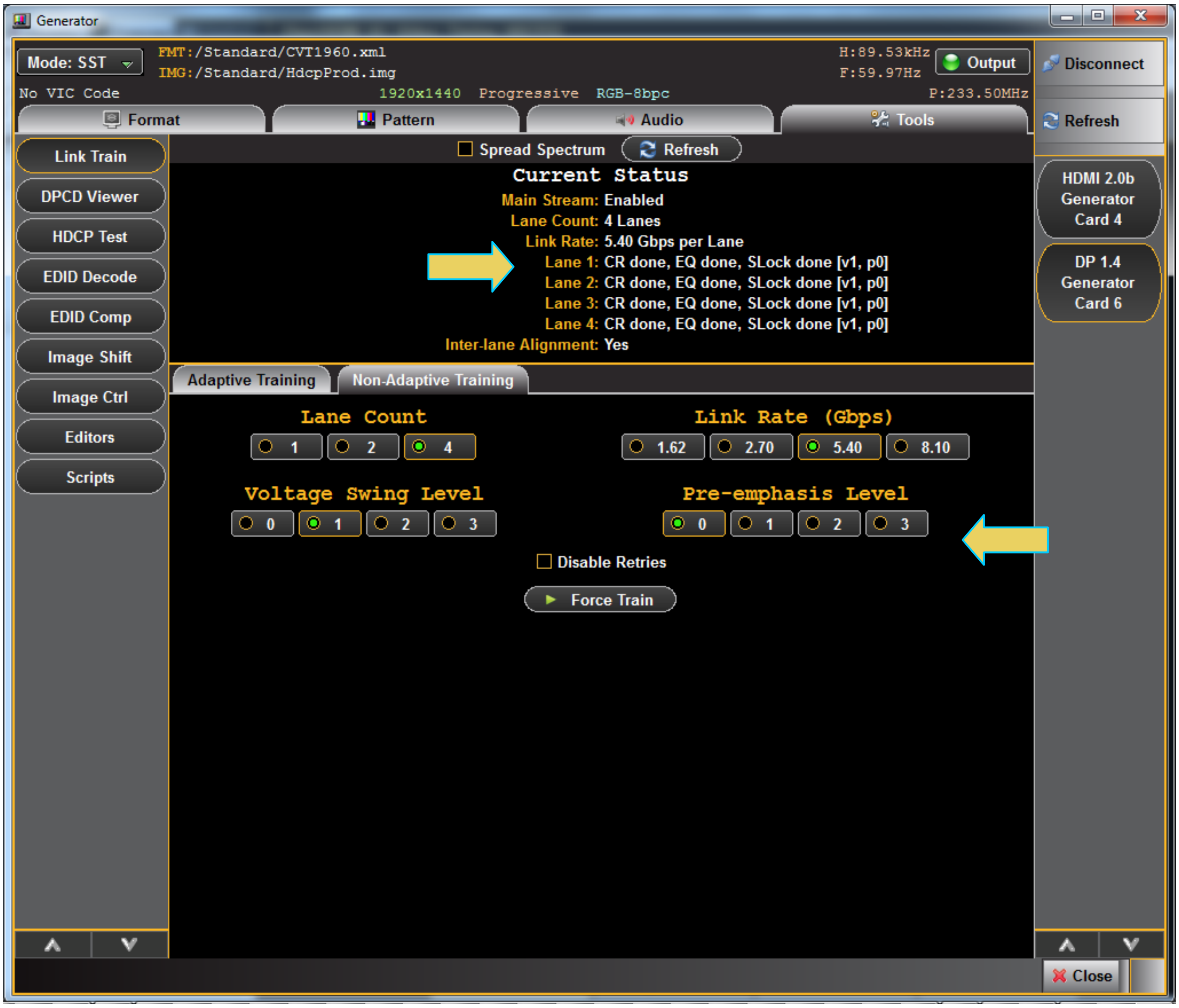
Lane Count: ○ 1 ○ 2 ○ 4

Link Rate (Gbps): ○ 1.62 ○ 2.70 ○ 5.40 ● 8.10

Voltage Swing Level: ○ 0 ● 1 ○ 2 ○ 3

Pre-emphasis Level: ○ 0 ○ 1 ● 2 ○ 3

☐ Disable Retries



FMT:/Standard/CVT1960.xml
IMG:/Standard/HdcpProd.img
H:89.53kHz
F:59.97Hz
No VIC Code
1920x1440 Progressive RGB-8bpc
P:233.50MHz

☐ Spread Spectrum

Current Status

Main Stream: Enabled
Lane Count: 4 Lanes
Link Rate: 5.40 Gbps per Lane
Lane 1: CR done, EQ done, SLock done [v1, p0]
Lane 2: CR done, EQ done, SLock done [v1, p0]
Lane 3: CR done, EQ done, SLock done [v1, p0]
Lane 4: CR done, EQ done, SLock done [v1, p0]
Inter-lane Alignment: Yes

Lane Count
○ 1 ○ 2 ● 4

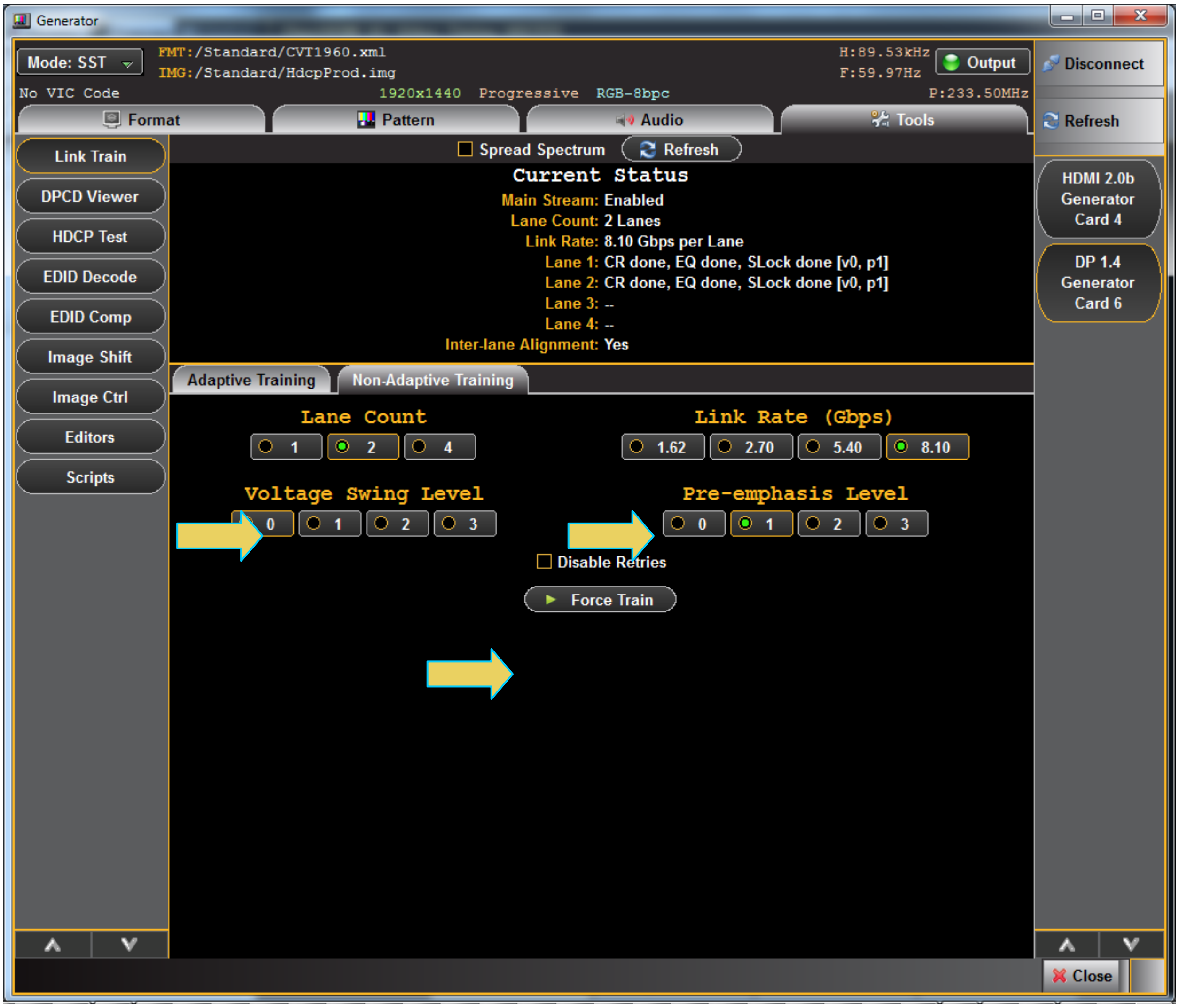
Link Rate (Gbps)
○ 1.62 ○ 2.70 ● 5.40 ○ 8.10

Voltage Swing Level
○ 0 ● 1 ○ 2 ○ 3

Pre-emphasis Level
● 0 ○ 1 ○ 2 ○ 3

☐ Disable Retries

A second example with 2 lanes at 8.1Gb/s:



FMT:/Standard/CVT1960.xml
IMG:/Standard/HdcpProd.img
H:89.53kHz
F:59.97Hz
No VIC Code
1920x1440 Progressive RGB-8bpc
P:233.50MHz

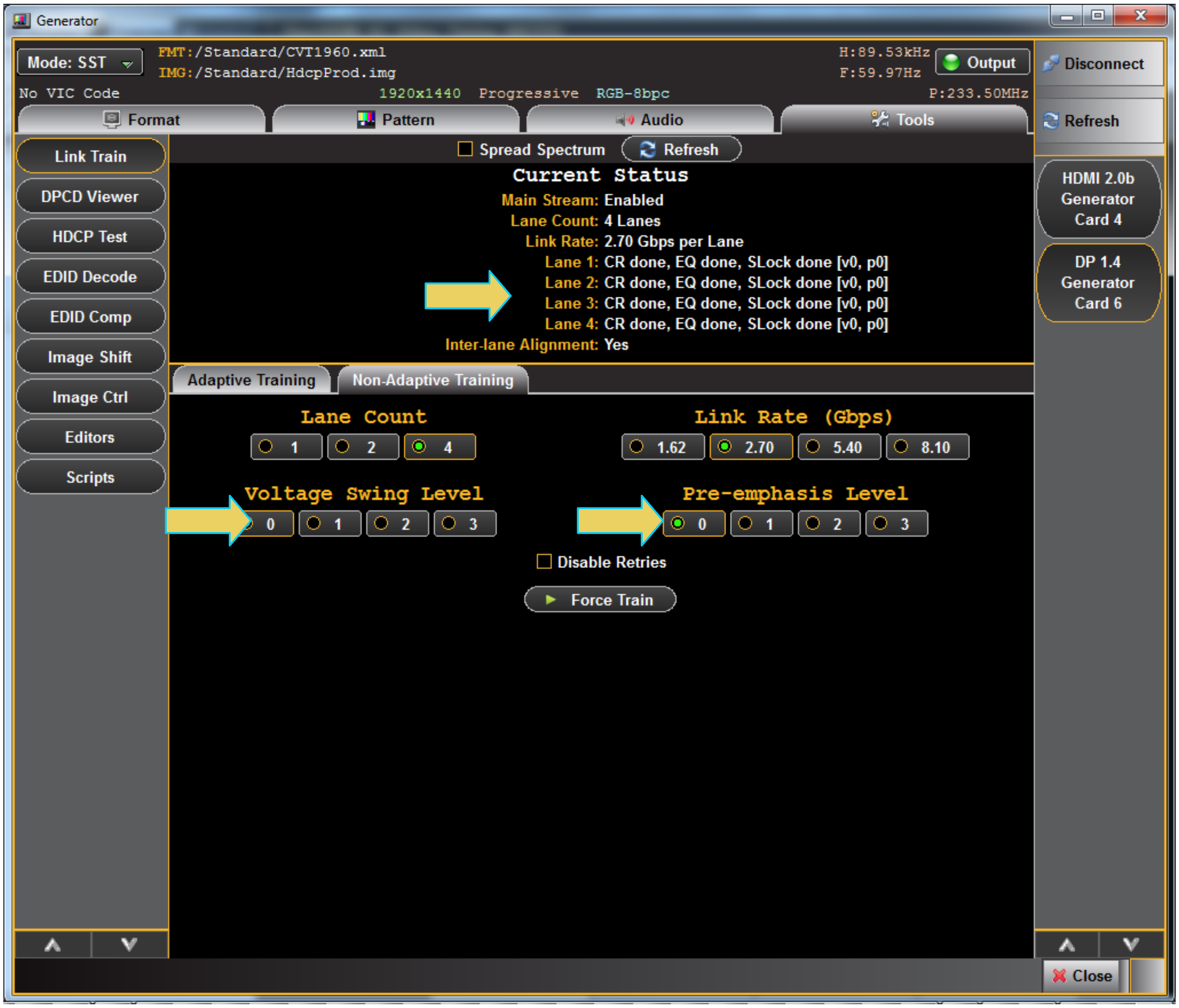
☐ Spread Spectrum

Current Status

Main Stream: Enabled
Lane Count: 2 Lanes
Link Rate: 8.10 Gbps per Lane
Lane 1: CR done, EQ done, SLock done [v0, p1]
Lane 2: CR done, EQ done, SLock done [v0, p1]
Lane 3: --
Lane 4: --
Inter-lane Alignment: Yes

Lane Count: ○ 1 ● 2 ○ 4
Link Rate (Gbps): ○ 1.62 ○ 2.70 ○ 5.40 ● 8.10
Voltage Swing Level: ○ 0 ○ 1 ○ 2 ○ 3
Pre-emphasis Level: ○ 0 ● 1 ○ 2 ○ 3
☐ Disable Retries

The result of the above configuration after forcing link training:



Current Status

Main Stream: Enabled
Lane Count: 4 Lanes
Link Rate: 2.70 Gbps per Lane
Lane 1: CR done, EQ done, SLock done [v0, p0]
Lane 2: CR done, EQ done, SLock done [v0, p0]
Lane 3: CR done, EQ done, SLock done [v0, p0]
Lane 4: CR done, EQ done, SLock done [v0, p0]
Inter-lane Alignment: Yes

Lane Count: ○ 1 ○ 2 ● 4

Link Rate (Gbps): ○ 1.62 ● 2.70 ○ 5.40 ○ 8.10

Voltage Swing Level: ○ 0 ○ 1 ○ 2 ○ 3

Pre-emphasis Level: ● 0 ○ 1 ○ 2 ○ 3

☐ Disable Retries

6 DP Multi-Stream Transport (MST) Testing

The 980 DP Video Generator / Analyzer module emulates an MST source for testing an MST branch device or MST-capable monitor. Up to four (4) streams are supported depending on bandwidth (resolutions) with a depth of one. You can configure the MST topology using a graphical interface. The optional Auxiliary Channel Analyzer (ACA) utility depicts the MST negotiations with the connected MST Rx device.

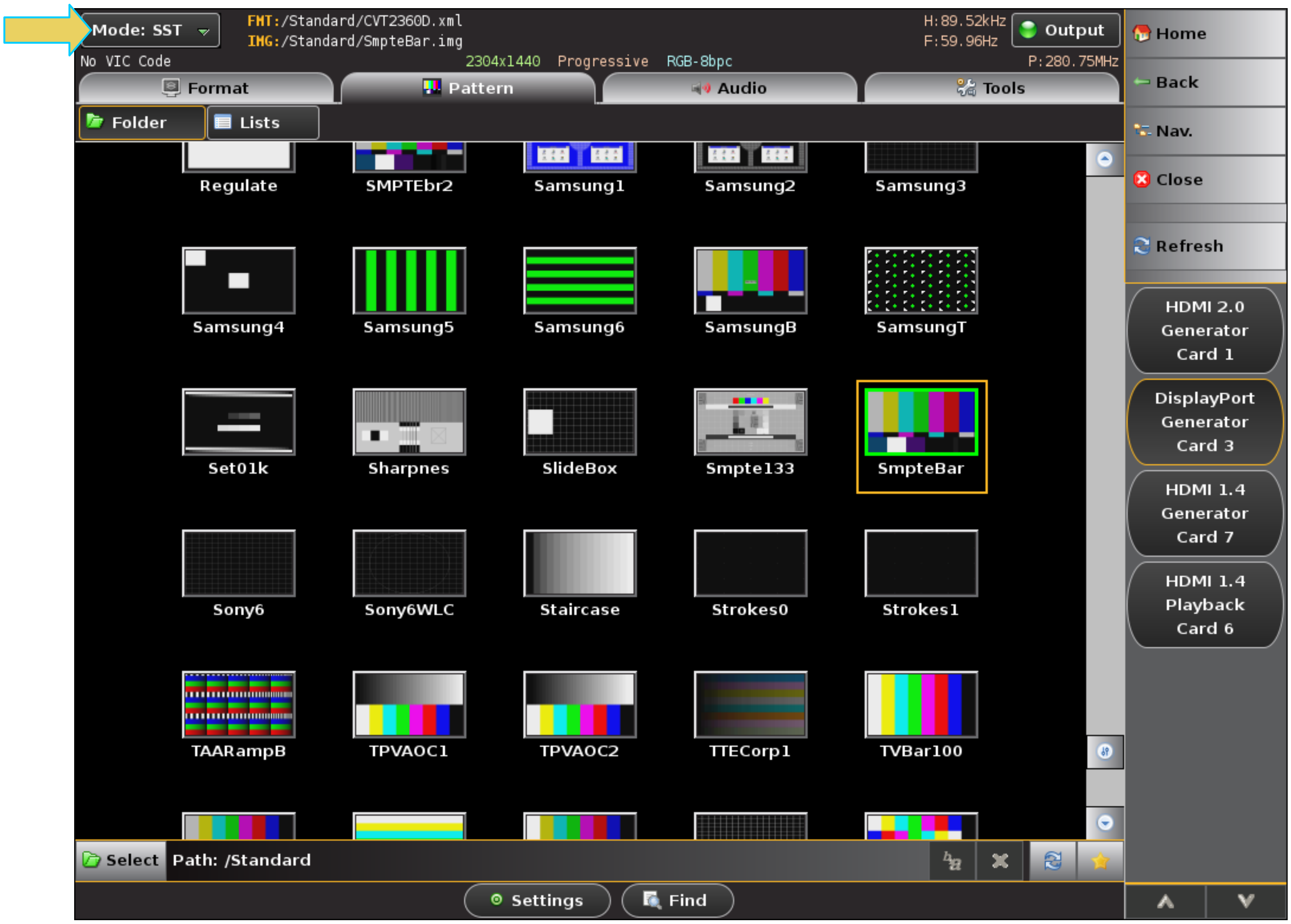
When MST is configured, the same video pattern and audio signal is transmitted to all downstream nodes. There is a number indicator that appears on the upper left screen of the downstream MST sink that identifies which stream is being delivered.

Note: MST testing is supported through both the standard DP port and the USB-C DP alt mode port.

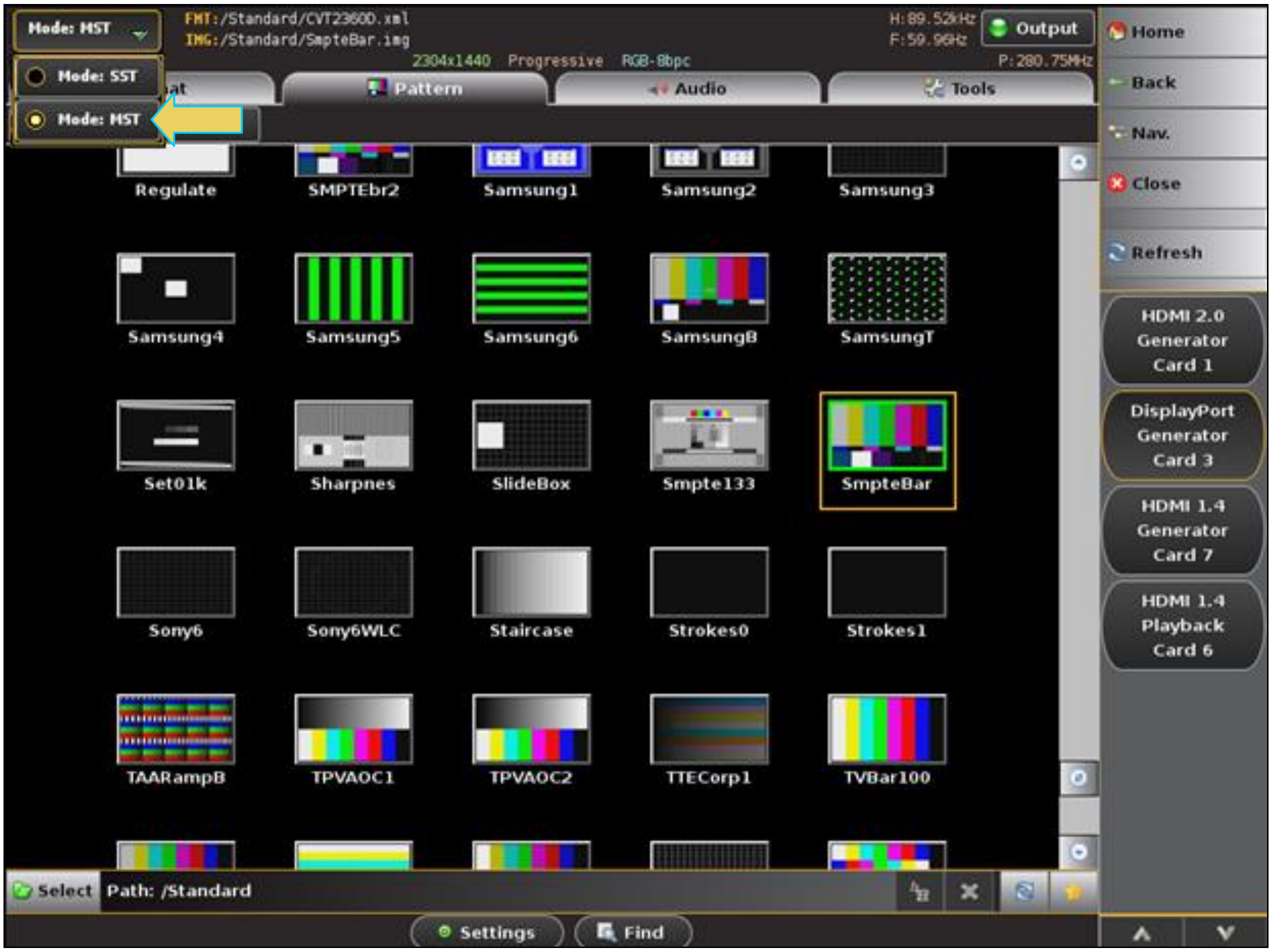
6.1 Accessing the MST Topology window

Use the following procedure to test MST on a connected MST-Capable sink device.

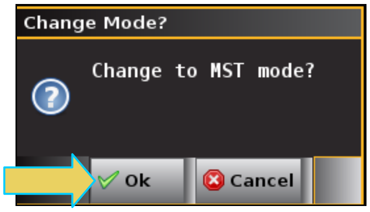
1. At the Generator dialog box, select MST from the Interface drop down menu. Refer to the screen example below.



Mode: SST
FMT:/Standard/CVT2360D.xml
IMG:/Standard/SmpteBar.img
No VIC Code
2304x1440 Progressive RGB-8bpc
H:89.52kHz
F:59.96Hz
P:280.75MHz
Path: /Standard

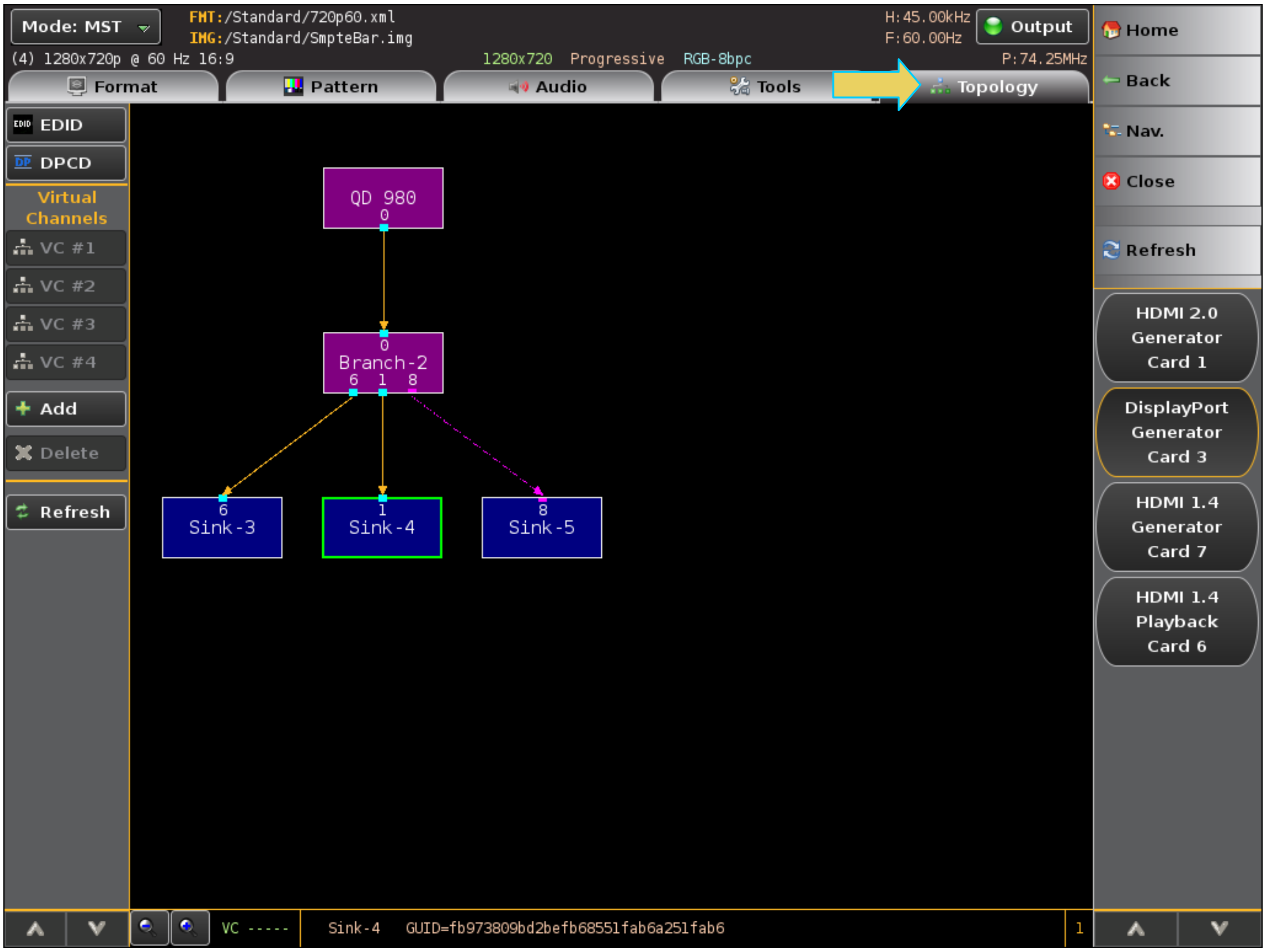


The following confirmation dialog box appears:



Click OK.

2. From the Generator window, access the **Topology** tab to control the MST application as shown below.



3. Access the **Topology** control application through the **Tools** tab on the 980 DP Video Generator module interface as shown below.

   The table below summarizes the graphical controls of the MST Topology window.

MST Topology Window	
Button	**Description**
EDID	Enables you to read the EDID of the selected downstream MST Rx node. **Note**: This activation button is not currently functional. To read the EDID of a downstream MST node, you must use the EDID read in the **Tools** menu.
DPCD	Enables you to read the DPCD of the selected downstream MST Rx node. **Note**: This activation button is not currently functional. To read the DPCD of a downstream MST node, you must use the DPCD read in the **Tools** menu.
Virtual Channels **VC #1…VC #4**	This capability is future.
Add	Enables you to add a downstream MST Rx node.
Delete	Enables you to delete a downstream MST Rx node.

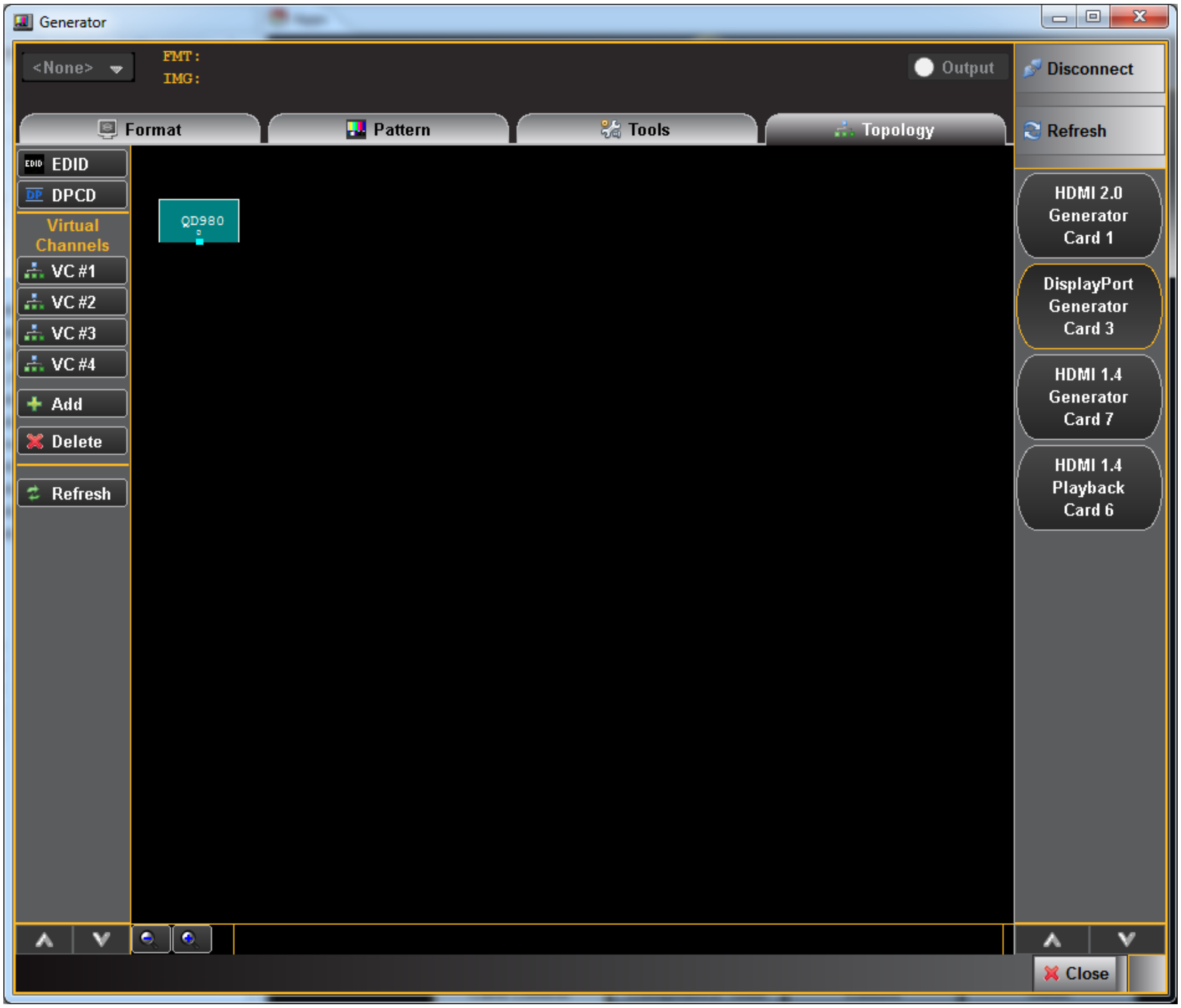
MST Topology Window	
Button	**Description**
Refresh	Refreshes the view.

6.2 Configuring the number of downstream MST nodes.

Use the following procedure to configure the number of downstream MST nodes.

To add an MST node(s):

1. Click on the **Add** + Add activation button on the left to add an MST node. The downstream nodes are shown in blue. Click Refresh if necessary. Refer to the screen example below.



Note: The **VC #x** buttons and the **EDID** and **DPCD** activation buttons are not currently functional.

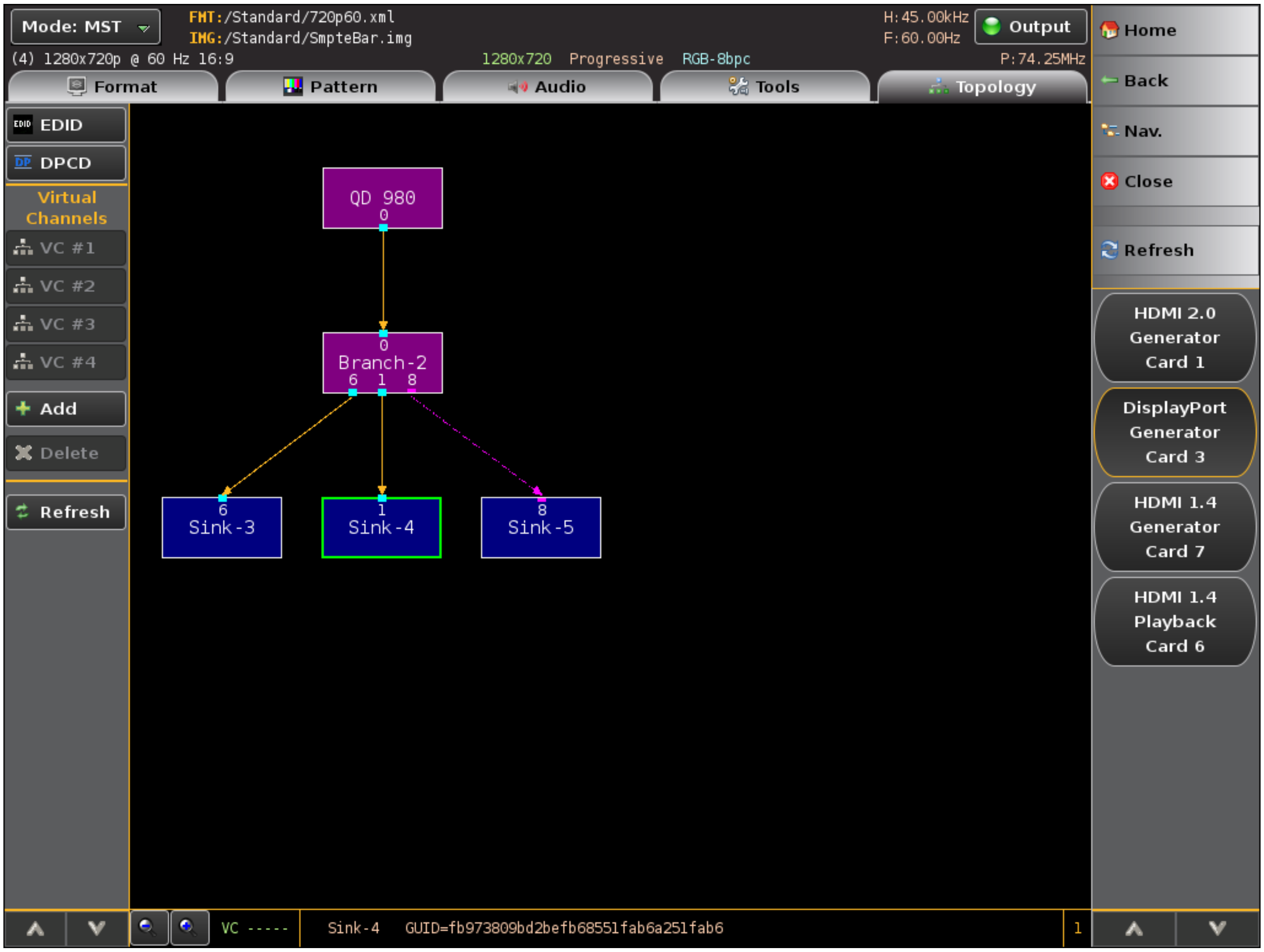
The following dialog box appears enabling you to select the number of downstream MST nodes (Virtual Channels).

Add a Virtual Channel

Virtual Channel #: ● VC #1 ○ VC #2 ○ VC #3 ○ VC #4

RAD:

The topology appears as shown below.



Mode: MST

FMT:/Standard/720p60.xml

IMG:/Standard/SmpteBar.img

(4) 1280x720p @ 60 Hz 16:9

1280x720 Progressive RGB-8bpc

H:45.00kHz

F:60.00Hz

P:74.25MHz

VC ----- Sink-4 GUID=fb973809bd2befb68551fab6a251fab6 1

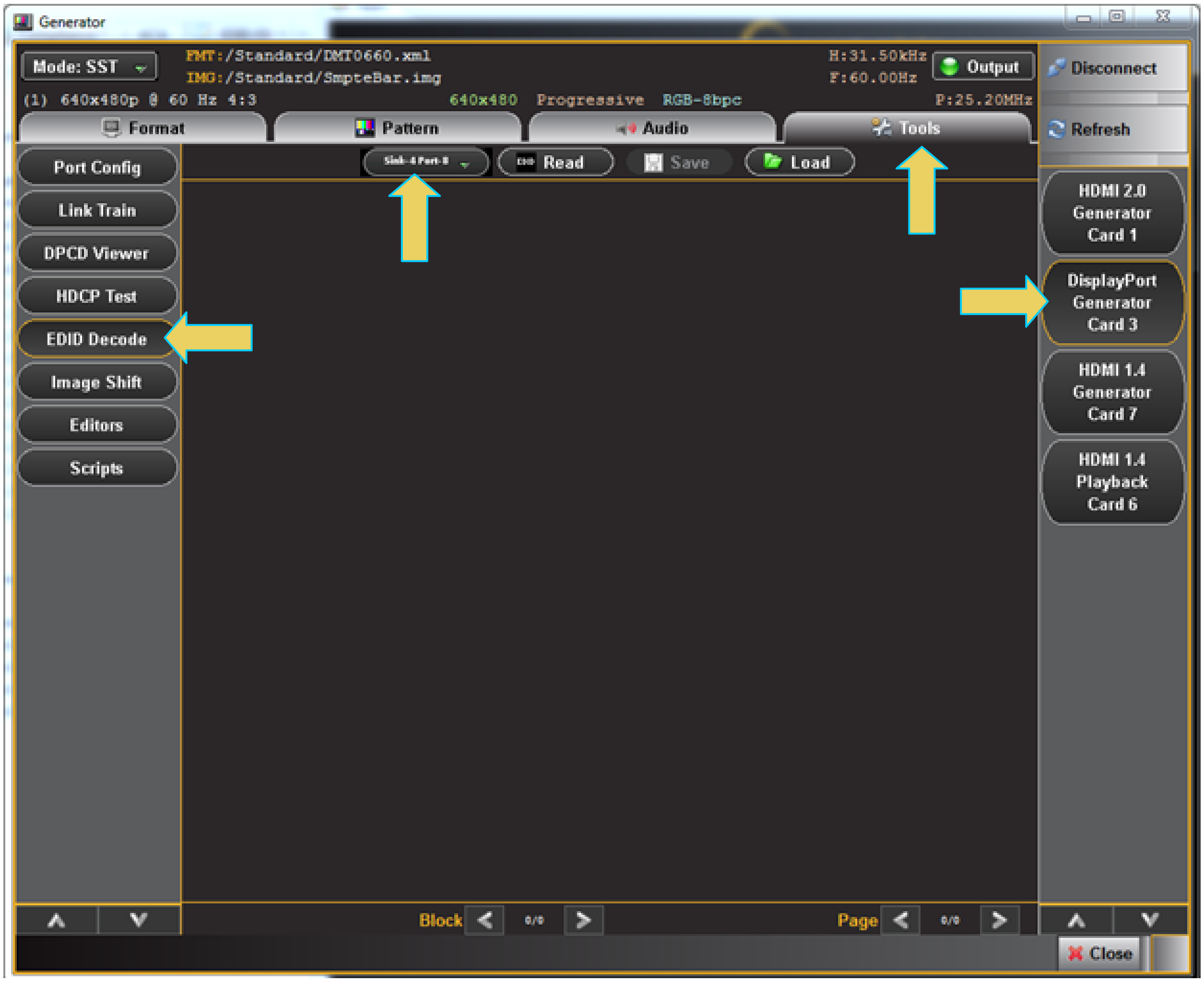
2. Click on the **Delete** ✖ Delete activation button on the left to delete an MST node. Click Refresh if necessary. Refer to the screen example above. A confirmation dialog box will appear. Click OK.

6.3 Reading the EDID of a downstream MST node.

Use the following procedures to read the EDID of any downstream MST Rx node. Currently the EDID button shown on the left panel of the **Topology** window is not functional. To read the EDID of a downstream not you have to use the EDID read function in the **Tools** menu.

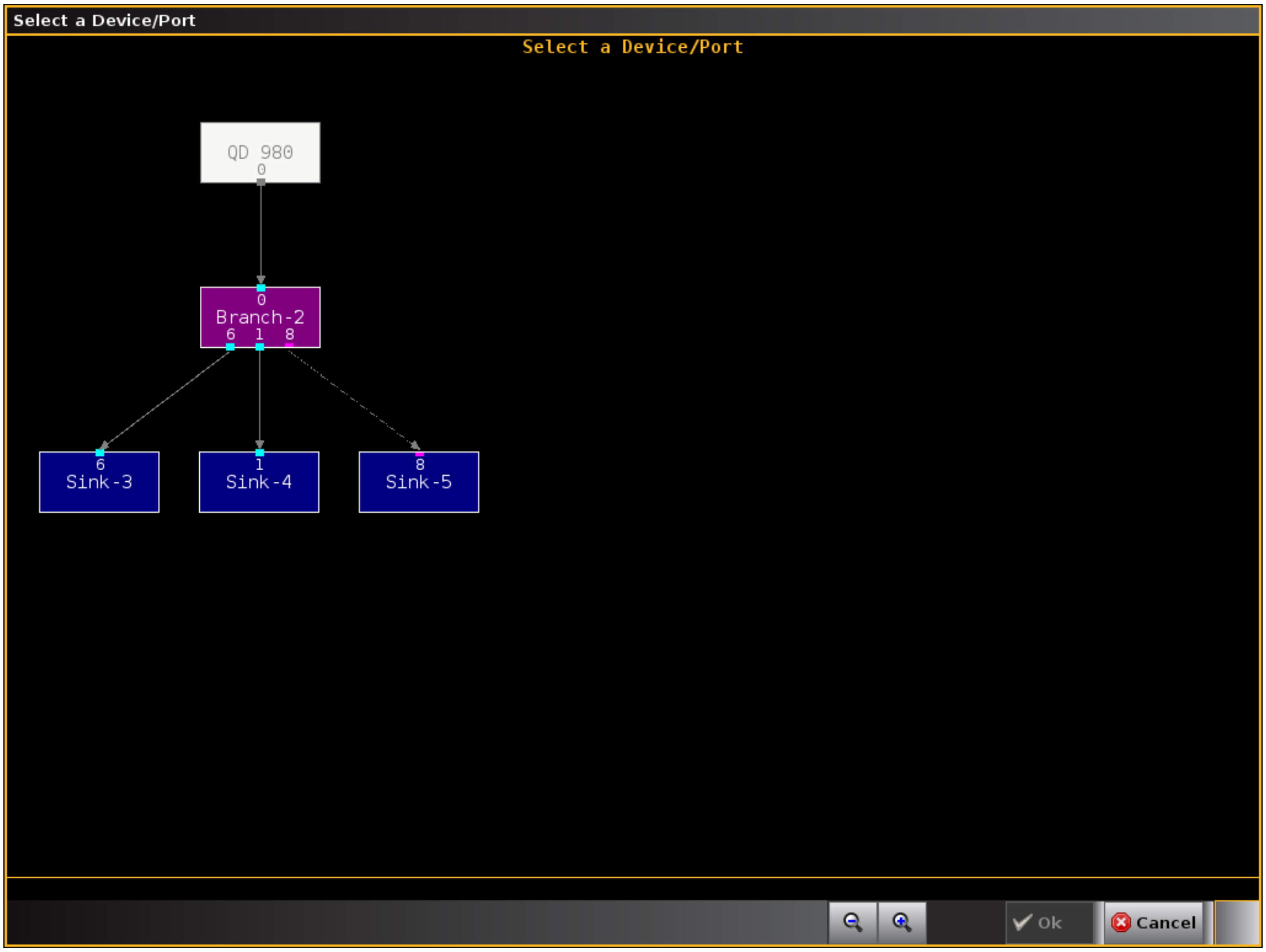
To read the EDID of a downstream MST Rx node:

1. From the main window of the 980 DP Video Generator / Analyzer module, select the **Tools** tab.
2. Select EDID Decode and select the virtual port (downstream MST node) whose EDID you wish to read. Refer to the following screen example.

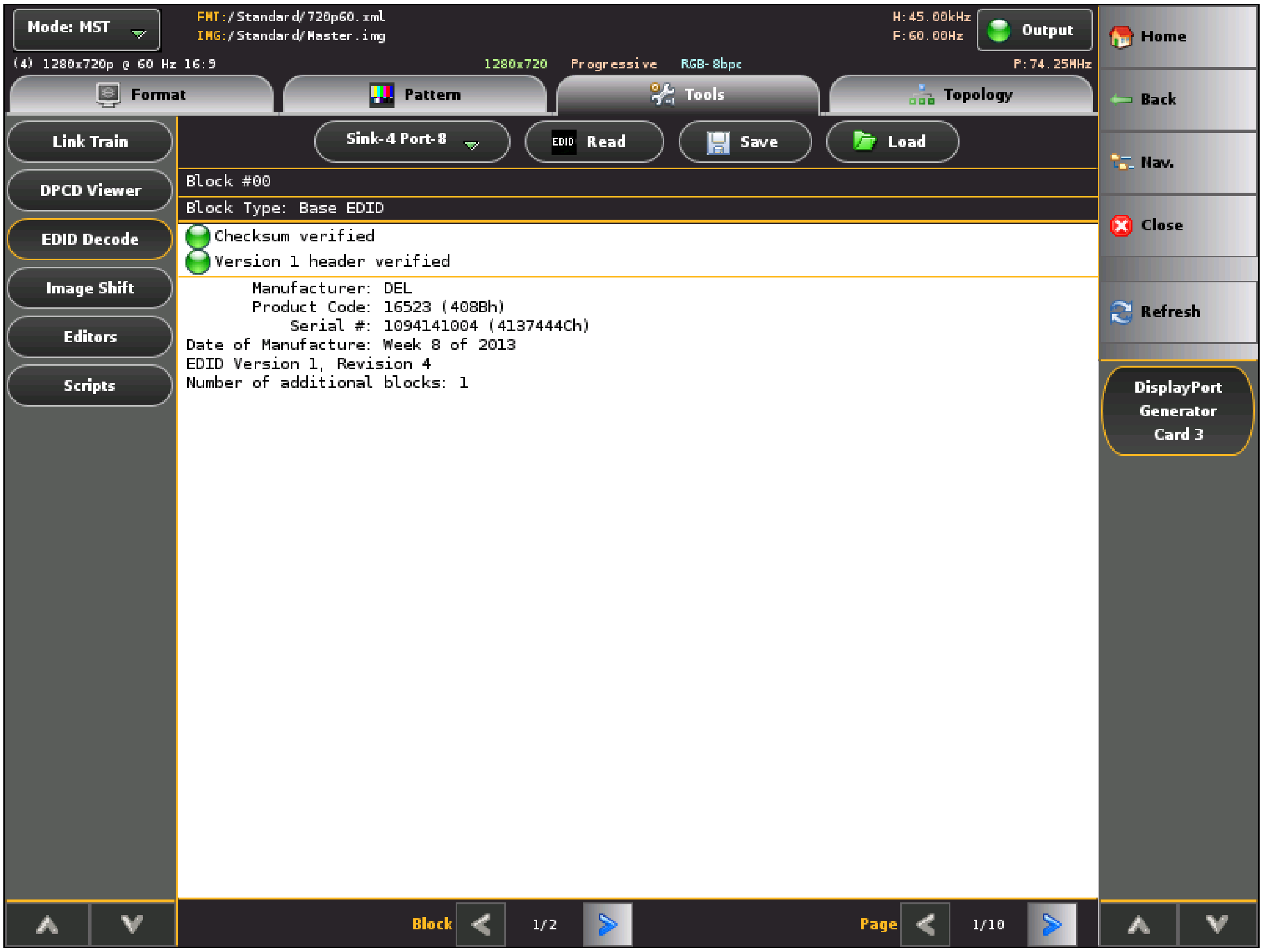


A window showing all the MST topology will appear.

3. The downstream nodes are shown in blue. Click Refresh if necessary. Select the desired downstream MST Rx node (Sink-3, Sink-4, Sink-5 in the example below).



The EDID will appear as shown in the following screen example. Follow procedures provided earlier in this User Guide to read each page of the EDID.



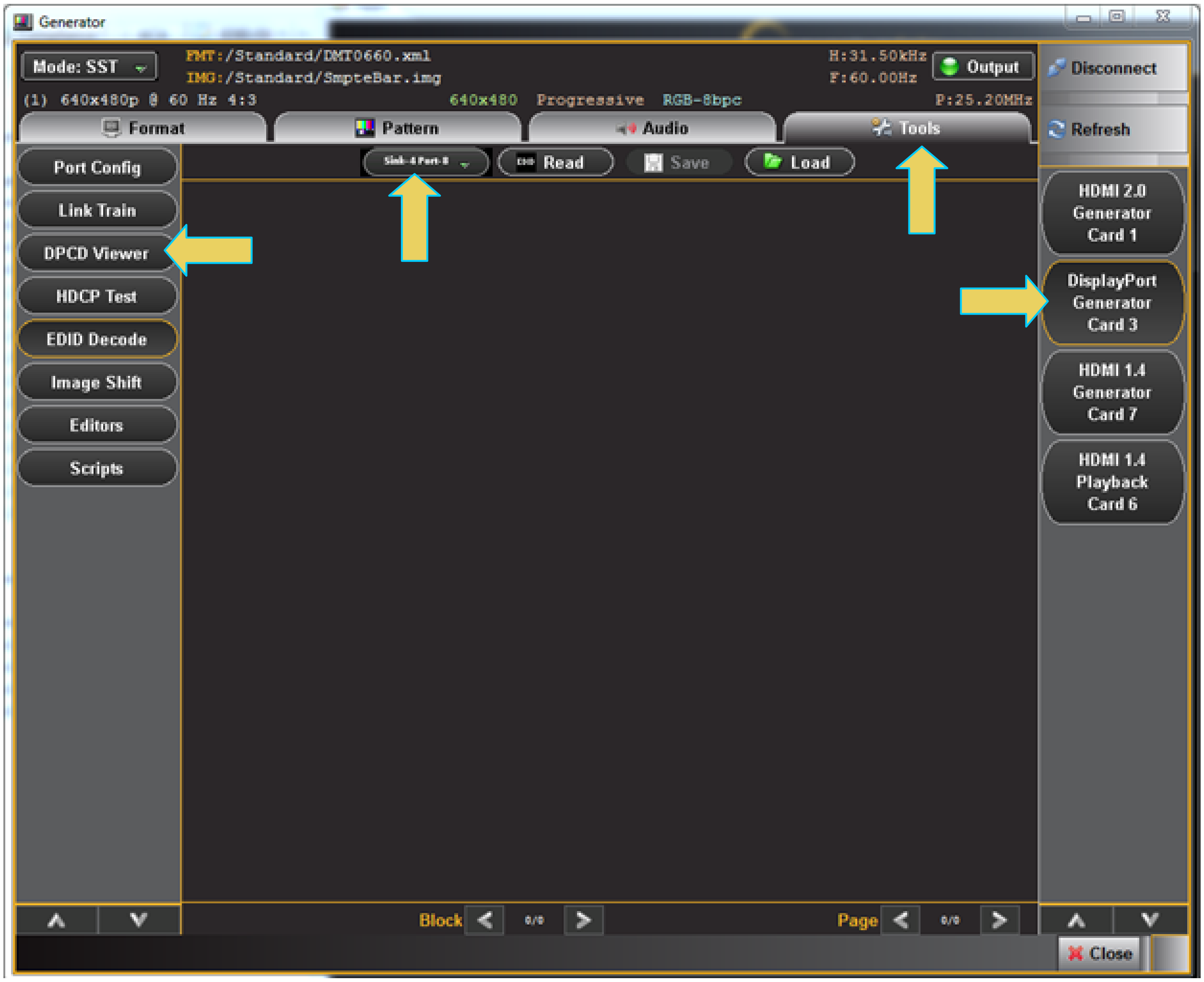
```
Block #00
Block Type: Base EDID
Checksum verified
Version 1 header verified
        Manufacturer: DEL
        Product Code: 16523 (408Bh)
            Serial #: 1094141004 (4137444Ch)
Date of Manufacture: Week 8 of 2013
EDID Version 1, Revision 4
Number of additional blocks: 1
```

6.4 Reading the DPCD of a downstream MST node.

Use the following procedures to read the EDID of any downstream MST Rx node. Currently the DPCD button shown on the left panel of the **Topology** window is not functional. To read the DPCD of a downstream not you have to use the DPCD read function in the **Tools** menu.

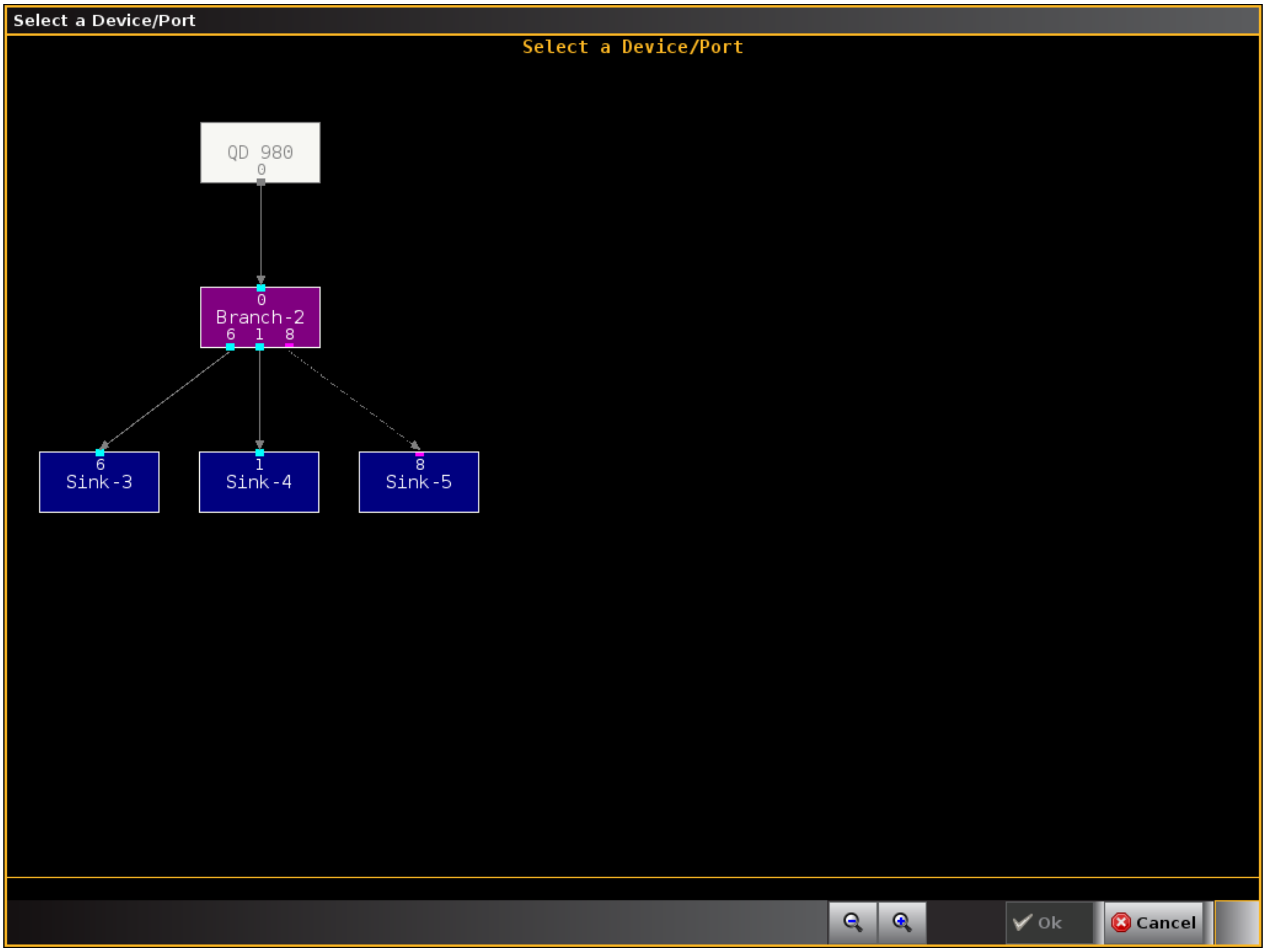
To read the DPCD of a downstream MST Rx node:

1. From the main window of the 980 DP Video Generator / Analyzer module, select the **Tools** tab.
2. Select DPCD Decode and select the virtual port (downstream MST node) whose DPCD you wish to read. Refer to the following screen example.

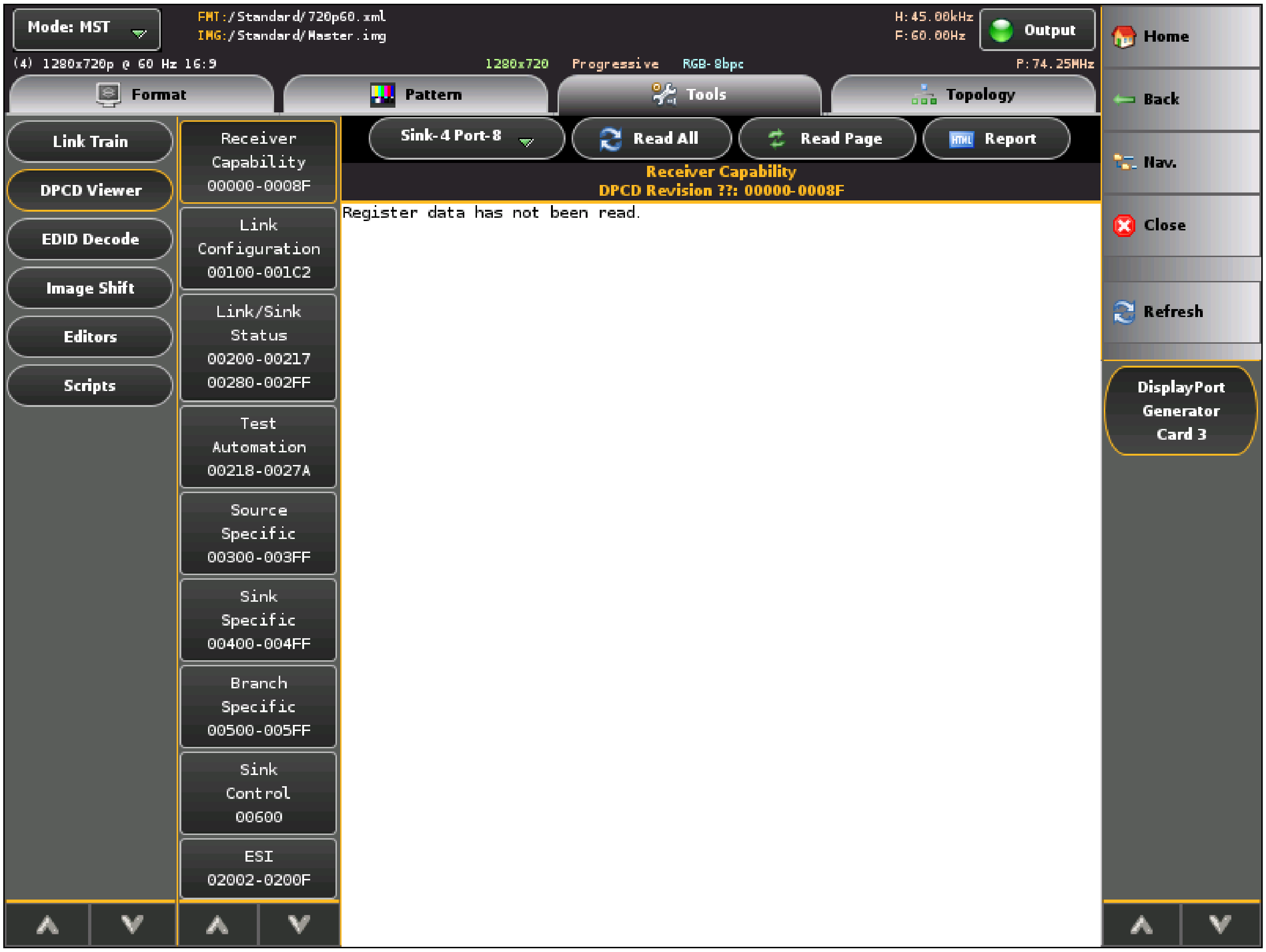


A window showing all the MST topology will appear.

3. The downstream nodes are shown in blue. Click Refresh if necessary. Select the desired downstream MST Rx node (Sink-3, Sink-4, Sink-5 in the example below).



The DPCD will appear as shown in the following screen example. Follow procedures provided earlier in this User Guide to read each register set Viewing the DPCD of a connected display.

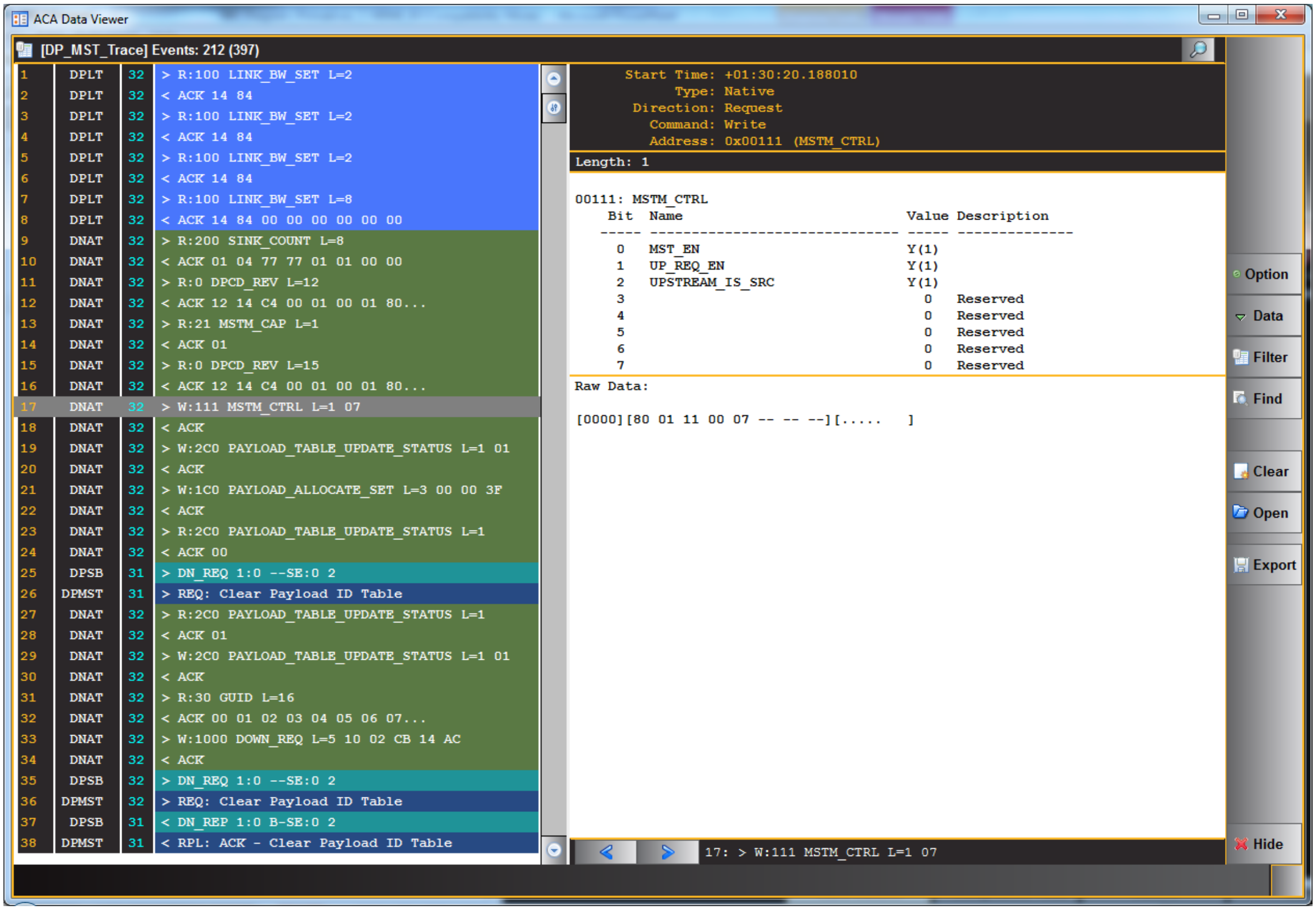


Receiver Capability
DPCD Revision ??: 00000-0008F

```
Register data has not been read.
```

6.5 View the MST transactions on the Auxiliary Channel Analyzer (ACA).

Refer to the ACA section Monitoring the DisplayPort auxiliary channels with the ACA utilities for procedures in monitoring the MST transactions associated with the MST negotiations. A sample screen shot is shown below.



```
[DP_MST_Trace] Events: 212 (397)
1    DPLT   32  > R:100 LINK_BW_SET L=2
2    DPLT   32  < ACK 14 84
3    DPLT   32  > R:100 LINK_BW_SET L=2
4    DPLT   32  < ACK 14 84
5    DPLT   32  > R:100 LINK_BW_SET L=2
6    DPLT   32  < ACK 14 84
7    DPLT   32  > R:100 LINK_BW_SET L=8
8    DPLT   32  < ACK 14 84 00 00 00 00 00 00
9    DNAT   32  > R:200 SINK_COUNT L=8
10   DNAT   32  < ACK 01 04 77 77 01 01 00 00
11   DNAT   32  > R:0 DPCD_REV L=12
12   DNAT   32  < ACK 12 14 C4 00 01 00 01 80...
13   DNAT   32  > R:21 MSTM_CAP L=1
14   DNAT   32  < ACK 01
15   DNAT   32  > R:0 DPCD_REV L=15
16   DNAT   32  < ACK 12 14 C4 00 01 00 01 80...
17   DNAT   32  > W:111 MSTM_CTRL L=1 07
18   DNAT   32  < ACK
19   DNAT   32  > W:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1 01
20   DNAT   32  < ACK
21   DNAT   32  > W:1C0 PAYLOAD_ALLOCATE_SET L=3 00 00 3F
22   DNAT   32  < ACK
23   DNAT   32  > R:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1
24   DNAT   32  < ACK 00
25   DPSB   31  > DN_REQ 1:0 --SE:0 2
26   DPMST  31  > REQ: Clear Payload ID Table
27   DNAT   32  > R:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1
28   DNAT   32  < ACK 01
29   DNAT   32  > W:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1 01
30   DNAT   32  < ACK
31   DNAT   32  > R:30 GUID L=16
32   DNAT   32  < ACK 00 01 02 03 04 05 06 07...
33   DNAT   32  > W:1000 DOWN_REQ L=5 10 02 CB 14 AC
34   DNAT   32  < ACK
35   DPSB   32  > DN_REQ 1:0 --SE:0 2
36   DPMST  32  > REQ: Clear Payload ID Table
37   DPSB   31  < DN_REP 1:0 B-SE:0 2
38   DPMST  31  < RPL: ACK - Clear Payload ID Table
```

```
      Start Time: +01:30:20.188010
            Type: Native
       Direction: Request
         Command: Write
         Address: 0x00111 (MSTM_CTRL)
Length: 1

00111: MSTM_CTRL
    Bit  Name                           Value Description
   ----- ------------------------------ ----- --------------
     0   MST_EN                         Y(1)
     1   UP_REQ_EN                      Y(1)
     2   UPSTREAM_IS_SRC                Y(1)
     3                                    0   Reserved
     4                                    0   Reserved
     5                                    0   Reserved
     6                                    0   Reserved
     7                                    0   Reserved
Raw Data:

[0000][80 01 11 00 07 -- -- --][.....   ]

17: > W:111 MSTM_CTRL L=1 07
```

7 Auxiliary Channel Analyzer (ACA) Utilities

The Auxiliary Channel Analyzer **(ACA)** utilities enable you to view the DDC and aux channel traffic for DisplayPort streams in real time or from stored real time log files. For DisplayPort, you can view the HDCP authentication transactions, EDID exchanges, Link Training transactions, side band messages, MST negotiations, etc. in real time with the ACA either through the embedded 980 GUI or the external 980 GUI Manager application running on a host PC. You can view the transactions between the 980 DP Video Generator ports and a connected DP display device and you can monitor the transactions between the 980 DP Video Generator's Analyzer port and a connected DP source device.

There are three (3) Auxiliary Channel Analyzer utilities:

- **Auxiliary Channel Analyzer ("ACA")** – Used for real time viewing auxiliary channel DisplayPort Aux Chan data through the *embedded* 980 GUI Manager. You can also open existing ACA trace files stored on the 980 Instrument.
- **ACA Remote Control** - Used for viewing auxiliary channel DisplayPort data through the *external* 980 GUI Manager. This application operates in sync with the Aux Channel Analyzer on the embedded display.
- **ACA Data Viewer -** Used for viewing previously captured auxiliary channel data. You can view these saved ACA traces and disseminate them to colleagues at other locations. These colleagues can then use the ACA Data Viewer utility off-line without a 980 test instrument to view these transactions.

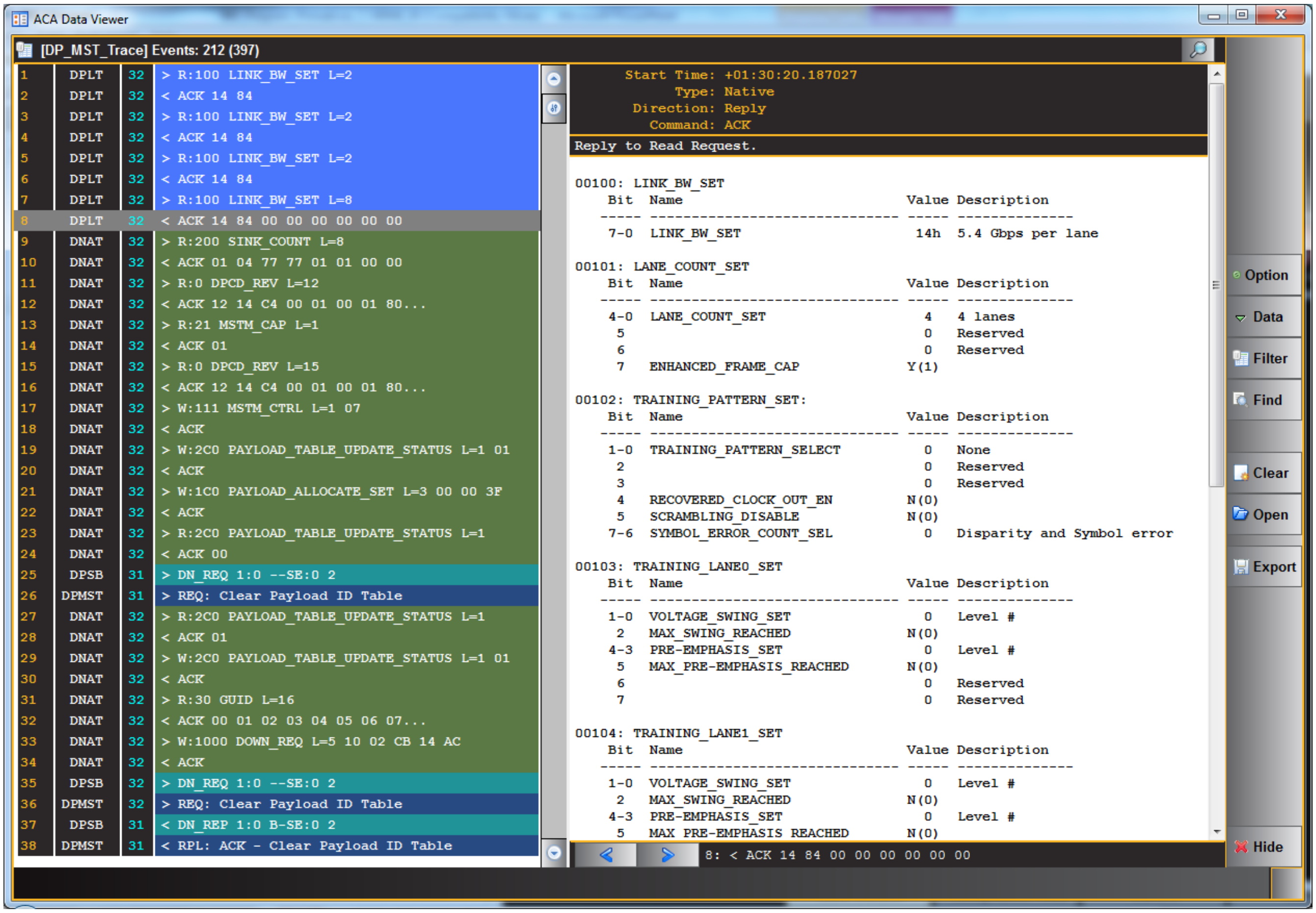
7.1 Aux Channel Analyzer (ACA) – For Real Time Viewing of Auxiliary Channel Data

This subsection describes the **Aux Channel Analyzer** utility used for viewing the real time auxiliary channel data through the *embedded* 980 GUI Manager.

7.1.1 Aux Channel Analyzer (ACA) – Panel Description

The Aux Channel Analyzer panel is described in the table below. There is a control menu panel on the right side. The control menu and elements of the ACA panel are described in the following table.

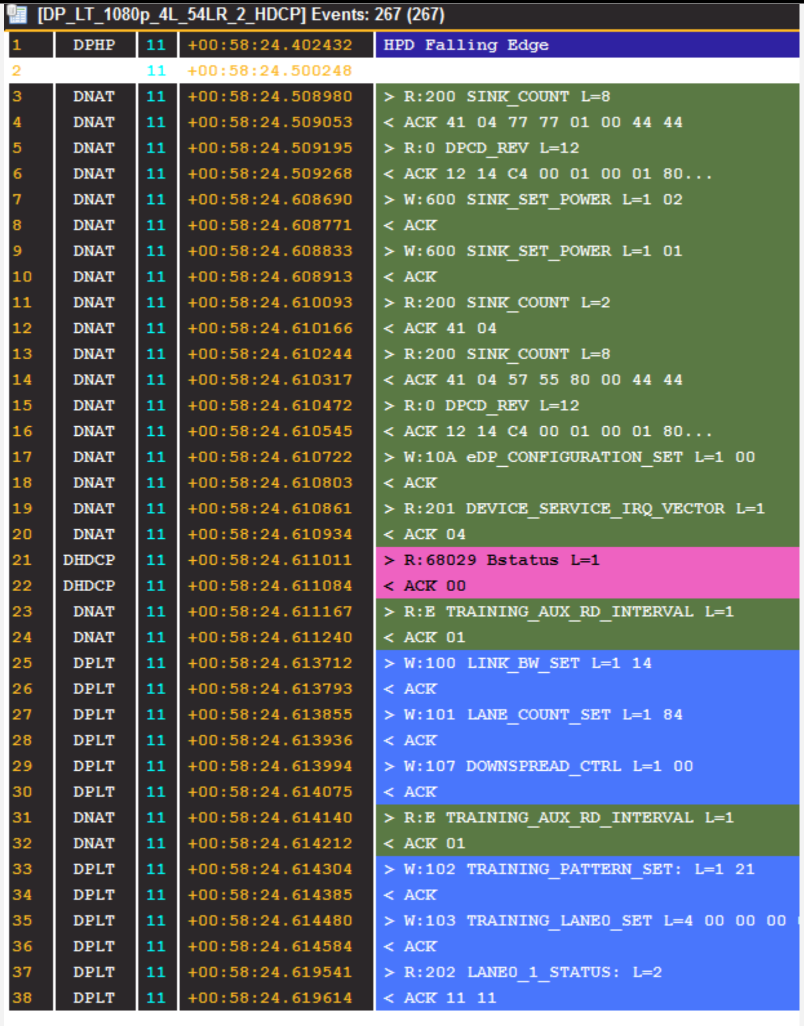
The following is an example of a populated ACA window.



```
[DP_MST_Trace] Events: 212 (397)
1   DPLT   32  > R:100 LINK_BW_SET L=2
2   DPLT   32  < ACK 14 84
3   DPLT   32  > R:100 LINK_BW_SET L=2
4   DPLT   32  < ACK 14 84
5   DPLT   32  > R:100 LINK_BW_SET L=2
6   DPLT   32  < ACK 14 84
7   DPLT   32  > R:100 LINK_BW_SET L=8
8   DPLT   32  < ACK 14 84 00 00 00 00 00 00
9   DNAT   32  > R:200 SINK_COUNT L=8
10  DNAT   32  < ACK 01 04 77 77 01 01 00 00
11  DNAT   32  > R:0 DPCD_REV L=12
12  DNAT   32  < ACK 12 14 C4 00 01 00 01 80...
13  DNAT   32  > R:21 MSTM_CAP L=1
14  DNAT   32  < ACK 01
15  DNAT   32  > R:0 DPCD_REV L=15
16  DNAT   32  < ACK 12 14 C4 00 01 00 01 80...
17  DNAT   32  > W:111 MSTM_CTRL L=1 07
18  DNAT   32  < ACK
19  DNAT   32  > W:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1 01
20  DNAT   32  < ACK
21  DNAT   32  > W:1C0 PAYLOAD_ALLOCATE_SET L=3 00 00 3F
22  DNAT   32  < ACK
23  DNAT   32  > R:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1
24  DNAT   32  < ACK 00
25  DPSB   31  > DN_REQ 1:0 --SE:0 2
26  DPMST  31  > REQ: Clear Payload ID Table
27  DNAT   32  > R:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1
28  DNAT   32  < ACK 01
29  DNAT   32  > W:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1 01
30  DNAT   32  < ACK
31  DNAT   32  > R:30 GUID L=16
32  DNAT   32  < ACK 00 01 02 03 04 05 06 07...
33  DNAT   32  > W:1000 DOWN_REQ L=5 10 02 CB 14 AC
34  DNAT   32  < ACK
35  DPSB   32  > DN_REQ 1:0 --SE:0 2
36  DPMST  32  > REQ: Clear Payload ID Table
37  DPSB   31  < DN_REP 1:0 B-SE:0 2
38  DPMST  31  < RPL: ACK - Clear Payload ID Table
```

```
    Start Time: +01:30:20.187027
          Type: Native
     Direction: Reply
       Command: ACK
Reply to Read Request.

00100: LINK_BW_SET
    Bit  Name                           Value Description
   ----- ------------------------------ ----- --------------
    7-0  LINK_BW_SET                     14h  5.4 Gbps per lane

00101: LANE_COUNT_SET
    Bit  Name                           Value Description
   ----- ------------------------------ ----- --------------
    4-0  LANE_COUNT_SET                   4   4 lanes
     5                                    0   Reserved
     6                                    0   Reserved
     7   ENHANCED_FRAME_CAP             Y(1)

00102: TRAINING_PATTERN_SET:
    Bit  Name                           Value Description
   ----- ------------------------------ ----- --------------
    1-0  TRAINING_PATTERN_SELECT          0   None
     2                                    0   Reserved
     3                                    0   Reserved
     4   RECOVERED_CLOCK_OUT_EN         N(0)
     5   SCRAMBLING_DISABLE             N(0)
    7-6  SYMBOL_ERROR_COUNT_SEL           0   Disparity and Symbol error

00103: TRAINING_LANE0_SET
    Bit  Name                           Value Description
   ----- ------------------------------ ----- --------------
    1-0  VOLTAGE_SWING_SET                0   Level #
     2   MAX_SWING_REACHED              N(0)
    4-3  PRE-EMPHASIS_SET                 0   Level #
     5   MAX_PRE-EMPHASIS_REACHED       N(0)
     6                                    0   Reserved
     7                                    0   Reserved

00104: TRAINING_LANE1_SET
    Bit  Name                           Value Description
   ----- ------------------------------ ----- --------------
    1-0  VOLTAGE_SWING_SET                0   Level #
     2   MAX_SWING_REACHED              N(0)
    4-3  PRE-EMPHASIS_SET                 0   Level #
     5   MAX_PRE-EMPHASIS_REACHED       N(0)

8: < ACK 14 84 00 00 00 00 00 00
```

Real Time – ACA	**Information / Function**
Aux Channel Analyzer (ACA) **ACA Trace Panel** Transaction Example showing HDCP and Link Training transactions.	The following information is provided in the ACA data dialog box for each Event: ▪ **Item number** – This is a unique sequence number of the transaction. ▪ **Type** – There are various types of data that can be monitored on the DisplayPort interfaces: EDID, HDCP and DP specific data types related to Link Training, side band messaging, MST transactions, native transactions, etc.) ▪ **980 Port number, slot number**. ▪ **Time stamp** (optional viewing field) – Shows the timestamp of each transaction. Can either be absolute time based (shown) on the 980 system clock or relative time (Time

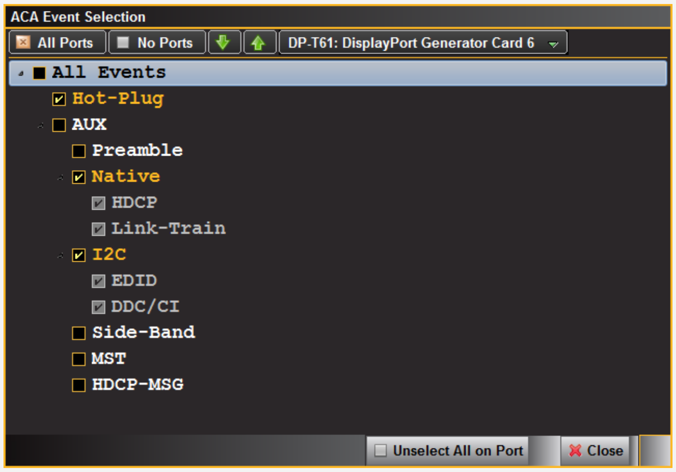
Real Time – ACA	**Information / Function**
	-deltas) referenced from the initial transaction in the trace. - **Transaction Description** – A description of the transaction.

[DP_LT_1080p_4L_54LR_2_HDCP] Events: 267 (267)

```
1   DPHP   11  +00:58:24.402432  HPD Falling Edge
2          11  +00:58:24.500248
3   DNAT   11  +00:58:24.508980  > R:200 SINK_COUNT L=8
4   DNAT   11  +00:58:24.509053  < ACK 41 04 77 77 01 00 44 44
5   DNAT   11  +00:58:24.509195  > R:0 DPCD_REV L=12
6   DNAT   11  +00:58:24.509268  < ACK 12 14 C4 00 01 00 01 80...
7   DNAT   11  +00:58:24.608690  > W:600 SINK_SET_POWER L=1 02
8   DNAT   11  +00:58:24.608771  < ACK
9   DNAT   11  +00:58:24.608833  > W:600 SINK_SET_POWER L=1 01
10  DNAT   11  +00:58:24.608913  < ACK
11  DNAT   11  +00:58:24.610093  > R:200 SINK_COUNT L=2
12  DNAT   11  +00:58:24.610166  < ACK 41 04
13  DNAT   11  +00:58:24.610244  > R:200 SINK_COUNT L=8
14  DNAT   11  +00:58:24.610317  < ACK 41 04 57 55 80 00 44 44
15  DNAT   11  +00:58:24.610472  > R:0 DPCD_REV L=12
16  DNAT   11  +00:58:24.610545  < ACK 12 14 C4 00 01 00 01 80...
17  DNAT   11  +00:58:24.610722  > W:10A eDP_CONFIGURATION_SET L=1 00
18  DNAT   11  +00:58:24.610803  < ACK
19  DNAT   11  +00:58:24.610861  > R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
20  DNAT   11  +00:58:24.610934  < ACK 04
21  DHDCP  11  +00:58:24.611011  > R:68029 Bstatus L=1
22  DHDCP  11  +00:58:24.611084  < ACK 00
23  DNAT   11  +00:58:24.611167  > R:E TRAINING_AUX_RD_INTERVAL L=1
24  DNAT   11  +00:58:24.611240  < ACK 01
25  DPLT   11  +00:58:24.613712  > W:100 LINK_BW_SET L=1 14
26  DPLT   11  +00:58:24.613793  < ACK
27  DPLT   11  +00:58:24.613855  > W:101 LANE_COUNT_SET L=1 84
28  DPLT   11  +00:58:24.613936  < ACK
29  DPLT   11  +00:58:24.613994  > W:107 DOWNSPREAD_CTRL L=1 00
30  DPLT   11  +00:58:24.614075  < ACK
31  DNAT   11  +00:58:24.614140  > R:E TRAINING_AUX_RD_INTERVAL L=1
32  DNAT   11  +00:58:24.614212  < ACK 01
33  DPLT   11  +00:58:24.614304  > W:102 TRAINING_PATTERN_SET: L=1 21
34  DPLT   11  +00:58:24.614385  < ACK
35  DPLT   11  +00:58:24.614480  > W:103 TRAINING_LANE0_SET L=4 00 00 00
36  DPLT   11  +00:58:24.614584  < ACK
37  DPLT   11  +00:58:24.619541  > R:202 LANE0_1_STATUS: L=2
38  DPLT   11  +00:58:24.619614  < ACK 11 11
```

ACA Control Menu

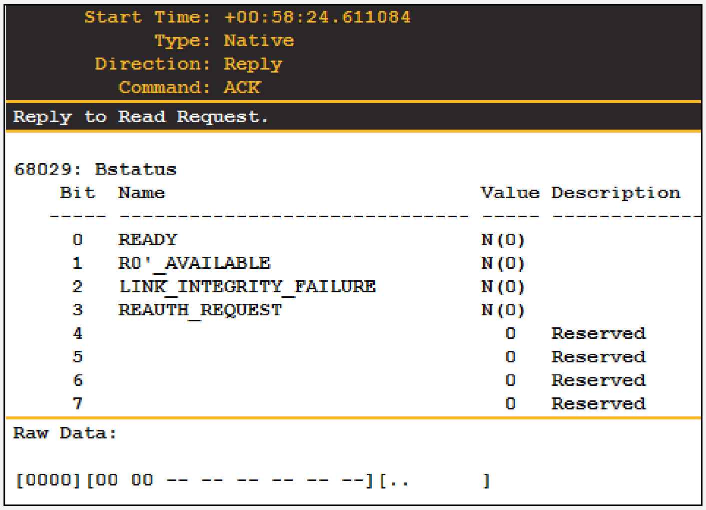
ACA Event Selection



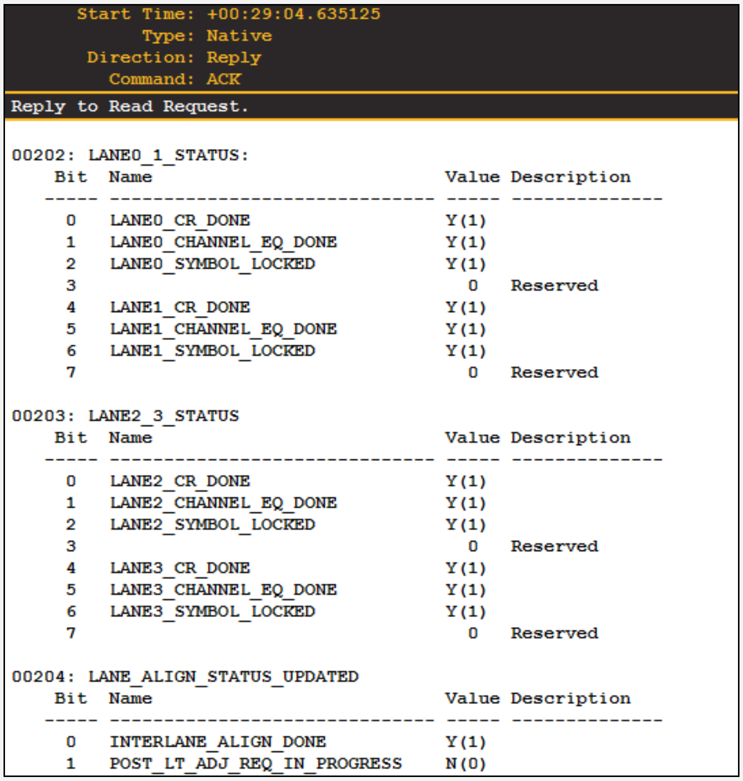
■ All Events
- ☑ Hot-Plug
- ☐ AUX
  - ☐ Preamble
  - ☑ Native
    - ☑ HDCP
    - ☑ Link-Train
  - ☑ I2C
    - ☑ EDID
    - ☑ DDC/CI
  - ☐ Side-Band
  - ☐ MST
  - ☐ HDCP-MSG

There is a menu associated with the ACA Info panel. It is location on the right side of the panel. The ACA pull-down menu provides the following functions:

- **Home** – Navigates you back to the Home menu screen of the embedded 980 GUI Manager.
- **Back** – Navigates back to the previous screen in the Real Time mode.
- **Nav** – Takes you to the Navigation window.
- **Close** – Closes out the ACA application.
- **Start/Stop** – Starts and Stops the collection of DDC data.
- **Resume/Pause** – Halts the updates of the data to the ACA panel to view traces and allows you to resume.
- **Events** – Opens up the **ACA Event Selection** window (below left) enabling you to specify the module and port that you wish to collect trace data from. Also selects which events you wish to collect. Use the check boxes to select which event you wish to collect or collect All Events.
- **Options** – Opens up a flyout menu described below-left.
- **Data** – Opens up flyout menu with the following options (described below).
- **Clear** – Clears the ACA Trace Panel.
- **Open** – Opens an existing trace file stored on the 980.
- **Save** – Saves a current trace file to the 980 file system.



```
      Start Time: +00:58:24.611084
            Type: Native
       Direction: Reply
         Command: ACK
Reply to Read Request.

68029: Bstatus
    Bit  Name                           Value Description
   ----- ------------------------------ ----- -------------
     0   READY                          N(0)
     1   R0'_AVAILABLE                  N(0)
     2   LINK_INTEGRITY_FAILURE         N(0)
     3   REAUTH_REQUEST                 N(0)
     4                                    0   Reserved
     5                                    0   Reserved
     6                                    0   Reserved
     7                                    0   Reserved
Raw Data:

[0000][00 00 -- -- -- -- -- --][..       ]
```



```
      Start Time: +00:29:04.635125
            Type: Native
       Direction: Reply
         Command: ACK
Reply to Read Request.

00202: LANE0_1_STATUS:
    Bit  Name                           Value Description
   ----- ------------------------------ ----- -------------
     0   LANE0_CR_DONE                  Y(1)
     1   LANE0_CHANNEL_EQ_DONE          Y(1)
     2   LANE0_SYMBOL_LOCKED            Y(1)
     3                                    0   Reserved
     4   LANE1_CR_DONE                  Y(1)
     5   LANE1_CHANNEL_EQ_DONE          Y(1)
     6   LANE1_SYMBOL_LOCKED            Y(1)
     7                                    0   Reserved

00203: LANE2_3_STATUS
    Bit  Name                           Value Description
   ----- ------------------------------ ----- -------------
     0   LANE2_CR_DONE                  Y(1)
     1   LANE2_CHANNEL_EQ_DONE          Y(1)
     2   LANE2_SYMBOL_LOCKED            Y(1)
     3                                    0   Reserved
     4   LANE3_CR_DONE                  Y(1)
     5   LANE3_CHANNEL_EQ_DONE          Y(1)
     6   LANE3_SYMBOL_LOCKED            Y(1)
     7                                    0   Reserved

00204: LANE_ALIGN_STATUS_UPDATED
    Bit  Name                           Value Description
   ----- ------------------------------ ----- -------------
     0   INTERLANE_ALIGN_DONE           Y(1)
     1   POST_LT_ADJ_REQ_IN_PROGRESS    N(0)
```

The following information is provided in the ACA **Event Details** dialog box. Two examples are shown on the left. One for HDCP transactions and another for Link Training transactions:

- **Type** – There are various types of data that can be monitored on the DisplayPort interfaces: EDID, HDCP and DP specific data types related to Link Training, side band messaging, MST transactions, native transactions, etc.)
- **Start Time** – This the start time of the transaction in microseconds from a reference time determined when the capture of real time data began.

Note: The information in the Details panel will vary depending on the type of log record that is selected.

- **Duration** – The duration in milliseconds of the transaction.
- **Direction** – The direction of the transaction either a request or a reply.
- **Maximum I2C Rate** – The rate that the I2C channel clock is operating.
- **Details** (text) – The contents of the transaction in human readable text.
- **Details** (hex) – The contents of the transaction in hex data.

There are some control arrows and a status panel on the bottom of the ACA Event Details panel. These are as follows:

- **Left arrow** – The left arrow allows you to see the details of the next transaction.
- **Right arrow** – The right arrow allows you to see the details of the previous transaction.
- **Status field** – Shows the sequence number and the description of the selected

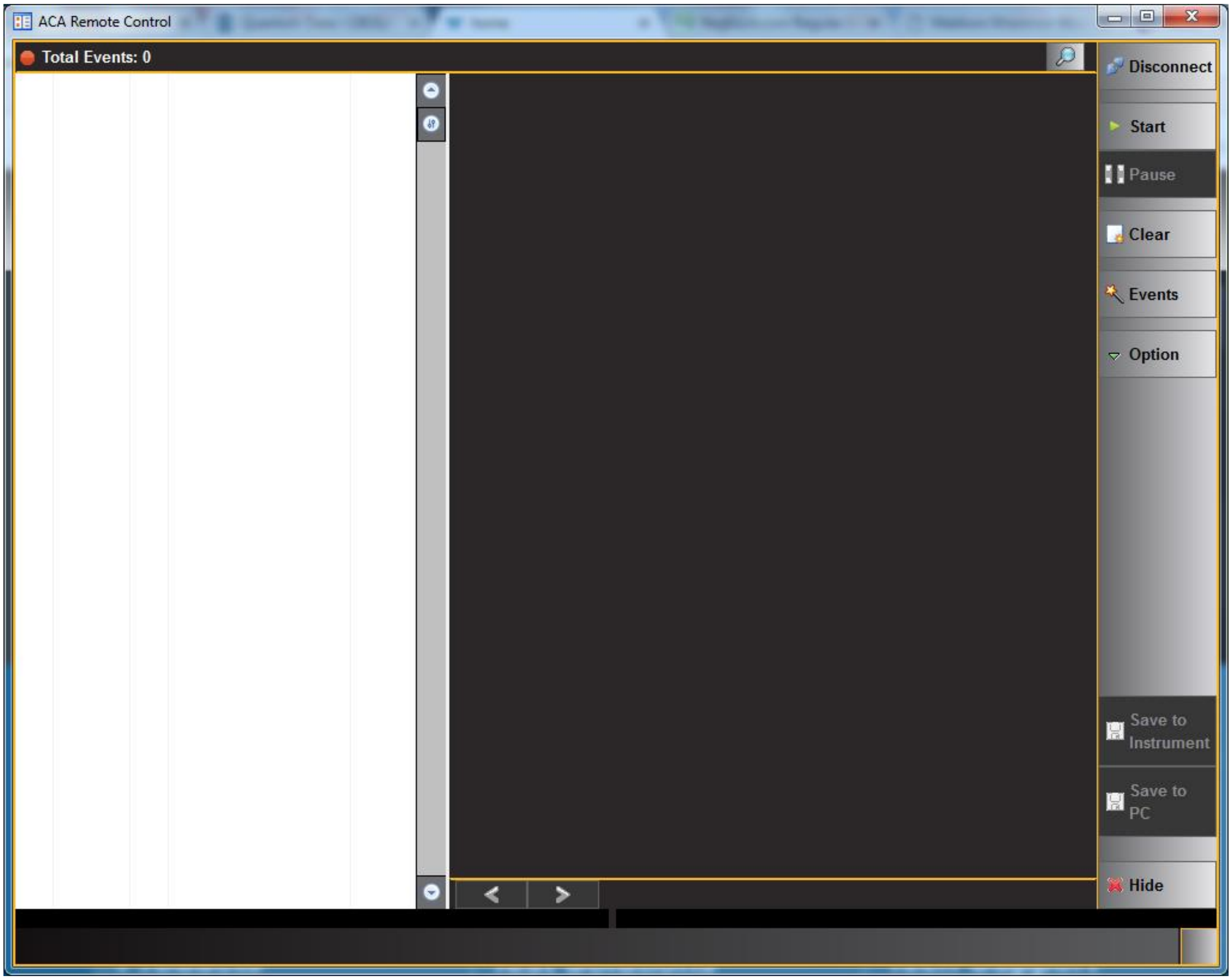
	transaction.
Options Flyout Menu  	The **Options** flyout menu items are described below. These options are only available on the Real Time ACA when the trace logging is stopped. ▪ **Scroll Lock** – The left arrow allows you to see the details of the next transaction. ▪ **Source Legend** – Displays a dialog box listing the interface cards on the 980 Instrument and their slot and port numbers, e.g. 32 is Slot 3, Port 2. ▪ **Show Port Name** – Enables you to display or not display the Port number. ▪ **Show Time-stamp** – Enables you to show or not show the time stamps for each transaction. ▪ **Show Time-deltas** – Enables you to show the time stamps relative to the previous transaction. Only available when Time-Stamps are shown (see above). ▪ **Set Zero Time** – Enables you to set a log record to zero. Subsequent log records are relative to this new zero time record. ▪ **Reset to Zero Time** – Resets the initial record in the active log in the ACA Trace window to zero.
Data Flyout Menu  	The **Data** flyout menu items are described below: ▪ **Sort by time** checkbox – Greyed out. ▪ **Filter** – Opens up a dialog box for filtering the current ACA log based on criteria you select. The Filter function is described in detail in the procedures in the following subsection. The Filter function is only available when the logging is stopped. ▪ **Find** – Opens up a dialog box for searching the current ACA log based on criteria you select. The Find function is described in detail in the procedures in the following subsection. The Find function is only available when the logging is stopped.

7.2 ACA Remote Control – For Real Time Viewing of DisplayPort Aux Channel Data

This subsection describes the **ACA Remote Control** utility used for viewing the real time DisplayPort Aux Channel transactions through the *external* 980 GUI Manager.

7.2.1 ACA Remote Control – Panel Description

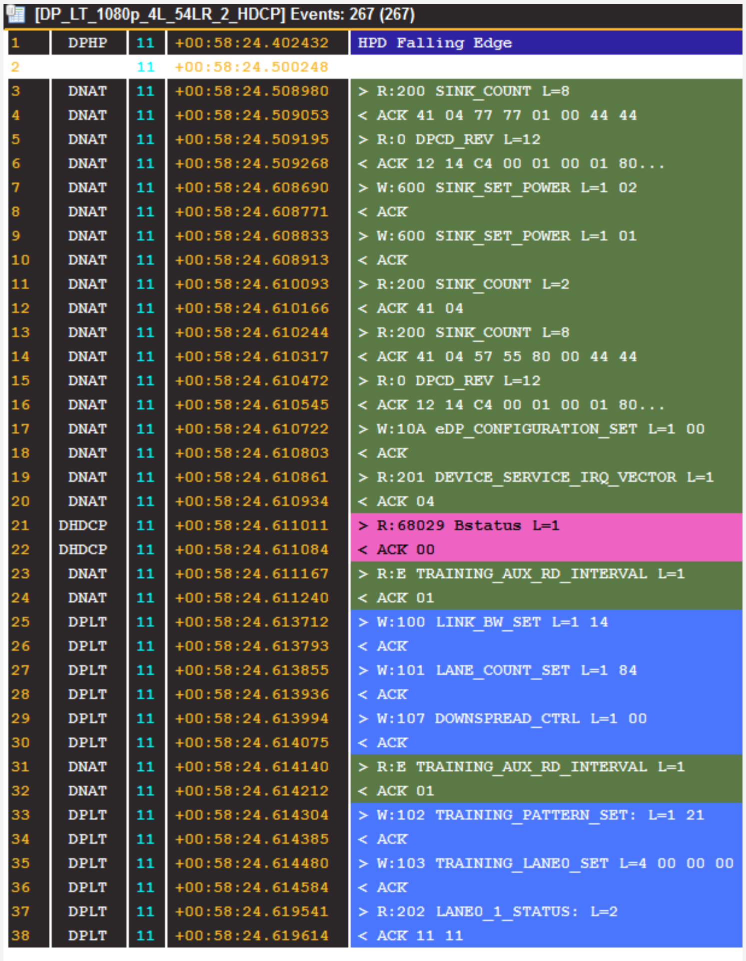
The **ACA Remote Control** panel application is available only on the *external* 980 GUI Manager. It enables you to collect and view the ACA transactions in real time from a remotely connected PC with the 980 GUI Manager application. The control panel elements are described in the table below.



ACA Remote Control | **Information / Function**

Auxiliary Channel Analyzer

ACA Trace Panel



```
[DP_LT_1080p_4L_54LR_2_HDCP] Events: 267 (267)
1    DPHP   11  +00:58:24.402432  HPD Falling Edge
2           11  +00:58:24.500248
3    DNAT   11  +00:58:24.508980  > R:200 SINK_COUNT L=8
4    DNAT   11  +00:58:24.509053  < ACK 41 04 77 77 01 00 44 44
5    DNAT   11  +00:58:24.509195  > R:0 DPCD_REV L=12
6    DNAT   11  +00:58:24.509268  < ACK 12 14 C4 00 01 00 01 80...
7    DNAT   11  +00:58:24.608690  > W:600 SINK_SET_POWER L=1 02
8    DNAT   11  +00:58:24.608771  < ACK
9    DNAT   11  +00:58:24.608833  > W:600 SINK_SET_POWER L=1 01
10   DNAT   11  +00:58:24.608913  < ACK
11   DNAT   11  +00:58:24.610093  > R:200 SINK_COUNT L=2
12   DNAT   11  +00:58:24.610166  < ACK 41 04
13   DNAT   11  +00:58:24.610244  > R:200 SINK_COUNT L=8
14   DNAT   11  +00:58:24.610317  < ACK 41 04 57 55 80 00 44 44
15   DNAT   11  +00:58:24.610472  > R:0 DPCD_REV L=12
16   DNAT   11  +00:58:24.610545  < ACK 12 14 C4 00 01 00 01 80...
17   DNAT   11  +00:58:24.610722  > W:10A eDP_CONFIGURATION_SET L=1 00
18   DNAT   11  +00:58:24.610803  < ACK
19   DNAT   11  +00:58:24.610861  > R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
20   DNAT   11  +00:58:24.610934  < ACK 04
21   DHDCP  11  +00:58:24.611011  > R:68029 Bstatus L=1
22   DHDCP  11  +00:58:24.611084  < ACK 00
23   DNAT   11  +00:58:24.611167  > R:E TRAINING_AUX_RD_INTERVAL L=1
24   DNAT   11  +00:58:24.611240  < ACK 01
25   DPLT   11  +00:58:24.613712  > W:100 LINK_BW_SET L=1 14
26   DPLT   11  +00:58:24.613793  < ACK
27   DPLT   11  +00:58:24.613855  > W:101 LANE_COUNT_SET L=1 84
28   DPLT   11  +00:58:24.613936  < ACK
29   DPLT   11  +00:58:24.613994  > W:107 DOWNSPREAD_CTRL L=1 00
30   DPLT   11  +00:58:24.614075  < ACK
31   DNAT   11  +00:58:24.614140  > R:E TRAINING_AUX_RD_INTERVAL L=1
32   DNAT   11  +00:58:24.614212  < ACK 01
33   DPLT   11  +00:58:24.614304  > W:102 TRAINING_PATTERN_SET: L=1 21
34   DPLT   11  +00:58:24.614385  < ACK
35   DPLT   11  +00:58:24.614480  > W:103 TRAINING_LANE0_SET L=4 00 00 00
36   DPLT   11  +00:58:24.614584  < ACK
37   DPLT   11  +00:58:24.619541  > R:202 LANE0_1_STATUS: L=2
38   DPLT   11  +00:58:24.619614  < ACK 11 11
```

The following information is provided in the ACA Remote Control Panel data dialog box for each event:

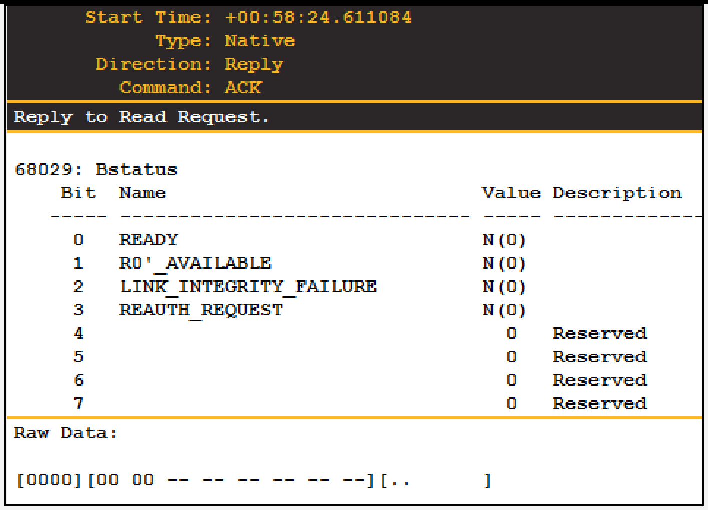
- **Item number** – This is a unique sequence number of the transaction.
- **Type** – There are various types of data that can be monitored on the DisplayPort interfaces: EDID, HDCP as well as the several Link Training, side band and MST transactions, native transactions, etc.)
- **980 Card** number, Interface number.
- **Time stamp** (optional viewing field) – Shows the timestamp of each transaction. Can either be absolute time based (shown) on the 980 system clock or relative time (Time-deltas) referenced from the initial transaction in the trace.
- **Transaction Description** – A description of the transaction.

Details Panel

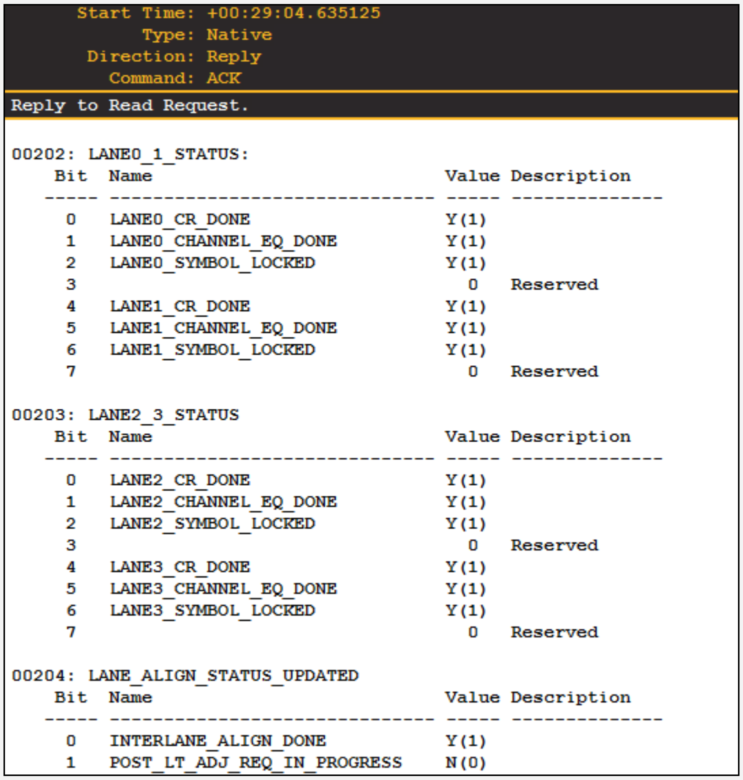
The following information is provided in the ACA **Event Details** dialog box. Two examples are shown on the left. One for HDCP transactions and another for Link Training transactions:

- **Type** – There are various types of data that can be monitored on the DisplayPort interfaces: EDID, HDCP as well as the several Link Training, side band and MST transactions, native transactions, etc.)
- **Start Time** – This the start time of the transaction in microseconds from a reference time determined when the

ACA Remote Control | **Information / Function**



```
      Start Time: +00:58:24.611084
            Type: Native
       Direction: Reply
         Command: ACK
Reply to Read Request.

68029: Bstatus
    Bit  Name                           Value Description
   ----- ------------------------------ ----- ------------
     0   READY                          N(0)
     1   R0'_AVAILABLE                  N(0)
     2   LINK_INTEGRITY_FAILURE         N(0)
     3   REAUTH_REQUEST                 N(0)
     4                                    0   Reserved
     5                                    0   Reserved
     6                                    0   Reserved
     7                                    0   Reserved
Raw Data:

[0000][00 00 -- -- -- -- -- --][..      ]
```

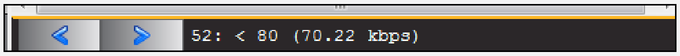


```
      Start Time: +00:29:04.635125
            Type: Native
       Direction: Reply
         Command: ACK
Reply to Read Request.

00202: LANE0_1_STATUS:
    Bit  Name                           Value Description
   ----- ------------------------------ ----- -------------
     0   LANE0_CR_DONE                  Y(1)
     1   LANE0_CHANNEL_EQ_DONE          Y(1)
     2   LANE0_SYMBOL_LOCKED            Y(1)
     3                                    0   Reserved
     4   LANE1_CR_DONE                  Y(1)
     5   LANE1_CHANNEL_EQ_DONE          Y(1)
     6   LANE1_SYMBOL_LOCKED            Y(1)
     7                                    0   Reserved

00203: LANE2_3_STATUS
    Bit  Name                           Value Description
   ----- ------------------------------ ----- -------------
     0   LANE2_CR_DONE                  Y(1)
     1   LANE2_CHANNEL_EQ_DONE          Y(1)
     2   LANE2_SYMBOL_LOCKED            Y(1)
     3                                    0   Reserved
     4   LANE3_CR_DONE                  Y(1)
     5   LANE3_CHANNEL_EQ_DONE          Y(1)
     6   LANE3_SYMBOL_LOCKED            Y(1)
     7                                    0   Reserved

00204: LANE_ALIGN_STATUS_UPDATED
    Bit  Name                           Value Description
   ----- ------------------------------ ----- -------------
     0   INTERLANE_ALIGN_DONE           Y(1)
     1   POST_LT_ADJ_REQ_IN_PROGRESS    N(0)
```

capture of real time data began.

Note: The information in the Details panel will vary depending on the type of log record that is selected.

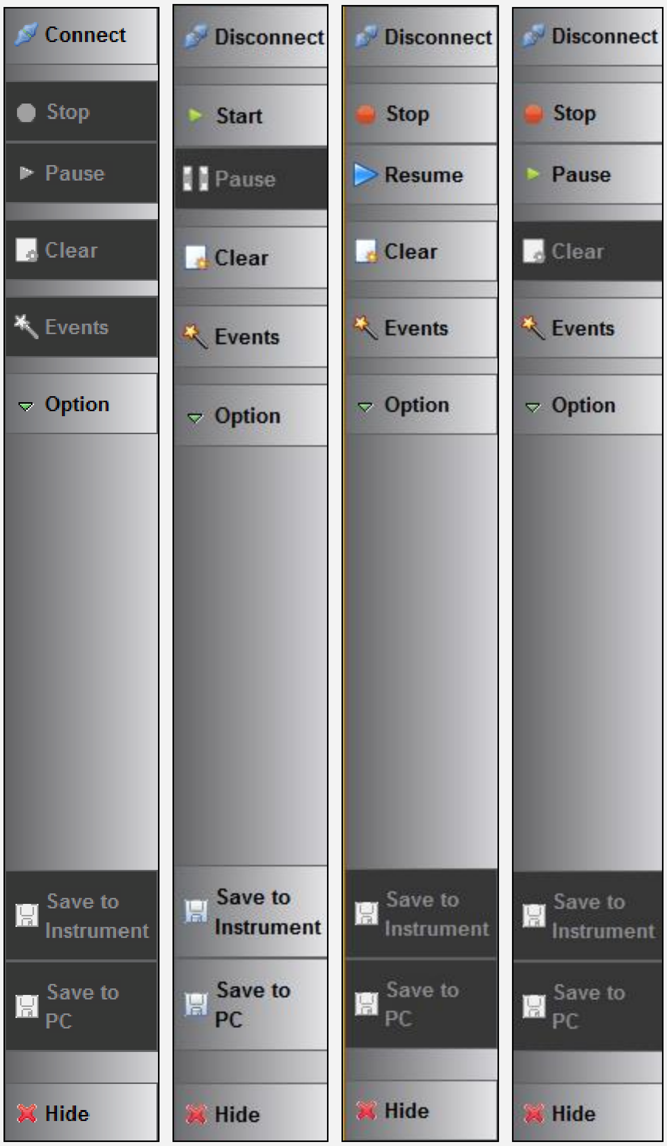
- **Duration** – The duration in milliseconds of the transaction.
- **Direction** – The direction of the transaction either a request or a reply.
- **Maximum I2C Rate** – The rate that the I2C channel clock is operating.
- **Details** (text) – The contents of the transaction in human readable text.
- **Details** (hex) – The contents of the transaction in hex data.

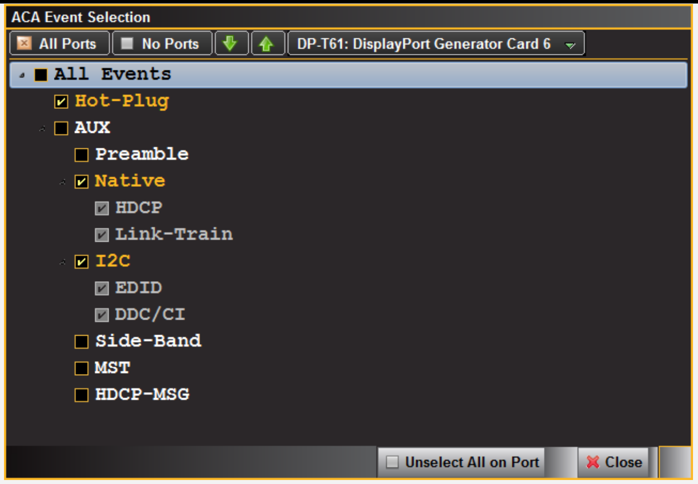


```
52: < 80 (70.22 kbps)
```

There are some control arrows and a status panel on the bottom of the ACA Event Details panel. These are as follows:

- **Left arrow** – The left arrow allows you to see the details of the next transaction.
- **Right arrow** – The right arrow allows you to see the details of the previous transaction.
- **Status field** – Shows the sequence

ACA Remote Control	Information / Function
	number and the description of the selected transaction.
 **ACA Event Selection**	There is a menu associated with the ACA Remote Control Info panel. It is location on the right side of the panel. There are four examples shown to the left reflecting the differ states: ▪ “Viewing Glass” – This icon is on the upper left of the ACA window. It is not part of the control menu. When activated it displays a pop up window that enables you to display the text in Small, Medium, or Large text. ▪ **Connect/Disconnect** – Connects or disconnects the ACA Remote Control application from a 980 System. ▪ **Start/Stop** – Starts and Stops the collection of auxiliary channel data. ▪ **Resume/Pause** – Pauses and/or Resumes the collection of auxiliary channel data to the ACA panel. ▪ **Clear** – Clears the ACA Trace Panel. The trace collection has to be paused or stopped in order to clear the traces. ▪ **Events** – Opens up the **ACA Event Selection** window (below left) enabling you to specify the module and port that you wish to collect trace data from. Also selects which events you wish to collect (left). Use the check boxes to select which event you wish to collect or collect All Events. ▪ **Options** – Opens up a flyout menu described below. ▪ **Save to Instrument** – Saves the file to the 980 system that the host PC is connected to. ▪ **Save to PC** – Saves a current trace file to the Host PC. ▪ **Hide** – Makes the ACA Remote Viewer window disappear.

ACA Remote Control	Information / Function
	
Options Flyout Menu 	The **Options** flyout menu items are described below. These options are only available on the real time ACA when the trace logging is stopped. ▪ **Scroll Lock** – The left arrow allows you to see the details of the next transaction. ▪ **Source Legend** – Displays a dialog box listing the interface cards on the 980 Instrument and their slot and port numbers, e.g. 32 is Slot 3, Port 2. ▪ **Show Port Name** – Enables you to display or not display the Port number. ▪ **Show Time-stamp** – Enables you to show or not show the time stamps for each transaction. ▪ **Show Time-deltas** – Enables you to show the time stamps relative to the previous transaction. Only available when Time-Stamps are shown (see above). ▪ **Set Zero Time** – Enables you to set a log record to zero. Subsequent log records are relative to this new zero time record. ▪ **Reset to Zero Time** – Resets the initial record in the active log in the ACA Trace window to zero.

7.3 Monitoring the Auxiliary Channels with the Aux Channel Analyzer utilities

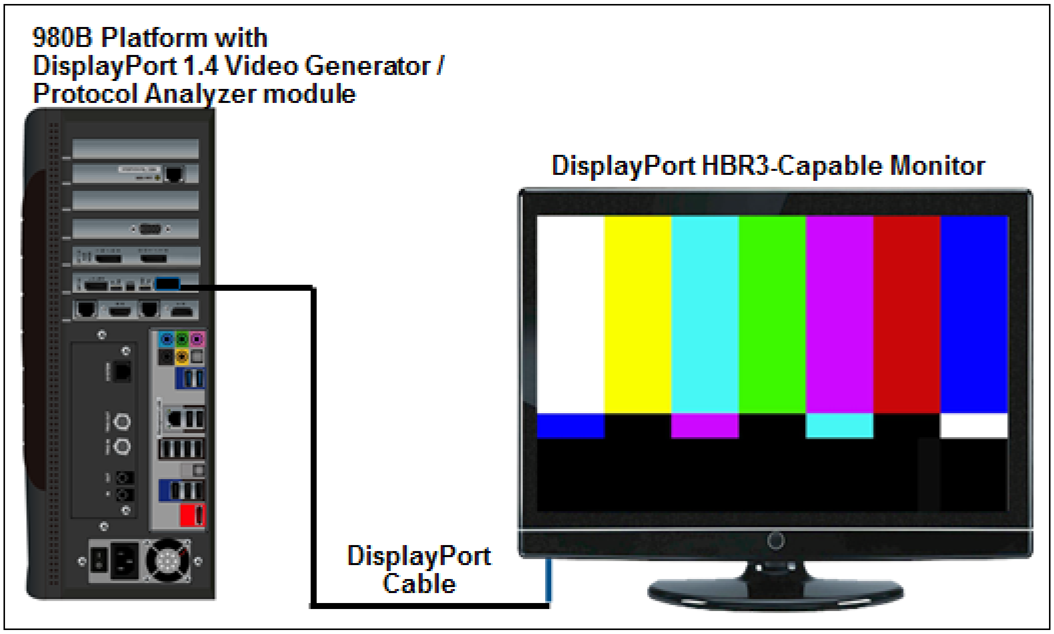
This subsection describes the procedures for monitoring the auxiliary channel data through the 980 GUI Manager using the Aux Channel Analyzer real time utilities—both the **Aux Channel Analyzer** utility through the *embedded* 980 GUI Manager or the **ACA Remote Control** utility available through the *external* 980 GUI Manager. You can monitor the DisplayPort transactions in real time when module is emulating a DisplayPort source device. If you have the DisplayPort Rx Analyzer port you can emulate a DisplayPort sink device to test a DisplayPort source device.

You can also optionally monitor the Aux Channel Transactions passively between a DP source and a DP sink with the Auxiliary DisplayPort module that is equipped with all DisplayPort 1.4 modules. You will need to use the custom capable provided with the passive monitoring option.

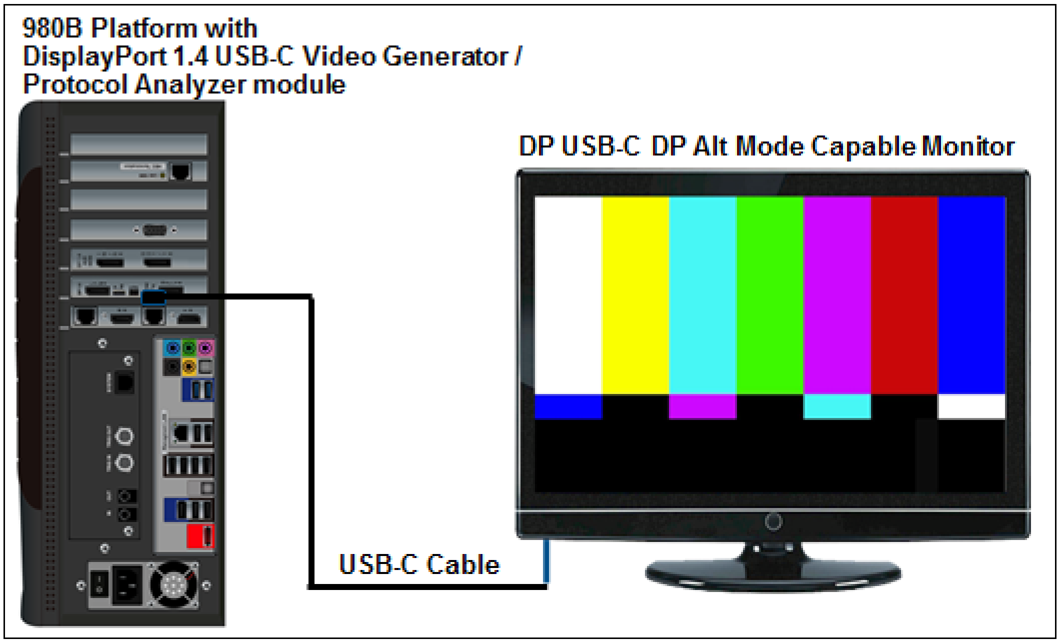
7.3.1 Making the physical connections

This subsection describes how to make the proper physical connections between the 980 module supporting the ACA features and the device under test. The following diagrams depict the test setups for testing a DisplayPort display device and a DisplayPort source device. The operation of the ACA is the same when testing a source or a sink.

1. Connect the DisplayPort display device under test to one of the DisplayPort module’s Tx ports as shown below (first example is showing monitoring the standard DP Tx port).

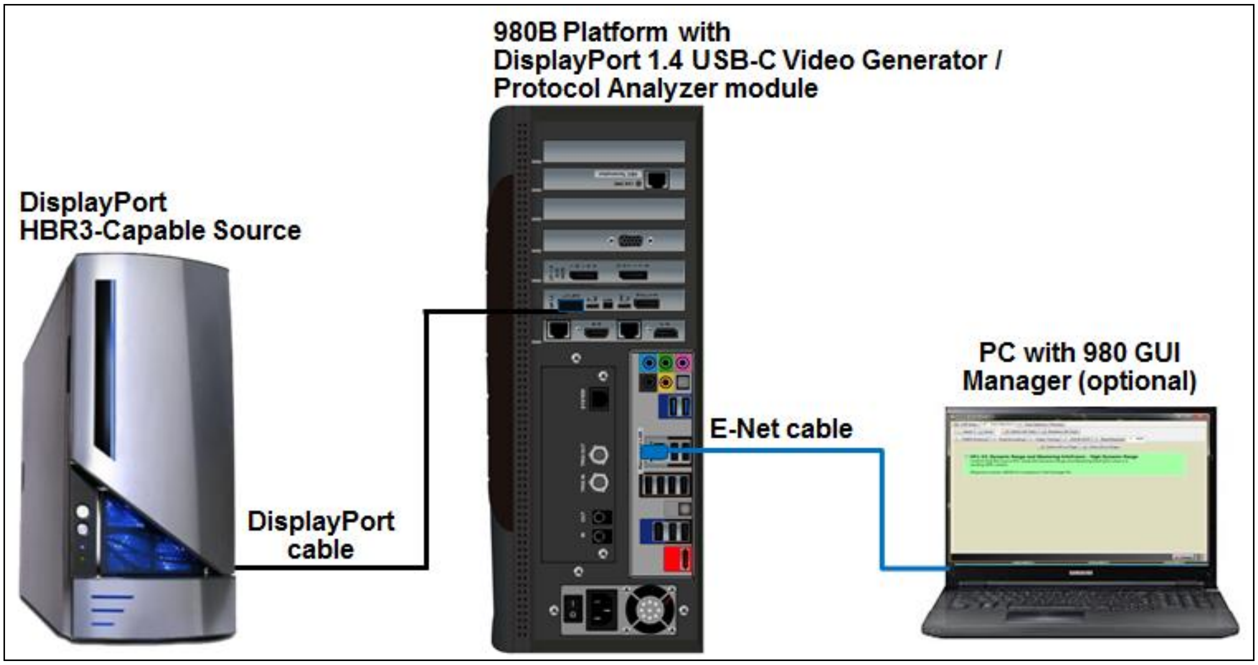


Connection for testing a DP display while DP Video Generator is emulating a DP source device



Connection for testing a USB-C DP Alt Mode display while DP Video Generator is emulating a USB-C DP Alt Mode source

2. Connect the DisplayPort source device under test to the DisplayPort module’s Rx port as shown below.



Connection for testing a DP source while DP Analyzer is emulating a sink emulation – 980B

3. Connect the DisplayPort source device to the Aux Channel module port labeled Aux IN RX using the custom cable. Connect the DisplayPort display device under test to the port labeled Aux OUT TX as shown below.

7.3.2 Monitoring the DisplayPort Aux Channel Transactions in Real Time with the ACA Utilities

Use the following procedures to monitor the DisplayPort Aux Chan transactions with a DisplayPort device in real time. The procedures assume that the DP device under test is powered up and connected to one of the 980 DP Video Generator / Analyzer ports. The operation of the ACA is the same when testing a source or a sink.

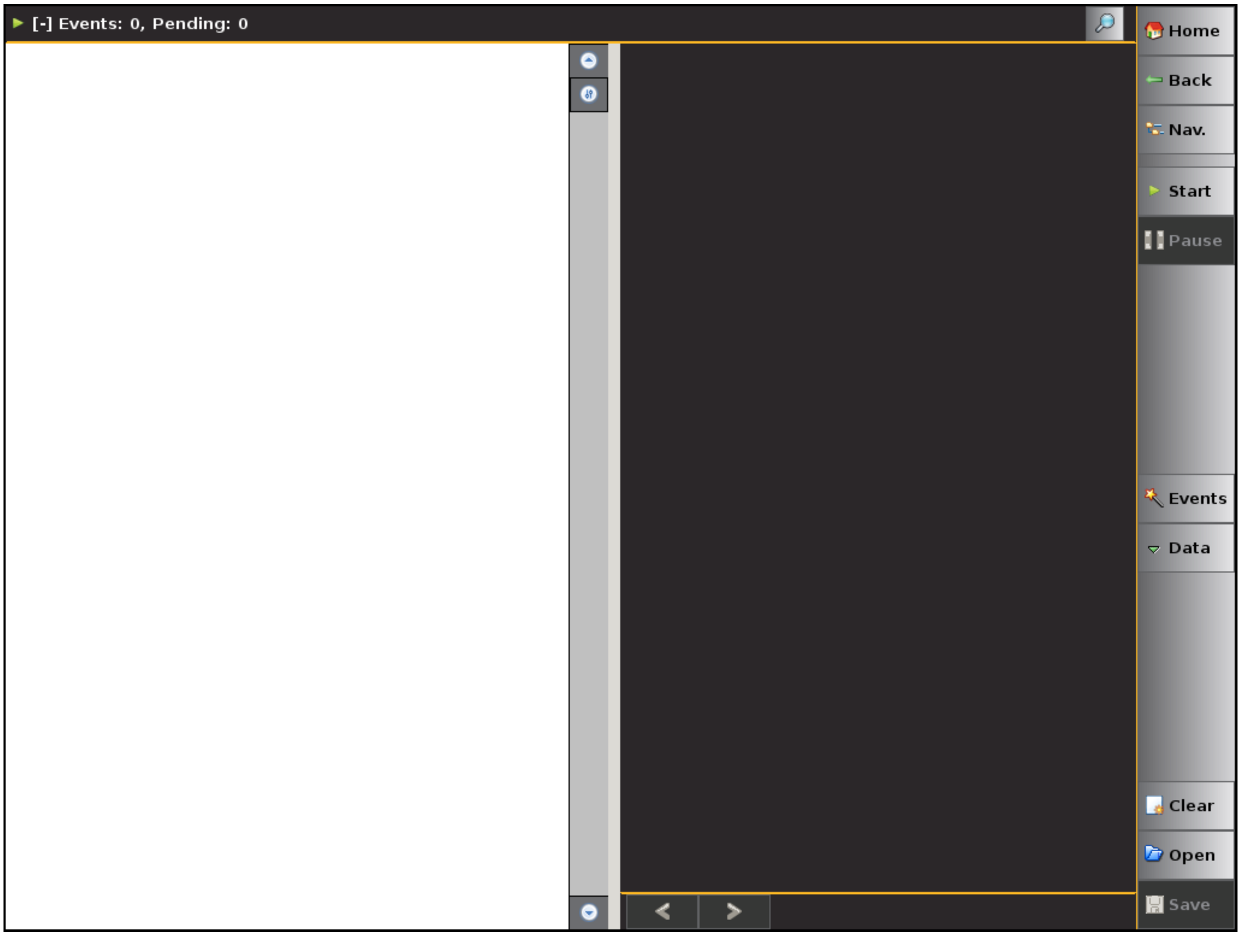
The operation of the two ACA real time utilities—**Aux Channel Analyzer** on the *embedded* 980 GUI and the **ACA Remote Control** on the *external* 980 GUI Manager-- is similar. The screen examples used in this subsection are from the **ACA Remote Control** utility on the *external* 980 GUI Manager exceptions related to the operation of the ACA on the embedded 980 GUI Manager are noted.

Important Note: You can filter and search through the ACA traces. Procedures for searching and sorting are provided in a separate subsection further below.

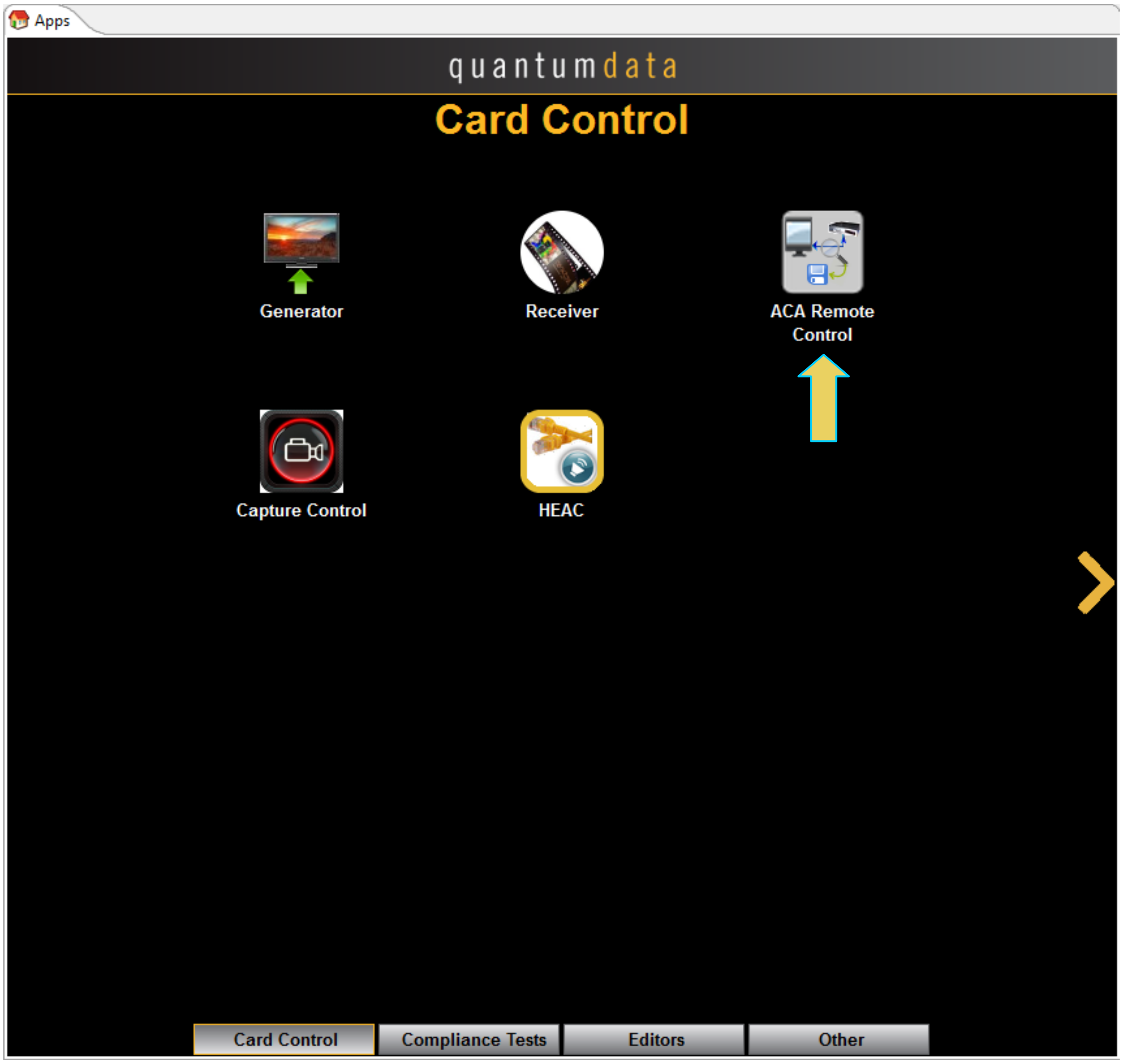
To monitor the DisplayPort transactions:

1. For the *embedded* ACA utility, touch select the **Aux Channel Analyzer** on the page 1 (Card Control) of the **Apps** panel:

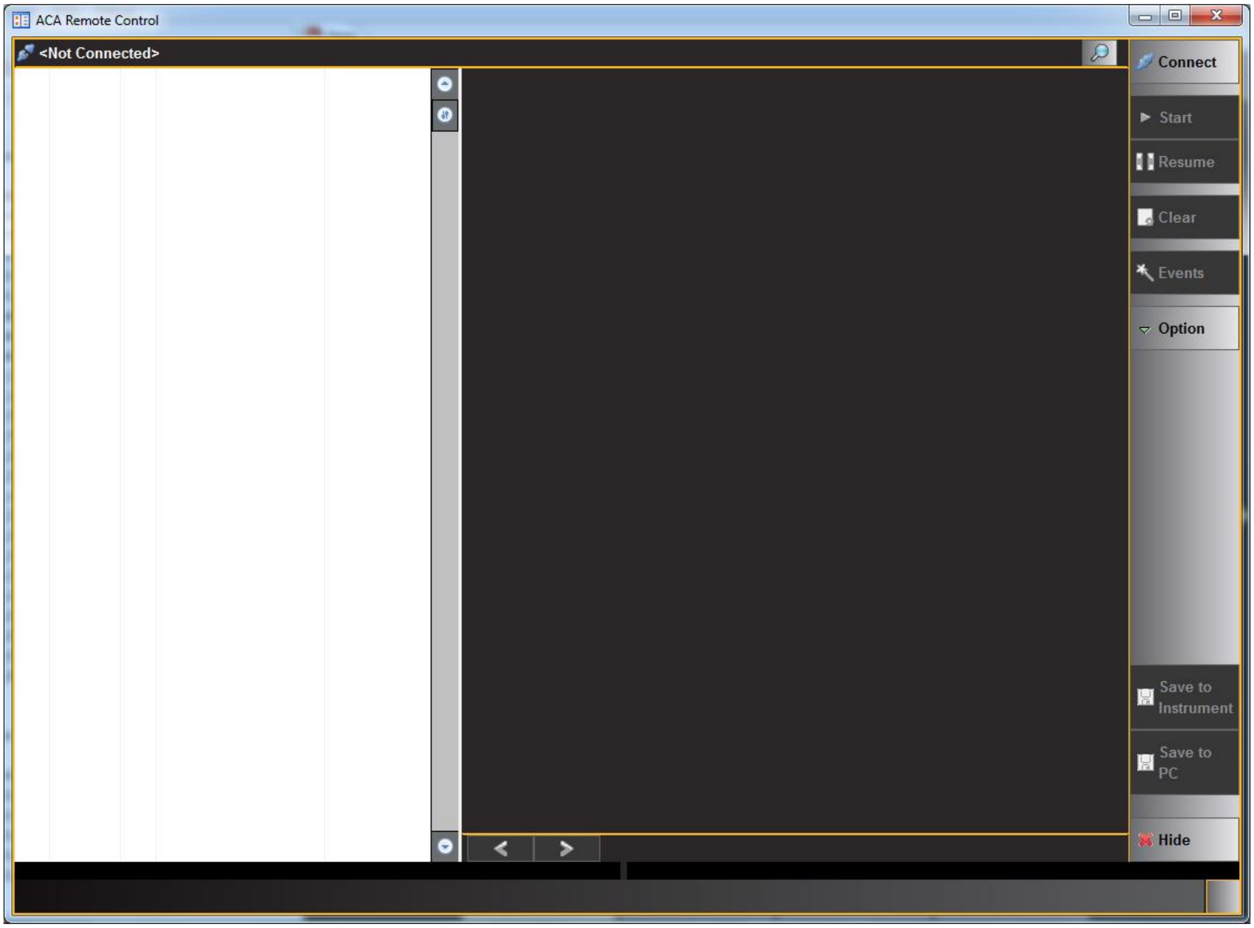
The **Aux Channel Analyzer** panel appears as shown below:



2. For the *embedded* ACA utility, touch select the **Aux Channel Analyzer** on the page 1 (Card Control) of the **Apps** panel:


Apps
quantumdata
Card Control
Generator
Receiver
ACA Remote Control
Capture Control
HEAC
Card Control
Compliance Tests
Editors
Other

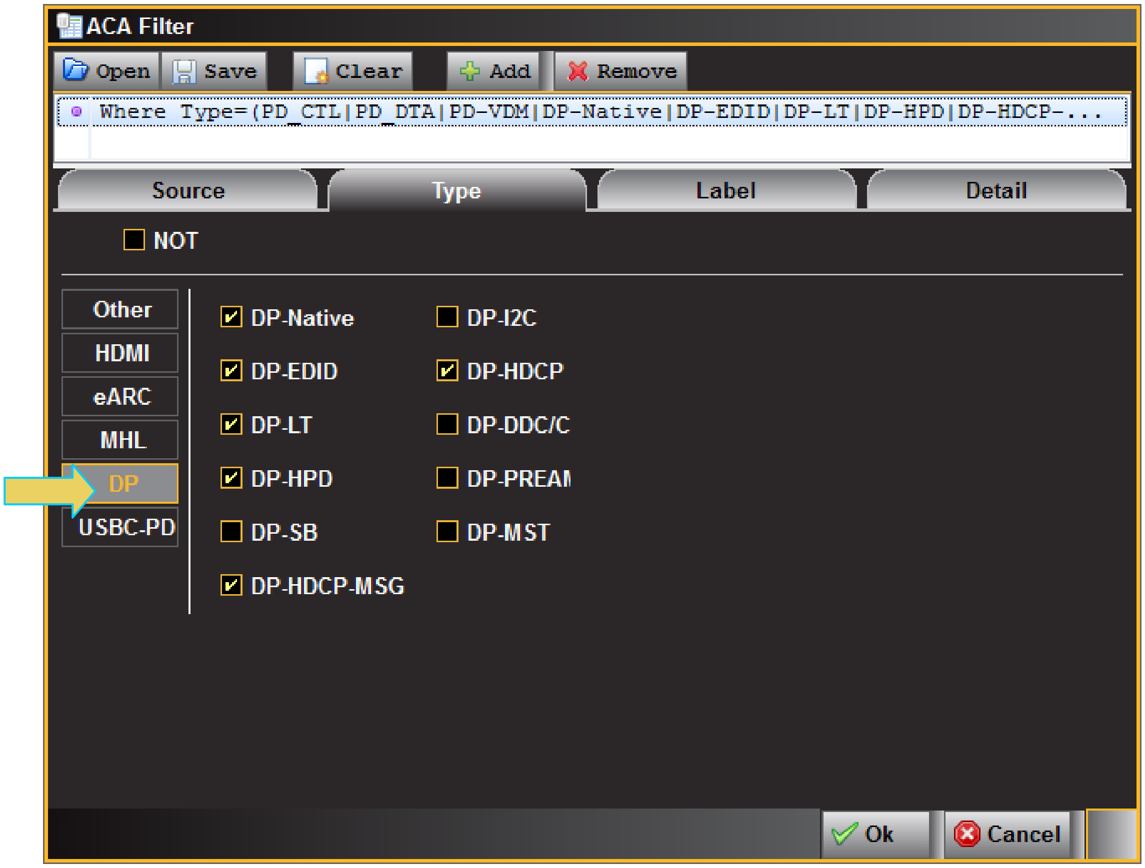
The **ACA Remote Control** panel appears as shown below:



For the **ACA Remote Control** panel you will have to connect to a 980 Instrument that you have provisioned in the external 980 GUI Manager application. The **ACA Remote Control** dialog box will appear showing all the 980 systems you have provisioned in the 980 GUI Manger. Typically you will only have one 980 system provisioned in the application, so you will simply select your lone 980 system and click the **OK** button on the dialog box.

The **ACA Event Selection** dialog box is shown below.

Specify which DP events you wish to monitor. You can select **All Events** of any set of individual events.



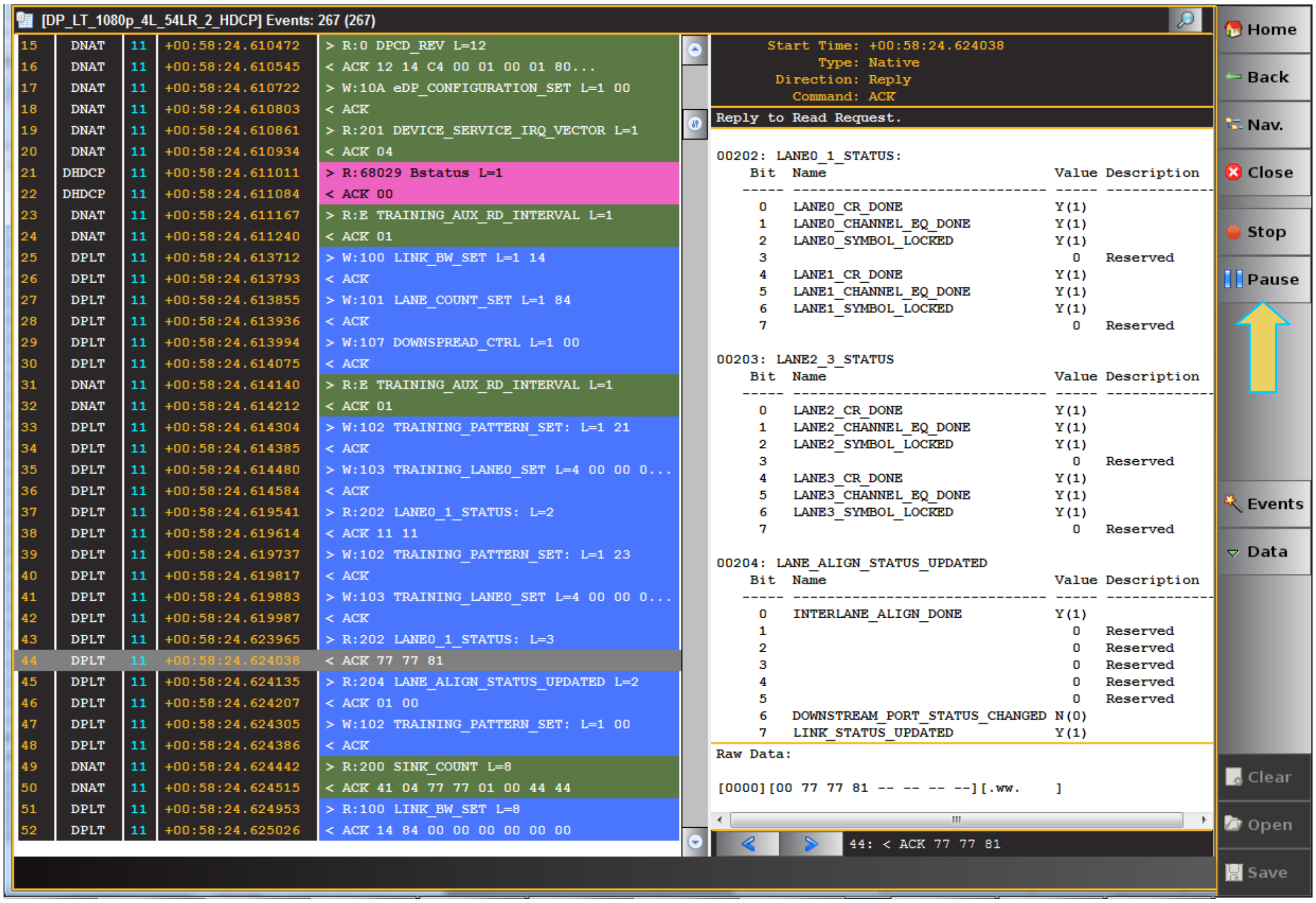
```
Where Type=(PD_CTL|PD_DTA|PD-VDM|DP-Native|DP-EDID|DP-LT|DP-HPD|DP-HDCP-...
```

☐ NOT

☑ DP-Native
☑ DP-EDID
☑ DP-LT
☑ DP-HPD
☐ DP-SB
☑ DP-HDCP-MSG
☐ DP-I2C
☑ DP-HDCP
☐ DP-DDC/C
☐ DP-PREAI
☐ DP-MST

Take the necessary action—such as a hot plug—to initiate EDID, HDCP or Link Training transactions. You will see the Aux Chan transactions in the ACA panel as shown below.

3. Touch select the **Start** button on the ACA Menu panel on the right to initiate the viewing of the DP Aux Chan transactions. An example showing monitored data is shown below. You can stop or pause the collection at any time using the buttons on the ACA menu panel on the right. These are indicated in the screen example below.

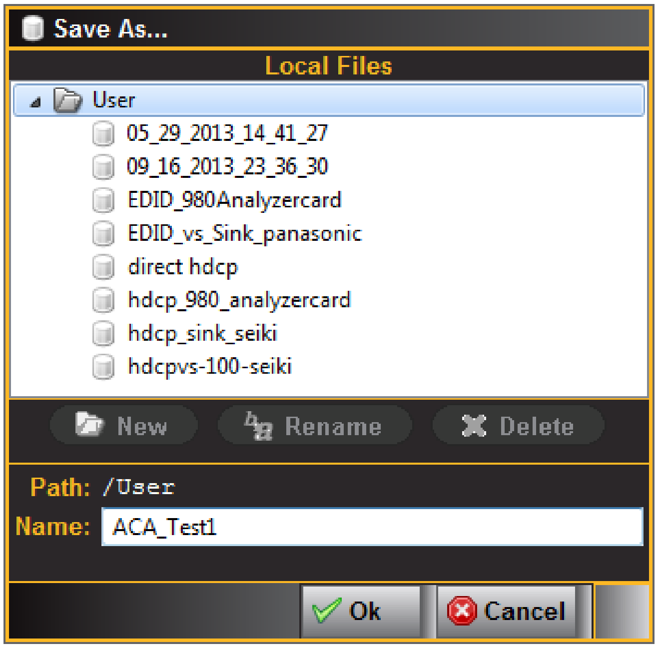


```
[DP_LT_1080p_4L_54LR_2_HDCP] Events: 267 (267)
15  DNAT   11  +00:58:24.610472  > R:0 DPCD_REV L=12
16  DNAT   11  +00:58:24.610545  < ACK 12 14 C4 00 01 00 01 80...
17  DNAT   11  +00:58:24.610722  > W:10A eDP_CONFIGURATION_SET L=1 00
18  DNAT   11  +00:58:24.610803  < ACK
19  DNAT   11  +00:58:24.610861  > R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
20  DNAT   11  +00:58:24.610934  < ACK 04
21  DHDCP  11  +00:58:24.611011  > R:68029 Bstatus L=1
22  DHDCP  11  +00:58:24.611084  < ACK 00
23  DNAT   11  +00:58:24.611167  > R:E TRAINING_AUX_RD_INTERVAL L=1
24  DNAT   11  +00:58:24.611240  < ACK 01
25  DPLT   11  +00:58:24.613712  > W:100 LINK_BW_SET L=1 14
26  DPLT   11  +00:58:24.613793  < ACK
27  DPLT   11  +00:58:24.613855  > W:101 LANE_COUNT_SET L=1 84
28  DPLT   11  +00:58:24.613936  < ACK
29  DPLT   11  +00:58:24.613994  > W:107 DOWNSPREAD_CTRL L=1 00
30  DPLT   11  +00:58:24.614075  < ACK
31  DNAT   11  +00:58:24.614140  > R:E TRAINING_AUX_RD_INTERVAL L=1
32  DNAT   11  +00:58:24.614212  < ACK 01
33  DPLT   11  +00:58:24.614304  > W:102 TRAINING_PATTERN_SET: L=1 21
34  DPLT   11  +00:58:24.614385  < ACK
35  DPLT   11  +00:58:24.614480  > W:103 TRAINING_LANE0_SET L=4 00 00 0...
36  DPLT   11  +00:58:24.614584  < ACK
37  DPLT   11  +00:58:24.619541  > R:202 LANE0_1_STATUS: L=2
38  DPLT   11  +00:58:24.619614  < ACK 11 11
39  DPLT   11  +00:58:24.619737  > W:102 TRAINING_PATTERN_SET: L=1 23
40  DPLT   11  +00:58:24.619817  < ACK
41  DPLT   11  +00:58:24.619883  > W:103 TRAINING_LANE0_SET L=4 00 00 0...
42  DPLT   11  +00:58:24.619987  < ACK
43  DPLT   11  +00:58:24.623965  > R:202 LANE0_1_STATUS: L=3
44  DPLT   11  +00:58:24.624038  < ACK 77 77 81
45  DPLT   11  +00:58:24.624135  > R:204 LANE_ALIGN_STATUS_UPDATED L=2
46  DPLT   11  +00:58:24.624207  < ACK 01 00
47  DPLT   11  +00:58:24.624305  > W:102 TRAINING_PATTERN_SET: L=1 00
48  DPLT   11  +00:58:24.624386  < ACK
49  DNAT   11  +00:58:24.624442  > R:200 SINK_COUNT L=8
50  DNAT   11  +00:58:24.624515  < ACK 41 04 77 77 01 00 44 44
51  DPLT   11  +00:58:24.624953  > R:100 LINK_BW_SET L=8
52  DPLT   11  +00:58:24.625026  < ACK 14 84 00 00 00 00 00 00
```

```
 Start Time: +00:58:24.624038
       Type: Native
  Direction: Reply
    Command: ACK
Reply to Read Request.

00202: LANE0_1_STATUS:
   Bit  Name                            Value Description
  ----- ------------------------------- ----- ------------
    0   LANE0_CR_DONE                   Y(1)
    1   LANE0_CHANNEL_EQ_DONE           Y(1)
    2   LANE0_SYMBOL_LOCKED             Y(1)
    3                                     0   Reserved
    4   LANE1_CR_DONE                   Y(1)
    5   LANE1_CHANNEL_EQ_DONE           Y(1)
    6   LANE1_SYMBOL_LOCKED             Y(1)
    7                                     0   Reserved

00203: LANE2_3_STATUS
   Bit  Name                            Value Description
  ----- ------------------------------- ----- ------------
    0   LANE2_CR_DONE                   Y(1)
    1   LANE2_CHANNEL_EQ_DONE           Y(1)
    2   LANE2_SYMBOL_LOCKED             Y(1)
    3                                     0   Reserved
    4   LANE3_CR_DONE                   Y(1)
    5   LANE3_CHANNEL_EQ_DONE           Y(1)
    6   LANE3_SYMBOL_LOCKED             Y(1)
    7                                     0   Reserved

00204: LANE_ALIGN_STATUS_UPDATED
   Bit  Name                            Value Description
  ----- ------------------------------- ----- ------------
    0   INTERLANE_ALIGN_DONE            Y(1)
    1                                     0   Reserved
    2                                     0   Reserved
    3                                     0   Reserved
    4                                     0   Reserved
    5                                     0   Reserved
    6   DOWNSTREAM_PORT_STATUS_CHANGED N(0)
    7   LINK_STATUS_UPDATED             Y(1)
Raw Data:

[0000][00 77 77 81 -- -- -- --][.ww.    ]

44: < ACK 77 77 81
```

Important Note: You can filter and search through the ACA traces. Procedures for searching and sorting are provided in a separate subsection further below.

4. Click on **Save to Instrument** or **Save to PC** depending on whether you are working with the external ACA Remote Control utility or the embedded Aux Channel Analyzer. A dialog box appears (below). Enter a name and then click on **OK**.

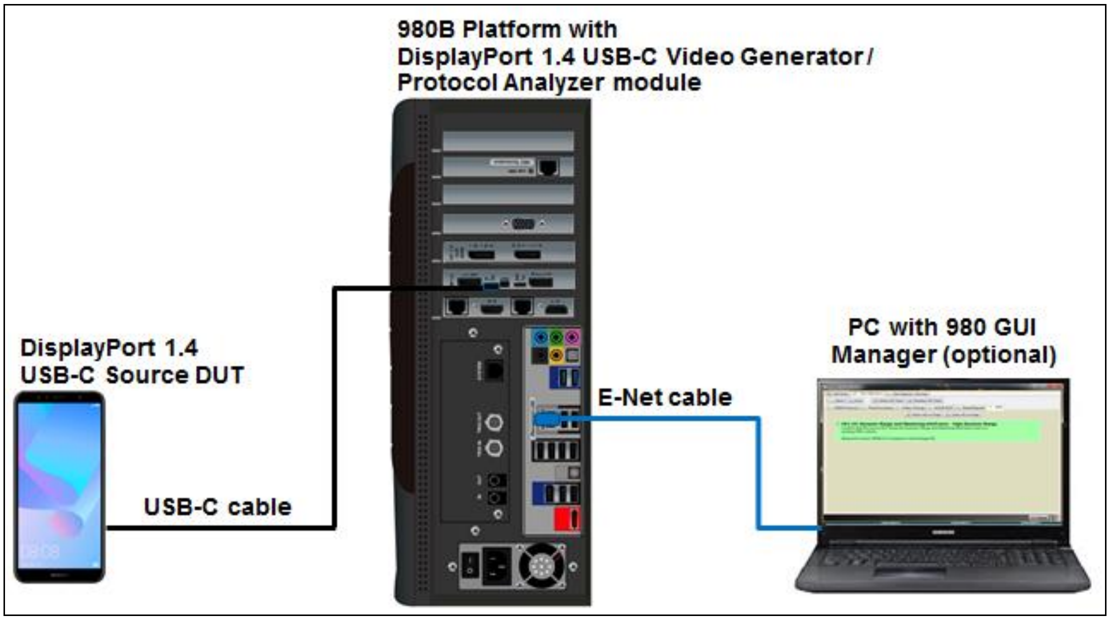


User
05_29_2013_14_41_27
09_16_2013_23_36_30
EDID_980Analyzercard
EDID_vs_Sink_panasonic
direct hdcp
hdcp_980_analyzercard
hdcp_sink_seiki
hdcpvs-100-seiki

Path: /User
Name: ACA_Test1

Please note that in order to use the **ACA Data Viewer** utility (next subsection) on your PC to view the traces or the ACA viewer on the 980 embedded display with the powerful searching and filtering features, you must save the file. If you are working on the embedded **Aux Channel Analyzer** viewer but prefer to use **ACA Data Viewer** on the external 980 GUI Manager, you will have to transfer the saved file to your PC using the external 980 GUI Manager.

7.4 Monitoring USB-C DP Alt Mode Protocol Negotiation Transactions



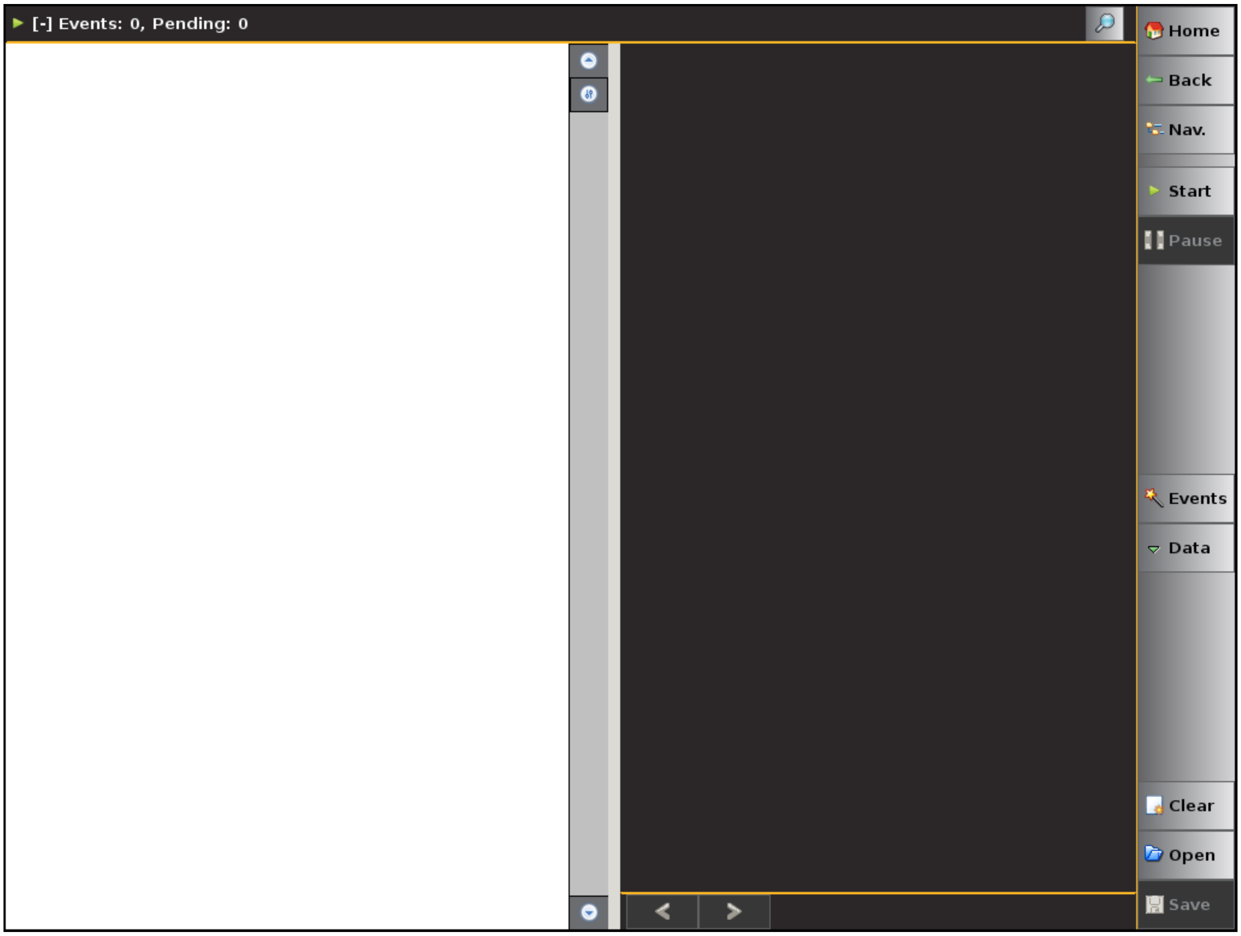
Connection for Testing a DP USB-C DP Alt Mode Source with DP Analyzer Emulating a USB-C DP Alt Mode Sink – 980B

You can monitor the USB-C Power Delivery (PD) protocol negotiations into DP Alt Mode in the 980 Auxiliary Channel Analyzer (ACA). Use the following procedures to view the PD negotiations.

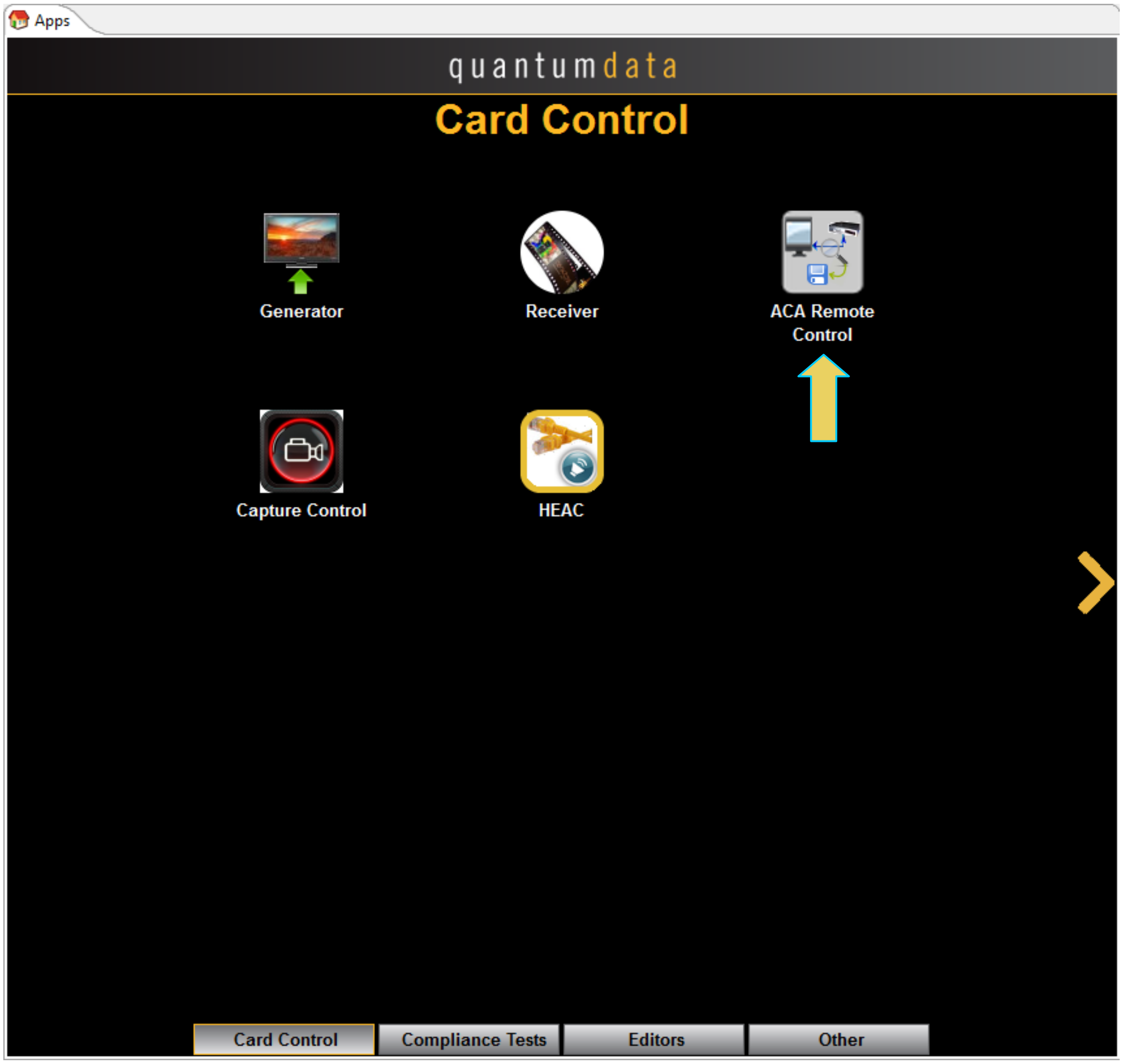
To monitor the USB-C DP Alt Mode transactions:

1. For the *embedded* ACA utility, touch select the **Aux Channel Analyzer** on the page 1 (Card Control) of the **Apps** panel:

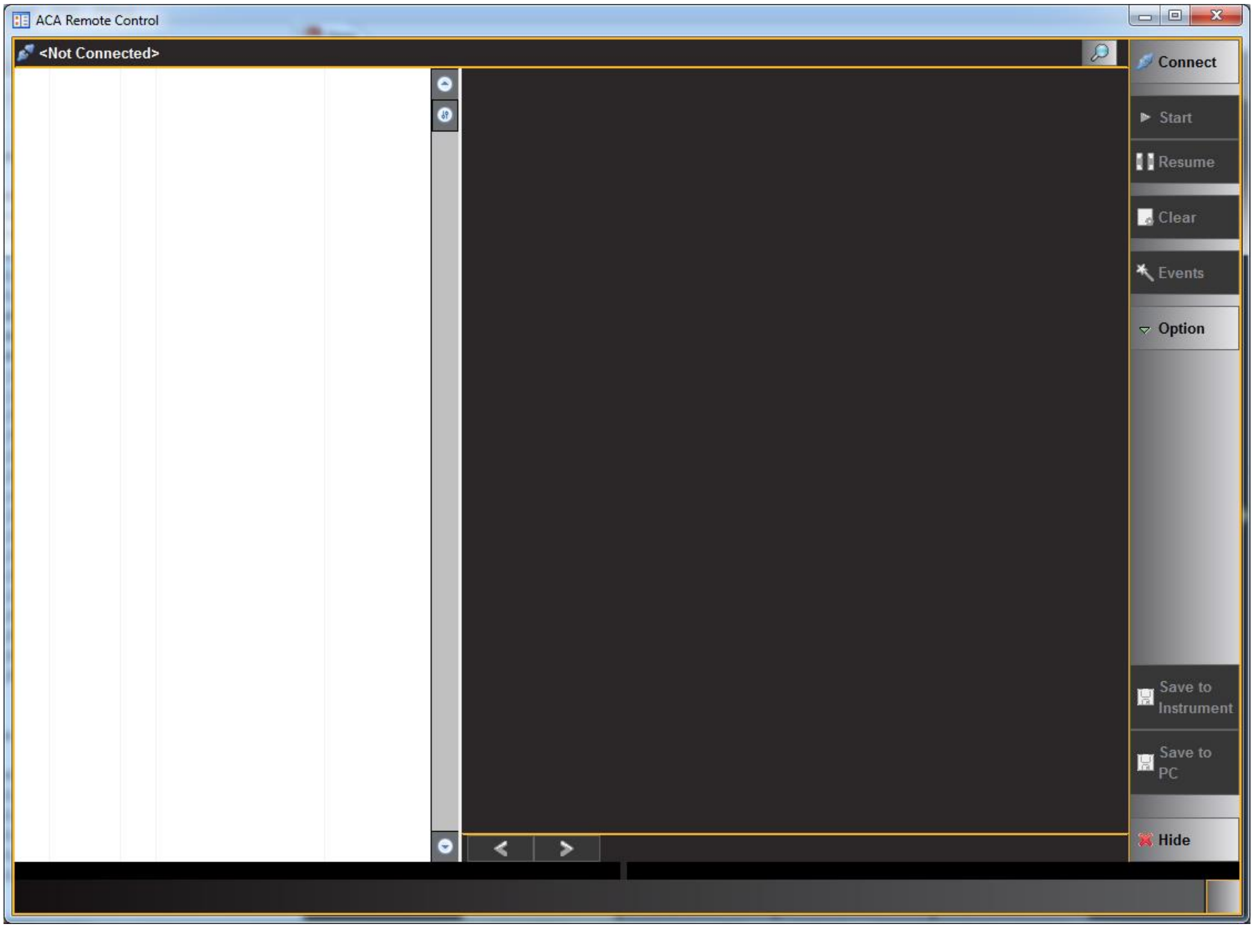
The **Aux Channel Analyzer** panel appears as shown below:



2. For the *embedded* ACA utility, touch select the **Aux Channel Analyzer** on the page 1 (Card Control) of the **Apps** panel:

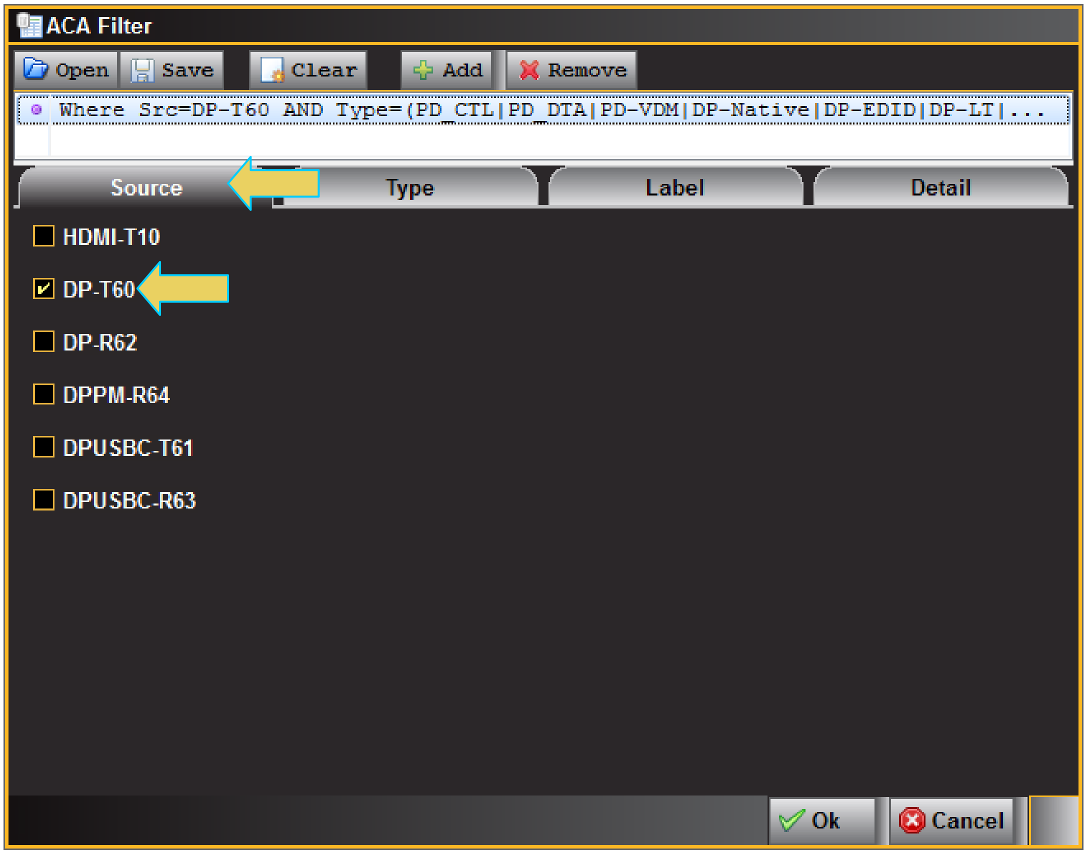

Apps
quantumdata
Card Control
Generator
Receiver
ACA Remote Control
Capture Control
HEAC
Card Control
Compliance Tests
Editors
Other

The **ACA Remote Control** panel appears as shown below:



For the **ACA Remote Control** panel you will have to connect to a 980 Instrument that you have provisioned in the external 980 GUI Manager application. The **ACA Remote Control** dialog box will appear showing all the 980 systems you have provisioned in the 980 GUI Manger. Typically you will only have one 980 system provisioned in the application, so you will simply select your lone 980 system and click the **OK** button on the dialog box.

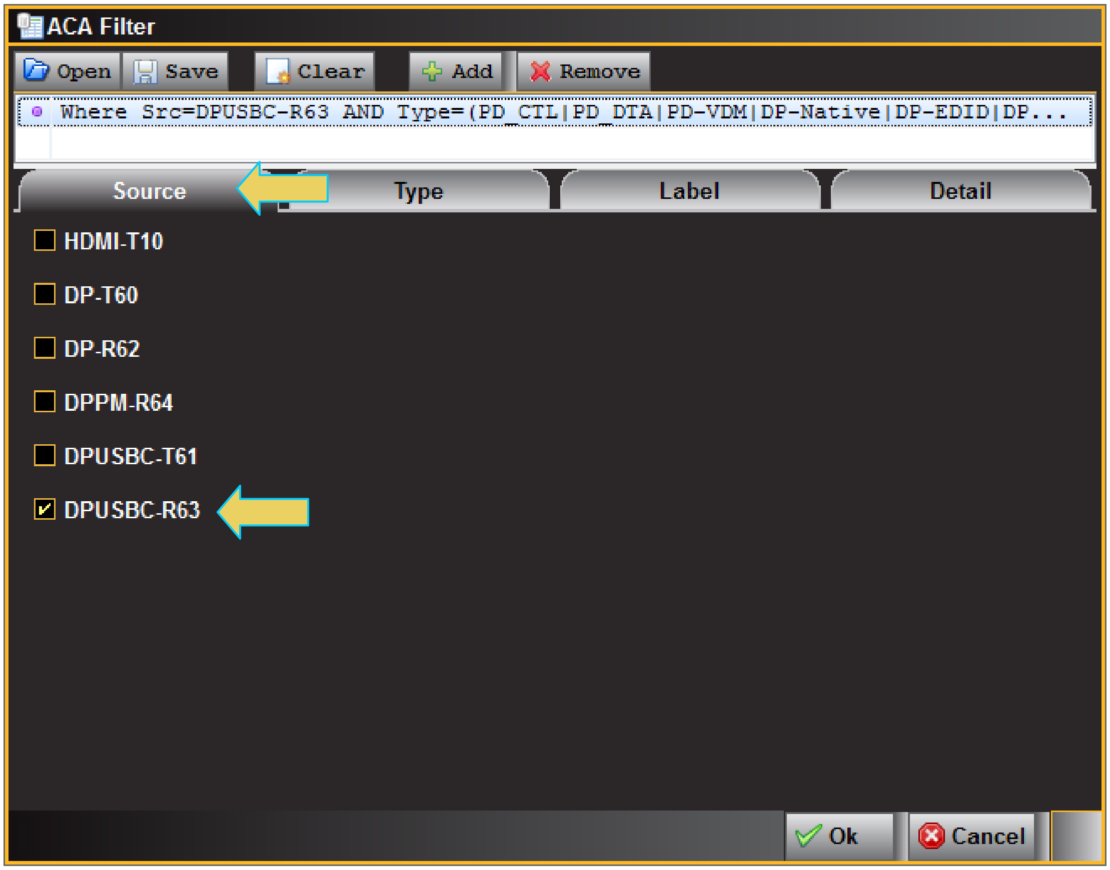
3. From the **Events** button on the ACA panel, select the DP module's port that you are monitoring using the pull-down menu. Refer to the screen examples below. You first select the Source tab to specify which 980 interface you wish to monitor with the ACA. In the first example below, the DP standard Tx port is selected.



`Where Src=DP-T60 AND Type=(PD_CTL|PD_DTA|PD-VDM|DP-Native|DP-EDID|DP-LT|...`

☐ HDMI-T10
☑ DP-T60
☐ DP-R62
☐ DPPM-R64
☐ DPUSBC-T61
☐ DPUSBC-R63

In the following example the USB-C DP Rx port is selected.

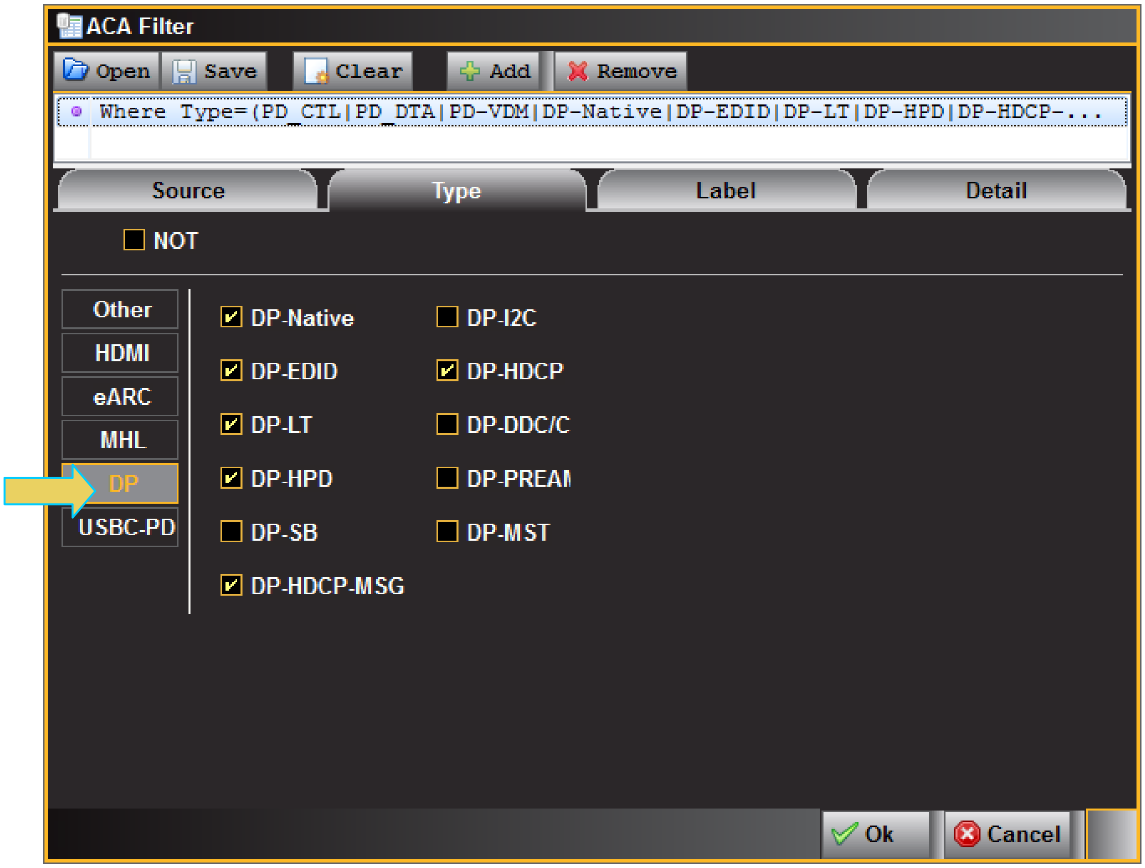


```
Where Src=DPUSBC-R63 AND Type=(PD_CTL|PD_DTA|PD-VDM|DP-Native|DP-EDID|DP...
```

- ☐ HDMI-T10
- ☐ DP-T60
- ☐ DP-R62
- ☐ DPPM-R64
- ☐ DPUSBC-T61
- ☑ DPUSBC-R63

The **ACA Event Selection** dialog box is shown below.

Specify which DP events you wish to monitor. You can select **All Events** of any set of individual events.



`Where Type=(PD_CTL|PD_DTA|PD-VDM|DP-Native|DP-EDID|DP-LT|DP-HPD|DP-HDCP-...`

☐ NOT

☑ DP-Native ☐ DP-I2C

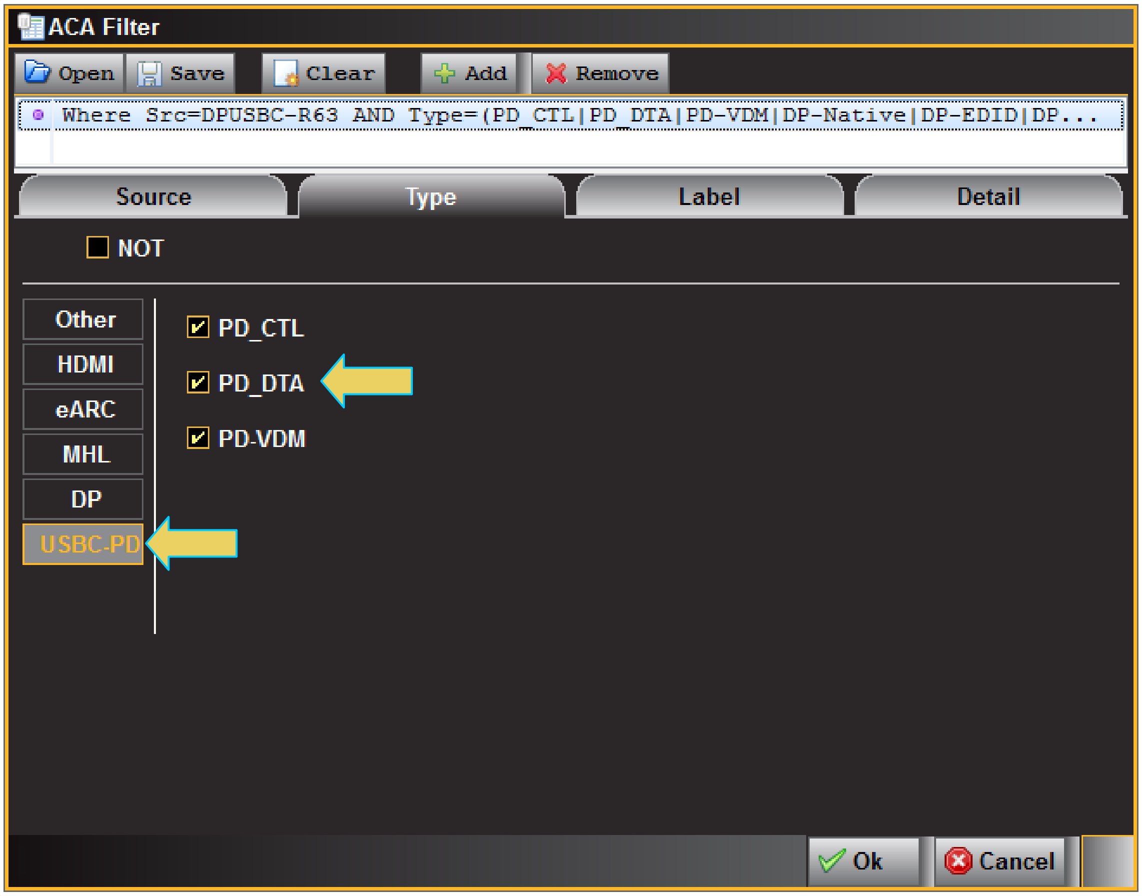
☑ DP-EDID ☑ DP-HDCP

☑ DP-LT ☐ DP-DDC/C

☑ DP-HPD ☐ DP-PREAI

☐ DP-SB ☐ DP-MST

☑ DP-HDCP-MSG



Where Src=DPUSBC-R63 AND Type=(PD_CTL|PD_DTA|PD-VDM|DP-Native|DP-EDID|DP...

☐ NOT

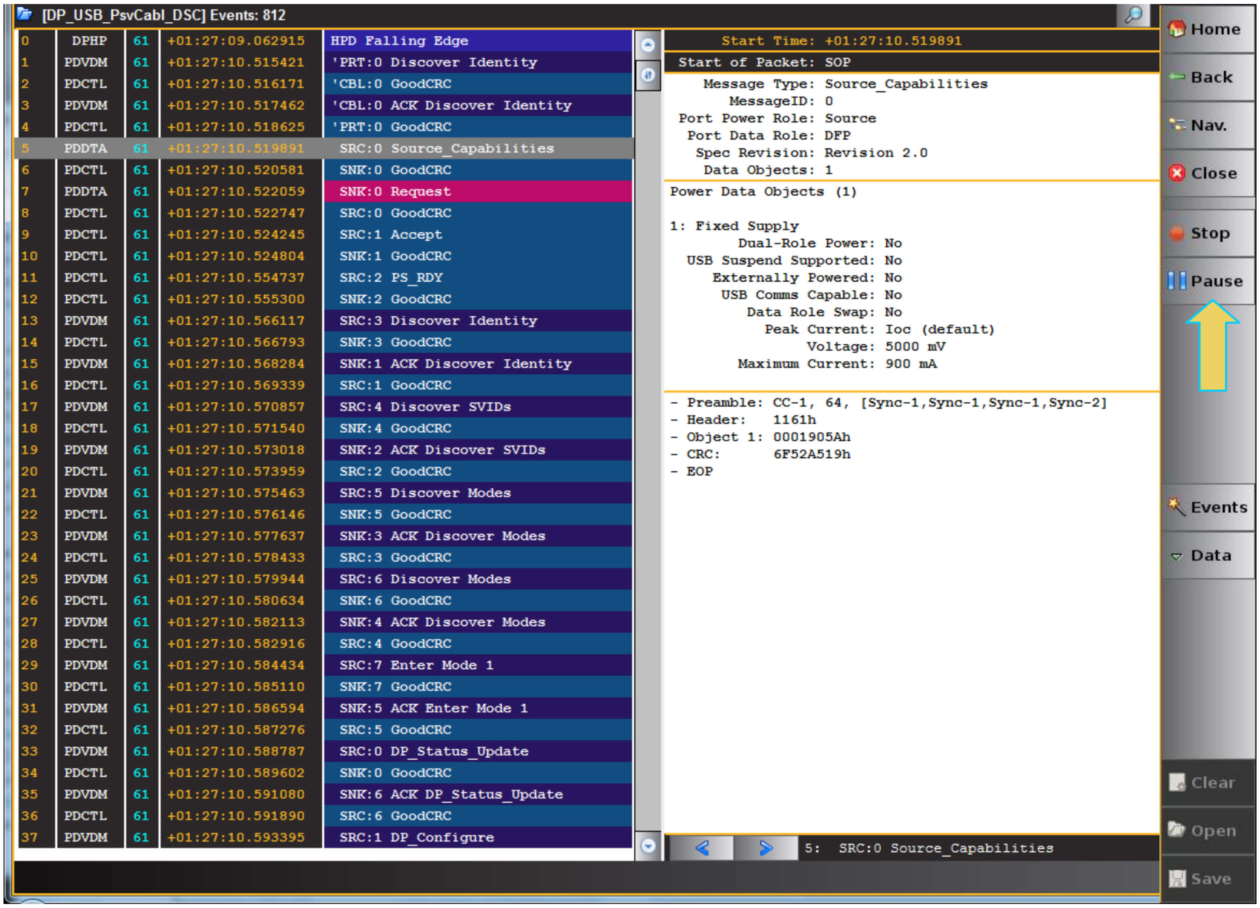
☑ PD_CTL

☑ PD_DTA

☑ PD-VDM

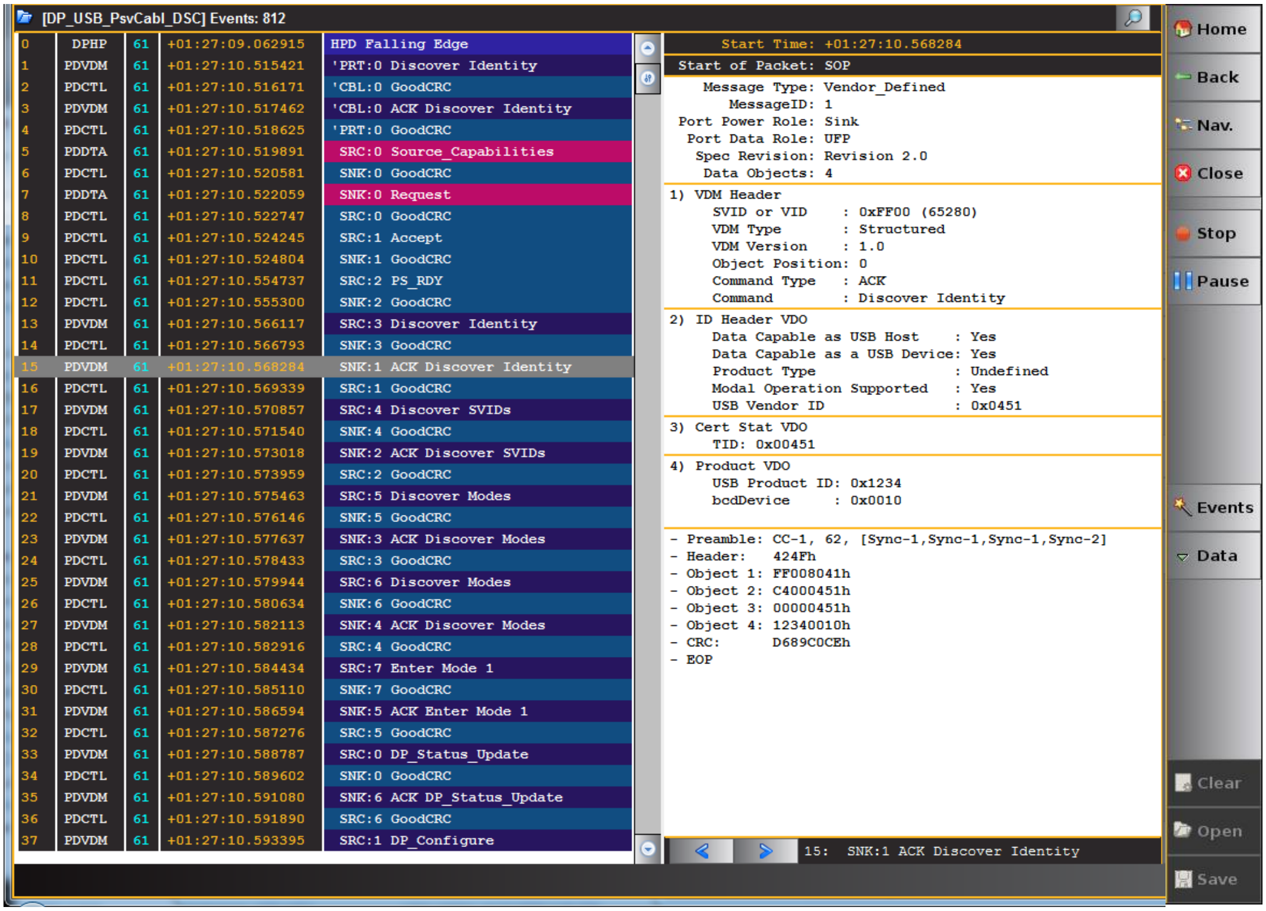
Take the necessary action—such as a hot plug—to initiate EDID, HDCP or Link Training transactions. You will see the Aux Chan transactions in the ACA panel as shown below.

4. Touch select the **Start** ▶ Start button on the ACA Menu panel on the right to initiate the viewing of the DP Aux Chan transactions. Several screen examples showing monitored PD DP Alt Mode protocol data is shown below. You can stop or pause the collection at any time using the buttons on the ACA menu panel on the right. These are indicated in the screen example below.



```
0   DPHP   61  +01:27:09.062915  HPD Falling Edge
1   PDVDM  61  +01:27:10.515421  'PRT:0 Discover Identity
2   PDCTL  61  +01:27:10.516171  'CBL:0 GoodCRC
3   PDVDM  61  +01:27:10.517462  'CBL:0 ACK Discover Identity
4   PDCTL  61  +01:27:10.518625  'PRT:0 GoodCRC
5   PDDTA  61  +01:27:10.519891   SRC:0 Source_Capabilities
6   PDCTL  61  +01:27:10.520581   SNK:0 GoodCRC
7   PDDTA  61  +01:27:10.522059   SNK:0 Request
8   PDCTL  61  +01:27:10.522747   SRC:0 GoodCRC
9   PDCTL  61  +01:27:10.524245   SRC:1 Accept
10  PDCTL  61  +01:27:10.524804   SNK:1 GoodCRC
11  PDCTL  61  +01:27:10.554737   SRC:2 PS_RDY
12  PDCTL  61  +01:27:10.555300   SNK:2 GoodCRC
13  PDVDM  61  +01:27:10.566117   SRC:3 Discover Identity
14  PDCTL  61  +01:27:10.566793   SNK:3 GoodCRC
15  PDVDM  61  +01:27:10.568284   SNK:1 ACK Discover Identity
16  PDCTL  61  +01:27:10.569339   SRC:1 GoodCRC
17  PDVDM  61  +01:27:10.570857   SRC:4 Discover SVIDs
18  PDCTL  61  +01:27:10.571540   SNK:4 GoodCRC
19  PDVDM  61  +01:27:10.573018   SNK:2 ACK Discover SVIDs
20  PDCTL  61  +01:27:10.573959   SRC:2 GoodCRC
21  PDVDM  61  +01:27:10.575463   SRC:5 Discover Modes
22  PDCTL  61  +01:27:10.576146   SNK:5 GoodCRC
23  PDVDM  61  +01:27:10.577637   SNK:3 ACK Discover Modes
24  PDCTL  61  +01:27:10.578433   SRC:3 GoodCRC
25  PDVDM  61  +01:27:10.579944   SRC:6 Discover Modes
26  PDCTL  61  +01:27:10.580634   SNK:6 GoodCRC
27  PDVDM  61  +01:27:10.582113   SNK:4 ACK Discover Modes
28  PDCTL  61  +01:27:10.582916   SRC:4 GoodCRC
29  PDVDM  61  +01:27:10.584434   SRC:7 Enter Mode 1
30  PDCTL  61  +01:27:10.585110   SNK:7 GoodCRC
31  PDVDM  61  +01:27:10.586594   SNK:5 ACK Enter Mode 1
32  PDCTL  61  +01:27:10.587276   SRC:5 GoodCRC
33  PDVDM  61  +01:27:10.588787   SRC:0 DP_Status_Update
34  PDCTL  61  +01:27:10.589602   SNK:0 GoodCRC
35  PDVDM  61  +01:27:10.591080   SNK:6 ACK DP_Status_Update
36  PDCTL  61  +01:27:10.591890   SRC:6 GoodCRC
37  PDVDM  61  +01:27:10.593395   SRC:1 DP_Configure
```

```
      Start Time: +01:27:10.519891
 Start of Packet: SOP
    Message Type: Source_Capabilities
       MessageID: 0
 Port Power Role: Source
  Port Data Role: DFP
   Spec Revision: Revision 2.0
    Data Objects: 1
Power Data Objects (1)

1: Fixed Supply
         Dual-Role Power: No
  USB Suspend Supported: No
     Externally Powered: No
      USB Comms Capable: No
         Data Role Swap: No
           Peak Current: Ioc (default)
                Voltage: 5000 mV
        Maximum Current: 900 mA

- Preamble: CC-1, 64, [Sync-1,Sync-1,Sync-1,Sync-2]
- Header:   1161h
- Object 1: 0001905Ah
- CRC:      6F52A519h
- EOP

5:  SRC:0 Source_Capabilities
```

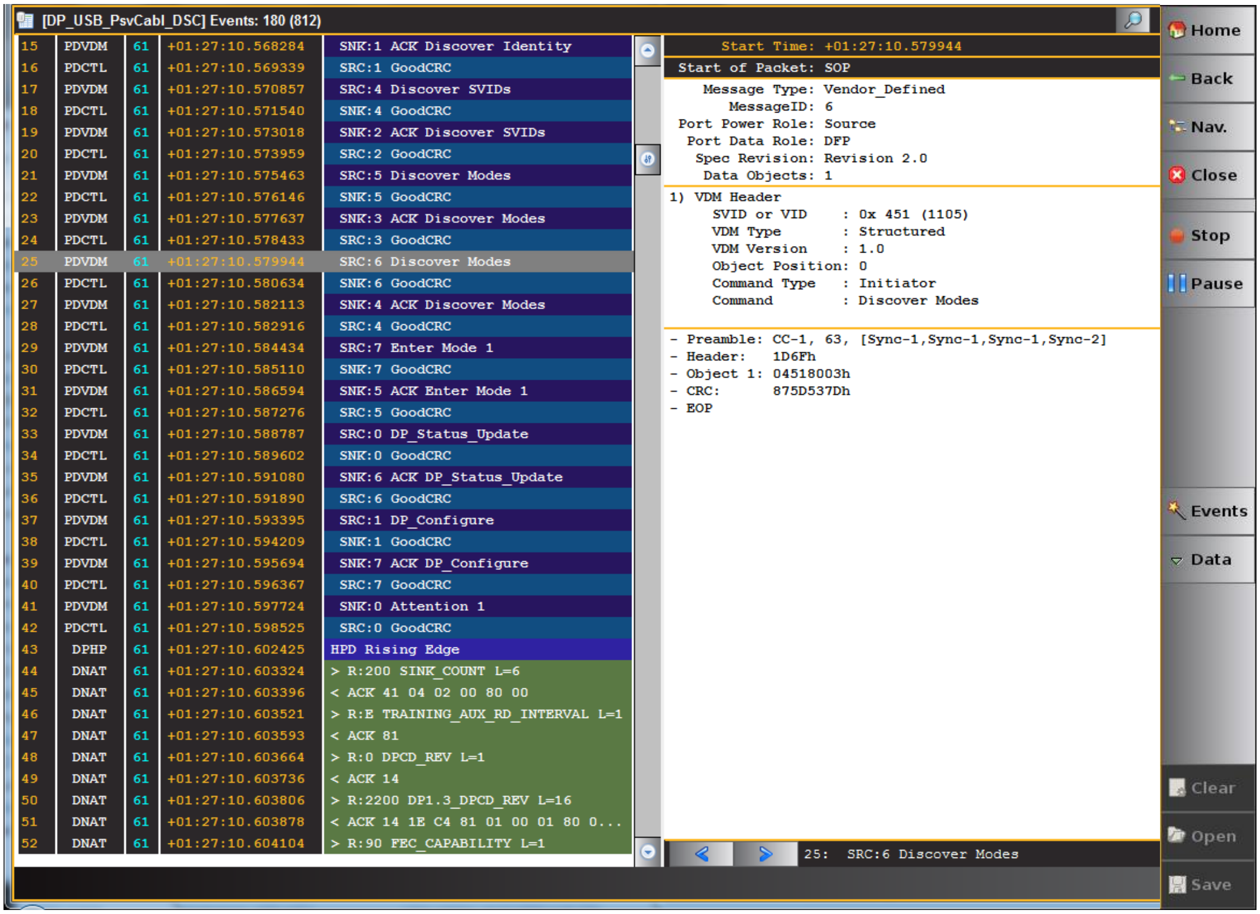


[DP_USB_PsvCabl_DSC] Events: 812

```
0    DPHP   61  +01:27:09.062915  HPD Falling Edge
1    PDVDM  61  +01:27:10.515421  'PRT:0 Discover Identity
2    PDCTL  61  +01:27:10.516171  'CBL:0 GoodCRC
3    PDVDM  61  +01:27:10.517462  'CBL:0 ACK Discover Identity
4    PDCTL  61  +01:27:10.518625  'PRT:0 GoodCRC
5    PDDTA  61  +01:27:10.519891   SRC:0 Source_Capabilities
6    PDCTL  61  +01:27:10.520581   SNK:0 GoodCRC
7    PDDTA  61  +01:27:10.522059   SNK:0 Request
8    PDCTL  61  +01:27:10.522747   SRC:0 GoodCRC
9    PDCTL  61  +01:27:10.524245   SRC:1 Accept
10   PDCTL  61  +01:27:10.524804   SNK:1 GoodCRC
11   PDCTL  61  +01:27:10.554737   SRC:2 PS_RDY
12   PDCTL  61  +01:27:10.555300   SNK:2 GoodCRC
13   PDVDM  61  +01:27:10.566117   SRC:3 Discover Identity
14   PDCTL  61  +01:27:10.566793   SNK:3 GoodCRC
15   PDVDM  61  +01:27:10.568284   SNK:1 ACK Discover Identity
16   PDCTL  61  +01:27:10.569339   SRC:1 GoodCRC
17   PDVDM  61  +01:27:10.570857   SRC:4 Discover SVIDs
18   PDCTL  61  +01:27:10.571540   SNK:4 GoodCRC
19   PDVDM  61  +01:27:10.573018   SNK:2 ACK Discover SVIDs
20   PDCTL  61  +01:27:10.573959   SRC:2 GoodCRC
21   PDVDM  61  +01:27:10.575463   SRC:5 Discover Modes
22   PDCTL  61  +01:27:10.576146   SNK:5 GoodCRC
23   PDVDM  61  +01:27:10.577637   SNK:3 ACK Discover Modes
24   PDCTL  61  +01:27:10.578433   SRC:3 GoodCRC
25   PDVDM  61  +01:27:10.579944   SRC:6 Discover Modes
26   PDCTL  61  +01:27:10.580634   SNK:6 GoodCRC
27   PDVDM  61  +01:27:10.582113   SNK:4 ACK Discover Modes
28   PDCTL  61  +01:27:10.582916   SRC:4 GoodCRC
29   PDVDM  61  +01:27:10.584434   SRC:7 Enter Mode 1
30   PDCTL  61  +01:27:10.585110   SNK:7 GoodCRC
31   PDVDM  61  +01:27:10.586594   SNK:5 ACK Enter Mode 1
32   PDCTL  61  +01:27:10.587276   SRC:5 GoodCRC
33   PDVDM  61  +01:27:10.588787   SRC:0 DP_Status_Update
34   PDCTL  61  +01:27:10.589602   SNK:0 GoodCRC
35   PDVDM  61  +01:27:10.591080   SNK:6 ACK DP_Status_Update
36   PDCTL  61  +01:27:10.591890   SRC:6 GoodCRC
37   PDVDM  61  +01:27:10.593395   SRC:1 DP_Configure
```

```
    Start Time: +01:27:10.568284
Start of Packet: SOP
   Message Type: Vendor_Defined
      MessageID: 1
Port Power Role: Sink
 Port Data Role: UFP
  Spec Revision: Revision 2.0
   Data Objects: 4
1) VDM Header
     SVID or VID    : 0xFF00 (65280)
     VDM Type       : Structured
     VDM Version    : 1.0
     Object Position: 0
     Command Type   : ACK
     Command        : Discover Identity
2) ID Header VDO
     Data Capable as USB Host    : Yes
     Data Capable as a USB Device: Yes
     Product Type                : Undefined
     Modal Operation Supported   : Yes
     USB Vendor ID               : 0x0451
3) Cert Stat VDO
     TID: 0x00451
4) Product VDO
     USB Product ID: 0x1234
     bcdDevice     : 0x0010

- Preamble: CC-1, 62, [Sync-1,Sync-1,Sync-1,Sync-2]
- Header:   424Fh
- Object 1: FF008041h
- Object 2: C4000451h
- Object 3: 00000451h
- Object 4: 12340010h
- CRC:      D689C0CEh
- EOP
```

15: SNK:1 ACK Discover Identity

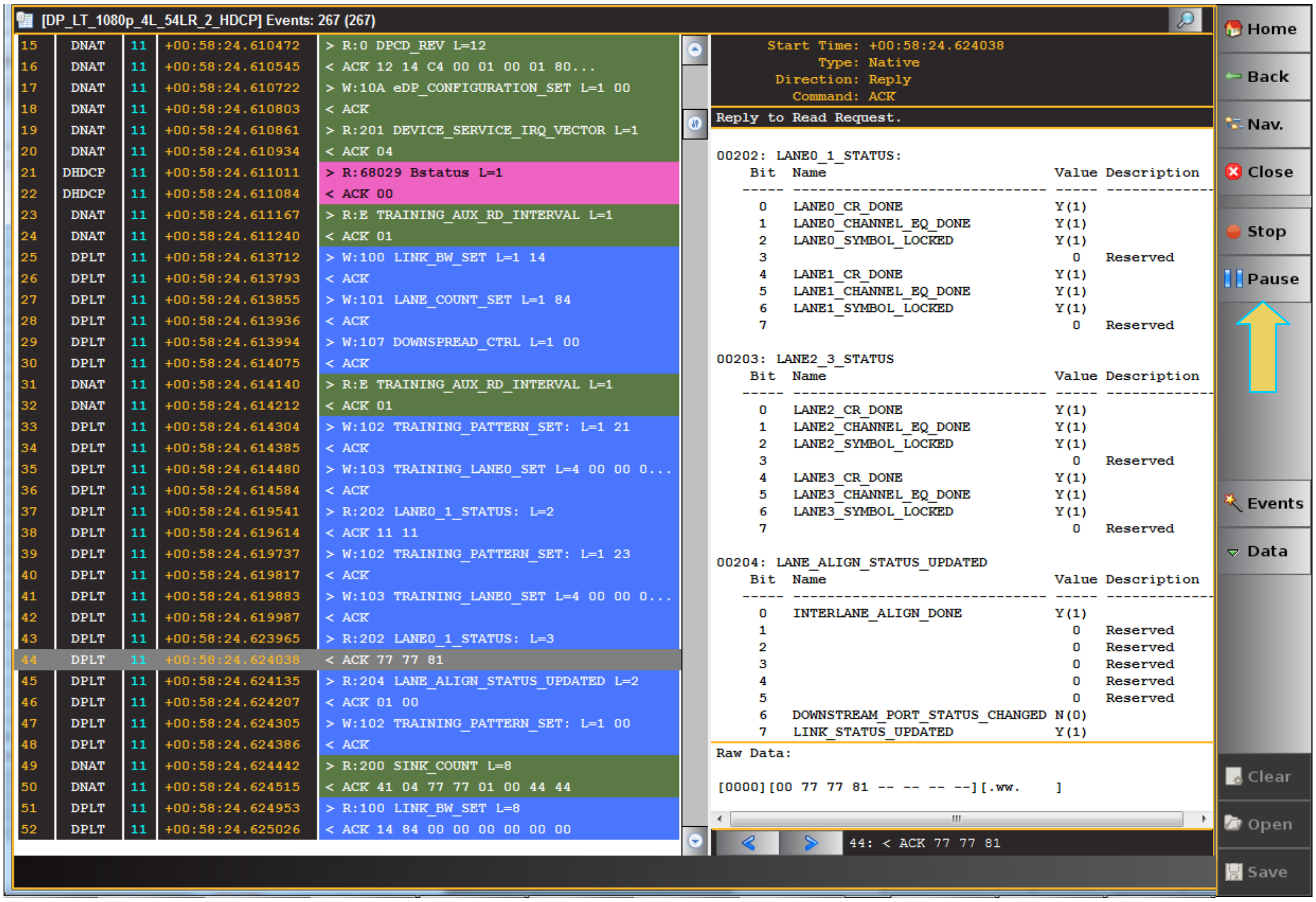


15	PDVDM	61	+01:27:10.568284	SNK:1 ACK Discover Identity
16	PDCTL	61	+01:27:10.569339	SRC:1 GoodCRC
17	PDVDM	61	+01:27:10.570857	SRC:4 Discover SVIDs
18	PDCTL	61	+01:27:10.571540	SNK:4 GoodCRC
19	PDVDM	61	+01:27:10.573018	SNK:2 ACK Discover SVIDs
20	PDCTL	61	+01:27:10.573959	SRC:2 GoodCRC
21	PDVDM	61	+01:27:10.575463	SRC:5 Discover Modes
22	PDCTL	61	+01:27:10.576146	SNK:5 GoodCRC
23	PDVDM	61	+01:27:10.577637	SNK:3 ACK Discover Modes
24	PDCTL	61	+01:27:10.578433	SRC:3 GoodCRC
25	PDVDM	61	+01:27:10.579944	SRC:6 Discover Modes
26	PDCTL	61	+01:27:10.580634	SNK:6 GoodCRC
27	PDVDM	61	+01:27:10.582113	SNK:4 ACK Discover Modes
28	PDCTL	61	+01:27:10.582916	SRC:4 GoodCRC
29	PDVDM	61	+01:27:10.584434	SRC:7 Enter Mode 1
30	PDCTL	61	+01:27:10.585110	SNK:7 GoodCRC
31	PDVDM	61	+01:27:10.586594	SNK:5 ACK Enter Mode 1
32	PDCTL	61	+01:27:10.587276	SRC:5 GoodCRC
33	PDVDM	61	+01:27:10.588787	SRC:0 DP_Status_Update
34	PDCTL	61	+01:27:10.589602	SNK:0 GoodCRC
35	PDVDM	61	+01:27:10.591080	SNK:6 ACK DP_Status_Update
36	PDCTL	61	+01:27:10.591890	SRC:6 GoodCRC
37	PDVDM	61	+01:27:10.593395	SRC:1 DP_Configure
38	PDCTL	61	+01:27:10.594209	SNK:1 GoodCRC
39	PDVDM	61	+01:27:10.595694	SNK:7 ACK DP_Configure
40	PDCTL	61	+01:27:10.596367	SRC:7 GoodCRC
41	PDVDM	61	+01:27:10.597724	SNK:0 Attention 1
42	PDCTL	61	+01:27:10.598525	SRC:0 GoodCRC
43	DPHP	61	+01:27:10.602425	HPD Rising Edge
44	DNAT	61	+01:27:10.603324	> R:200 SINK_COUNT L=6
45	DNAT	61	+01:27:10.603396	< ACK 41 04 02 00 80 00
46	DNAT	61	+01:27:10.603521	> R:E TRAINING_AUX_RD_INTERVAL L=1
47	DNAT	61	+01:27:10.603593	< ACK 81
48	DNAT	61	+01:27:10.603664	> R:0 DPCD_REV L=1
49	DNAT	61	+01:27:10.603736	< ACK 14
50	DNAT	61	+01:27:10.603806	> R:2200 DP1.3_DPCD_REV L=16
51	DNAT	61	+01:27:10.603878	< ACK 14 1E C4 81 01 00 01 80 0...
52	DNAT	61	+01:27:10.604104	> R:90 FEC_CAPABILITY L=1

```
      Start Time: +01:27:10.579944
 Start of Packet: SOP
    Message Type: Vendor_Defined
       MessageID: 6
 Port Power Role: Source
  Port Data Role: DFP
   Spec Revision: Revision 2.0
    Data Objects: 1
1) VDM Header
     SVID or VID    : 0x 451 (1105)
     VDM Type       : Structured
     VDM Version    : 1.0
     Object Position: 0
     Command Type   : Initiator
     Command        : Discover Modes

- Preamble: CC-1, 63, [Sync-1,Sync-1,Sync-1,Sync-2]
- Header:   1D6Fh
- Object 1: 04518003h
- CRC:      875D537Dh
- EOP
```

```
25:  SRC:6 Discover Modes
```

You can then view the DPCD reads and writes and the link training transactions as shown in the example below.



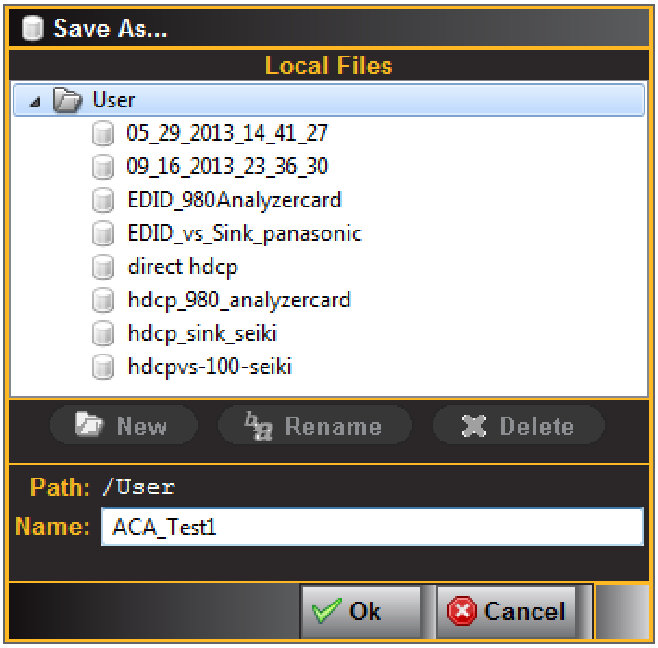
[DP_LT_1080p_4L_54LR_2_HDCP] Events: 267 (267)

```
15  DNAT   11  +00:58:24.610472  > R:0 DPCD_REV L=12
16  DNAT   11  +00:58:24.610545  < ACK 12 14 C4 00 01 00 01 80...
17  DNAT   11  +00:58:24.610722  > W:10A eDP_CONFIGURATION_SET L=1 00
18  DNAT   11  +00:58:24.610803  < ACK
19  DNAT   11  +00:58:24.610861  > R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
20  DNAT   11  +00:58:24.610934  < ACK 04
21  DHDCP  11  +00:58:24.611011  > R:68029 Bstatus L=1
22  DHDCP  11  +00:58:24.611084  < ACK 00
23  DNAT   11  +00:58:24.611167  > R:E TRAINING_AUX_RD_INTERVAL L=1
24  DNAT   11  +00:58:24.611240  < ACK 01
25  DPLT   11  +00:58:24.613712  > W:100 LINK_BW_SET L=1 14
26  DPLT   11  +00:58:24.613793  < ACK
27  DPLT   11  +00:58:24.613855  > W:101 LANE_COUNT_SET L=1 84
28  DPLT   11  +00:58:24.613936  < ACK
29  DPLT   11  +00:58:24.613994  > W:107 DOWNSPREAD_CTRL L=1 00
30  DPLT   11  +00:58:24.614075  < ACK
31  DNAT   11  +00:58:24.614140  > R:E TRAINING_AUX_RD_INTERVAL L=1
32  DNAT   11  +00:58:24.614212  < ACK 01
33  DPLT   11  +00:58:24.614304  > W:102 TRAINING_PATTERN_SET: L=1 21
34  DPLT   11  +00:58:24.614385  < ACK
35  DPLT   11  +00:58:24.614480  > W:103 TRAINING_LANE0_SET L=4 00 00 0...
36  DPLT   11  +00:58:24.614584  < ACK
37  DPLT   11  +00:58:24.619541  > R:202 LANE0_1_STATUS: L=2
38  DPLT   11  +00:58:24.619614  < ACK 11 11
39  DPLT   11  +00:58:24.619737  > W:102 TRAINING_PATTERN_SET: L=1 23
40  DPLT   11  +00:58:24.619817  < ACK
41  DPLT   11  +00:58:24.619883  > W:103 TRAINING_LANE0_SET L=4 00 00 0...
42  DPLT   11  +00:58:24.619987  < ACK
43  DPLT   11  +00:58:24.623965  > R:202 LANE0_1_STATUS: L=3
44  DPLT   11  +00:58:24.624038  < ACK 77 77 81
45  DPLT   11  +00:58:24.624135  > R:204 LANE_ALIGN_STATUS_UPDATED L=2
46  DPLT   11  +00:58:24.624207  < ACK 01 00
47  DPLT   11  +00:58:24.624305  > W:102 TRAINING_PATTERN_SET: L=1 00
48  DPLT   11  +00:58:24.624386  < ACK
49  DNAT   11  +00:58:24.624442  > R:200 SINK_COUNT L=8
50  DNAT   11  +00:58:24.624515  < ACK 41 04 77 77 01 00 44 44
51  DPLT   11  +00:58:24.624953  > R:100 LINK_BW_SET L=8
52  DPLT   11  +00:58:24.625026  < ACK 14 84 00 00 00 00 00 00
```

```
     Start Time: +00:58:24.624038
           Type: Native
      Direction: Reply
        Command: ACK
Reply to Read Request.

00202: LANE0_1_STATUS:
    Bit  Name                              Value Description
   ----- --------------------------------- ----- ------------
     0   LANE0_CR_DONE                     Y(1)
     1   LANE0_CHANNEL_EQ_DONE             Y(1)
     2   LANE0_SYMBOL_LOCKED               Y(1)
     3                                       0   Reserved
     4   LANE1_CR_DONE                     Y(1)
     5   LANE1_CHANNEL_EQ_DONE             Y(1)
     6   LANE1_SYMBOL_LOCKED               Y(1)
     7                                       0   Reserved

00203: LANE2_3_STATUS
    Bit  Name                              Value Description
   ----- --------------------------------- ----- ------------
     0   LANE2_CR_DONE                     Y(1)
     1   LANE2_CHANNEL_EQ_DONE             Y(1)
     2   LANE2_SYMBOL_LOCKED               Y(1)
     3                                       0   Reserved
     4   LANE3_CR_DONE                     Y(1)
     5   LANE3_CHANNEL_EQ_DONE             Y(1)
     6   LANE3_SYMBOL_LOCKED               Y(1)
     7                                       0   Reserved

00204: LANE_ALIGN_STATUS_UPDATED
    Bit  Name                              Value Description
   ----- --------------------------------- ----- ------------
     0   INTERLANE_ALIGN_DONE              Y(1)
     1                                       0   Reserved
     2                                       0   Reserved
     3                                       0   Reserved
     4                                       0   Reserved
     5                                       0   Reserved
     6   DOWNSTREAM_PORT_STATUS_CHANGED    N(0)
     7   LINK_STATUS_UPDATED               Y(1)
Raw Data:

[0000][00 77 77 81 -- -- -- --][.ww.    ]

44: < ACK 77 77 81
```

Important Note: You can filter and search through the ACA traces. Procedures for searching and sorting are provided in a separate subsection further below.

5. Click on **Save to Instrument** or **Save to PC** depending on whether you are working with the external ACA Remote Control utility or the embedded Aux Channel Analyzer. A dialog box appears (below). Enter a name and then click on **OK**.
6. Click on **Save to Instrument** or **Save to PC** depending on whether you are working with the external ACA Remote Control utility or the embedded Aux Channel Analyzer. A dialog box appears (below). Enter a name and then click on **OK**.



User
05_29_2013_14_41_27
09_16_2013_23_36_30
EDID_980Analyzercard
EDID_vs_Sink_panasonic
direct hdcp
hdcp_980_analyzercard
hdcp_sink_seiki
hdcpvs-100-seiki

Path: /User
Name: ACA_Test1

Please note that in order to use the **ACA Data Viewer** utility (next subsection) on your PC to view the traces or the ACA viewer on the 980 embedded display with the powerful searching and filtering features, you must save the file. If you are working on the embedded **Aux Channel Analyzer** viewer but prefer to use **ACA Data Viewer** on the external 980 GUI Manager, you will have to transfer the saved file to your PC using the external 980 GUI Manager.

7.5 Passively Monitoring the Auxiliary Channels with the Aux Channel Analyzer utilities

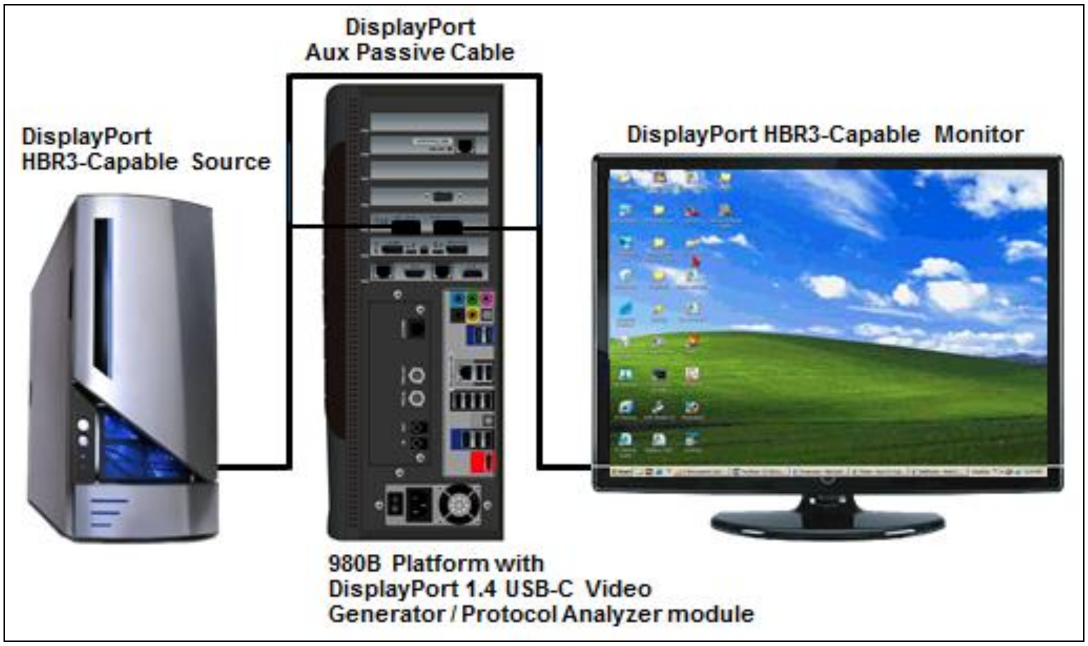
This subsection describes the procedures for monitoring the auxiliary channel data through the 980 GUI Manager using the Aux Channel Analyzer real time utilities—both the **Aux Channel Analyzer** utility through the *embedded* 980 GUI Manager or the **ACA Remote Control** utility available through the *external* 980 GUI Manager. You can monitor the DisplayPort transactions in real time when module is emulating a DisplayPort source device. If you have the DisplayPort Rx Analyzer port you can emulate a DisplayPort sink device to test a DisplayPort source device.

Note: You cannot monitor a USB-C to USB-C source to sink connection using the passive monitoring adjunct module.

7.5.1 Making the physical connections

This subsection describes how to make the proper physical connections between the 980 module supporting the ACA features and the device under test. The following diagrams depict the test setups for testing a DisplayPort display device and a DisplayPort source device. The operation of the ACA is the same when testing a source or a sink.

1. Connect the DisplayPort display device under test to one of the DisplayPort module's Tx and Rx ports as shown below.



7.5.2 Monitoring the DisplayPort Aux Channel Transactions in Real Time with the ACA Utilities

Use the following procedures to monitor the DisplayPort Aux Chan transactions with a DisplayPort device in real time. The procedures assume that the DP device under test is powered up and connected to one of the 980 DP Video Generator / Analyzer ports. The operation of the ACA is the same when testing a source or a sink.

The operation of the two ACA real time utilities—**Aux Channel Analyzer** on the *embedded* 980 GUI and the **ACA Remote Control** on the *external* 980 GUI Manager-- is similar. The screen examples used in this subsection are from the **ACA Remote Control** utility on the *external* 980 GUI Manager exceptions related to the operation of the ACA on the embedded 980 GUI Manager are noted.

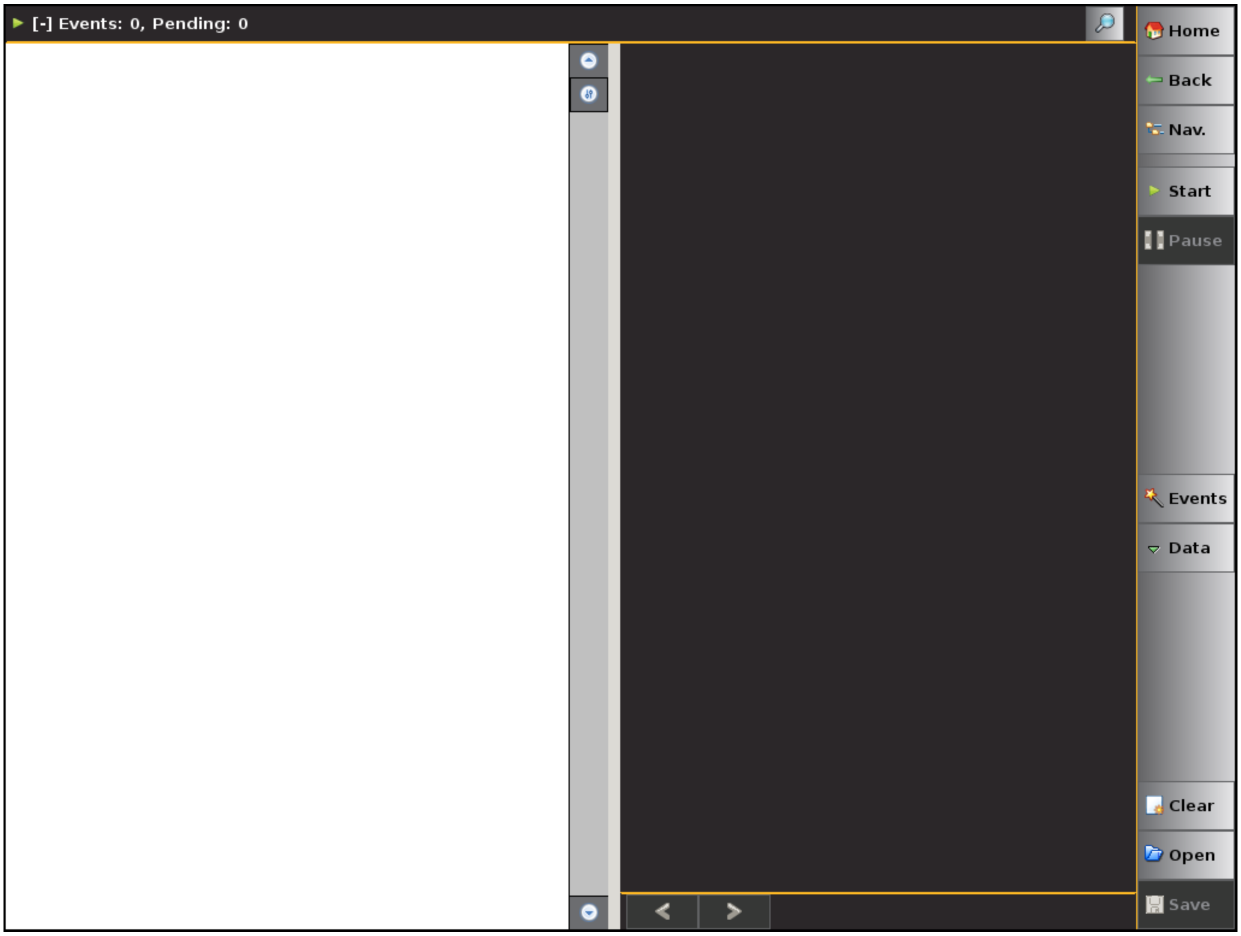
Important Note: You can filter and search through the ACA traces. Procedures for searching and sorting are provided in a separate subsection further below.

To monitor the DisplayPort transactions:

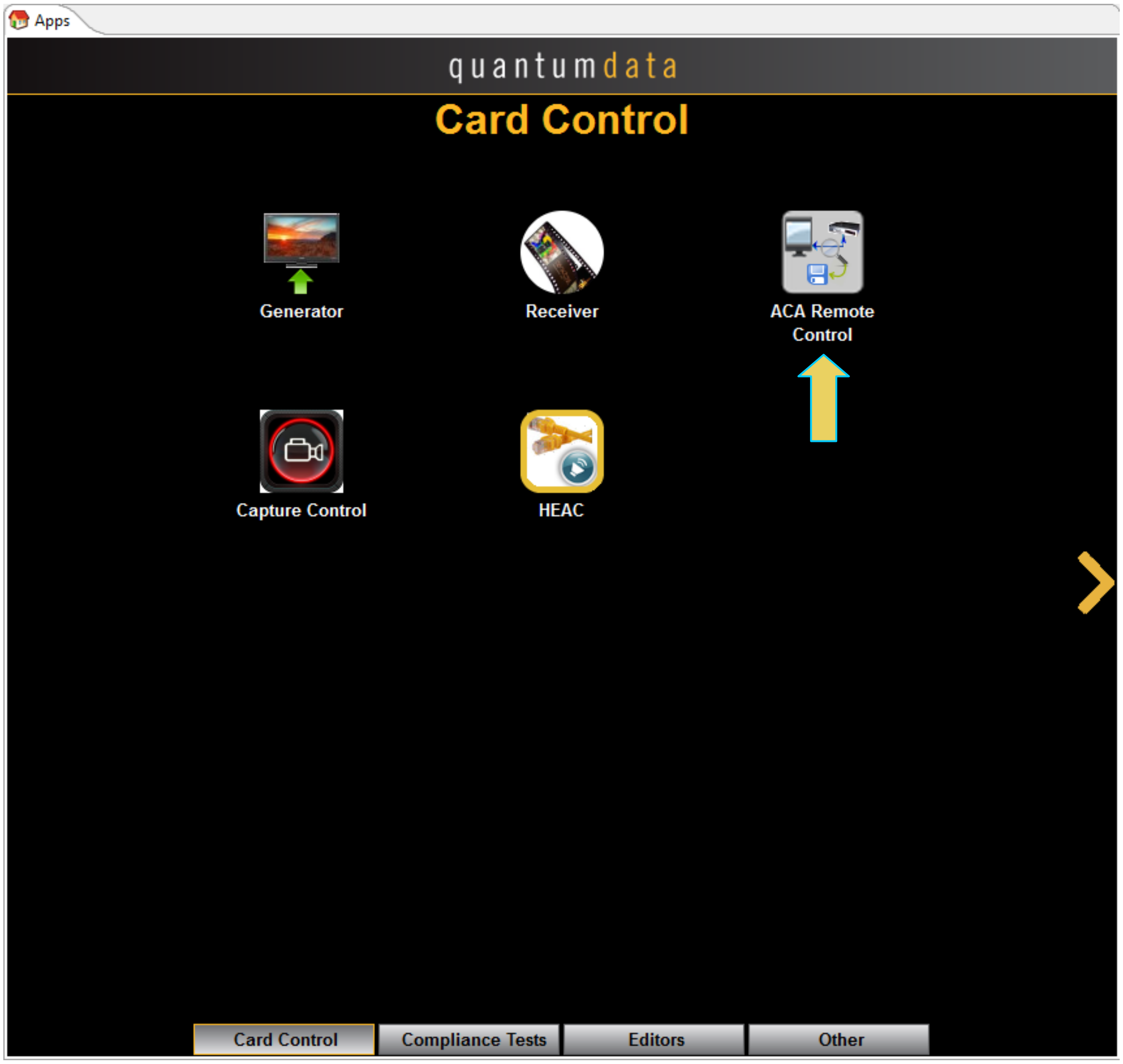
1. For the *embedded* ACA utility, touch select the **Aux Channel Analyzer** on the page 1 (Card Control) of the **Apps** panel:


quantumdata
Card Control
Generator
HDMI 1.4
Protocol Analyzer
RX - Card 3
HDMI 2.0a RX/TX
Protocol Analyzer
RX - Card 6
Aux. Channel
Analyzer
Capture Control
HEAC
Page 1 of 4
Card Control
Compliance Tests
Editors
Other
Back
Navigator
STATIC: 10.30.196.201
ATP Version: 4.18.13 (3 cards detected)

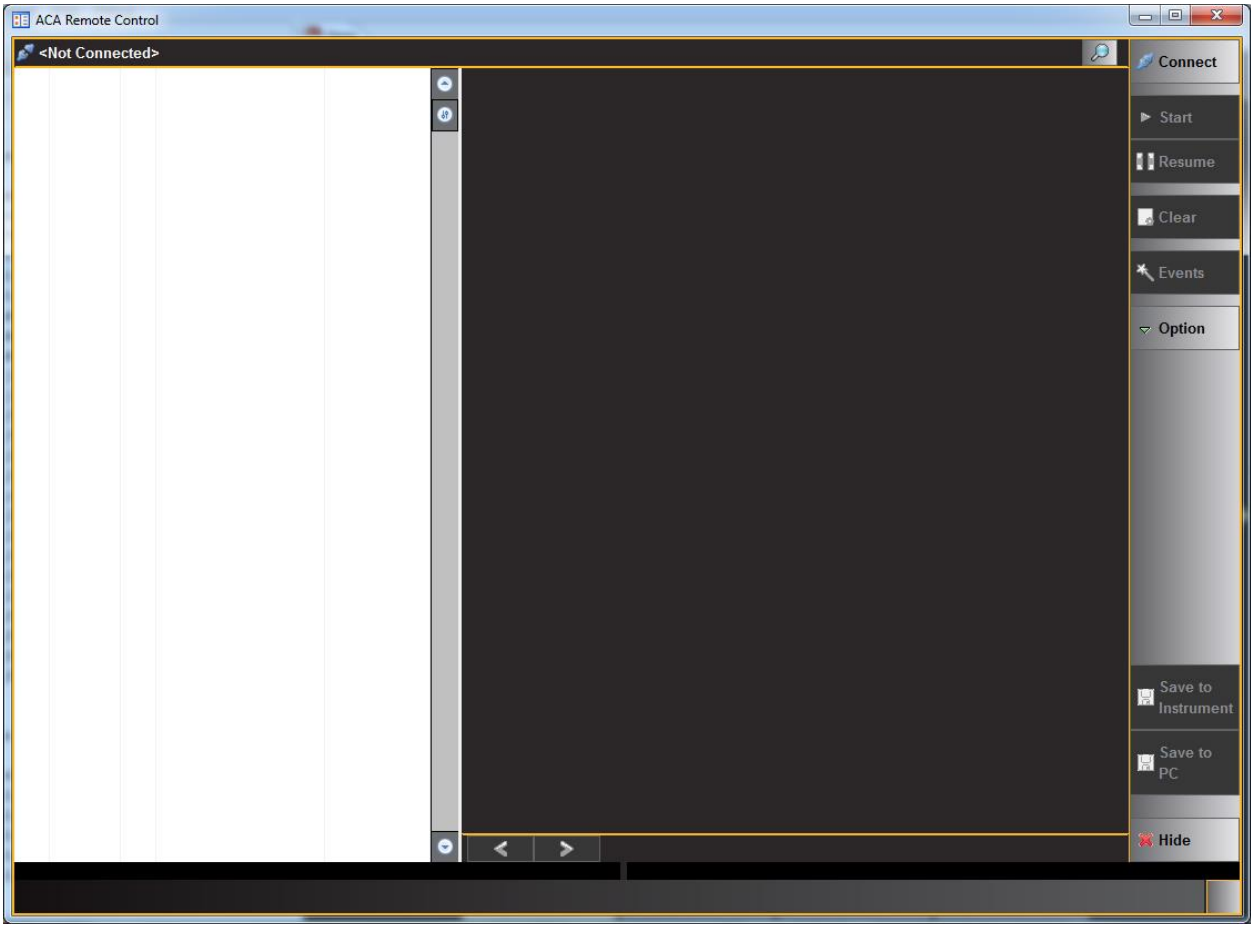
The **Aux Channel Analyzer** panel appears as shown below:



2. For the *embedded* ACA utility, touch select the **Aux Channel Analyzer** on the page 1 (Card Control) of the **Apps** panel:


Apps
quantumdata
Card Control
Generator
Receiver
ACA Remote Control
Capture Control
HEAC
Card Control
Compliance Tests
Editors
Other

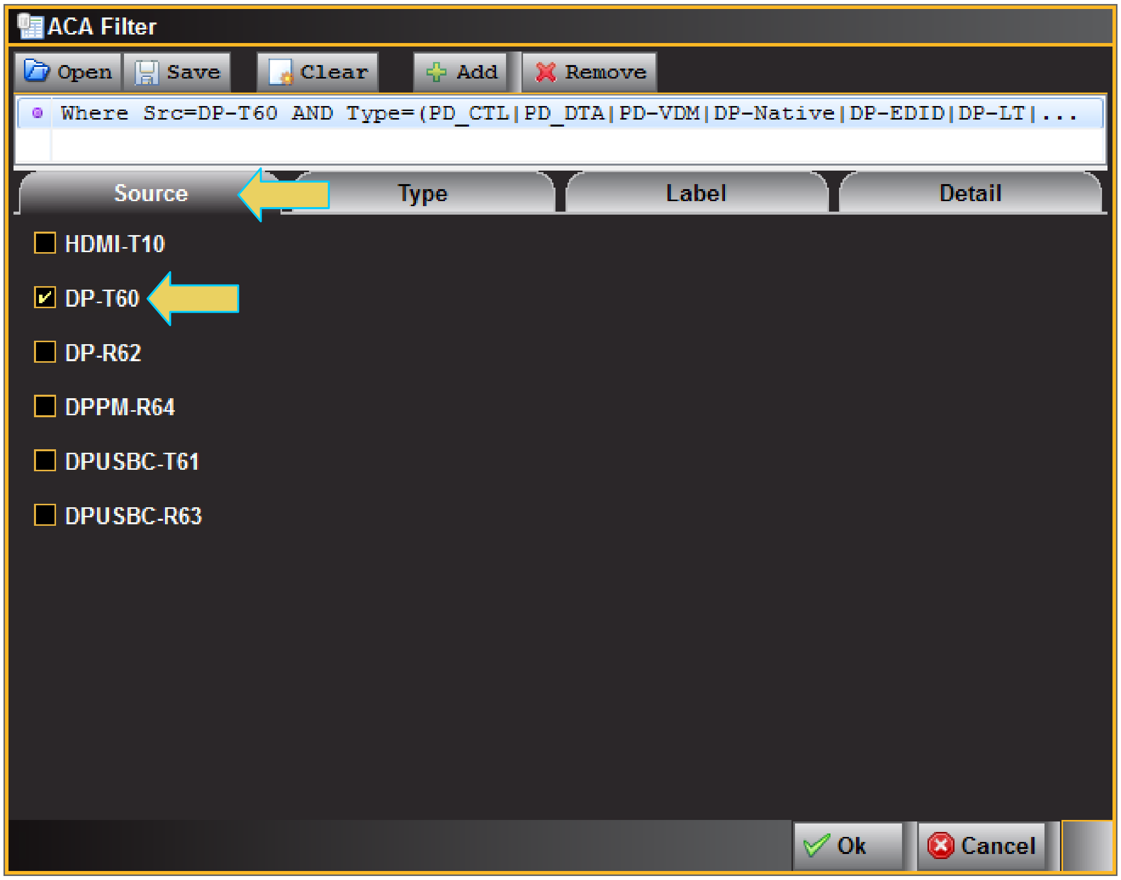
The **ACA Remote Control** panel appears as shown below:



For the **ACA Remote Control** panel you will have to connect to a 980 Instrument that you have provisioned in the external 980 GUI Manager application. The **ACA Remote Control** dialog box will appear showing all the 980 systems you have provisioned in the 980 GUI Manger. Typically you will only have one 980 system provisioned in the application, so you will simply select your lone 980 system and click the **OK** button on the dialog box.

3. From the **Events** [Events] button on the ACA panel, select the DP module's port that you are monitoring using the pull-down menu.

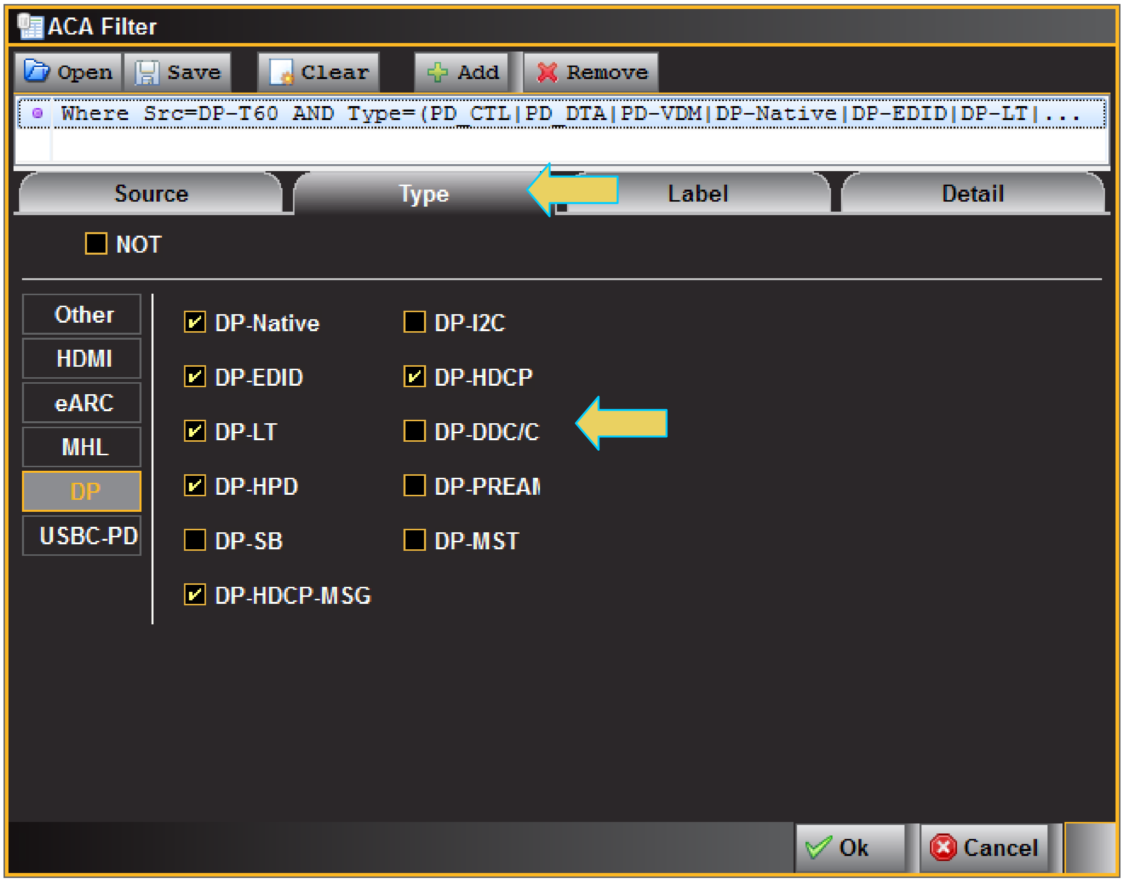
The **ACA Event Selection** dialog box is shown below.



Where Src=DP-T60 AND Type=(PD_CTL|PD_DTA|PD-VDM|DP-Native|DP-EDID|DP-LT|...

☐ HDMI-T10
☑ DP-T60
☐ DP-R62
☐ DPPM-R64
☐ DPUSBC-T61
☐ DPUSBC-R63

4. Select the DP protocol elements you wish to monitor on the ACA.



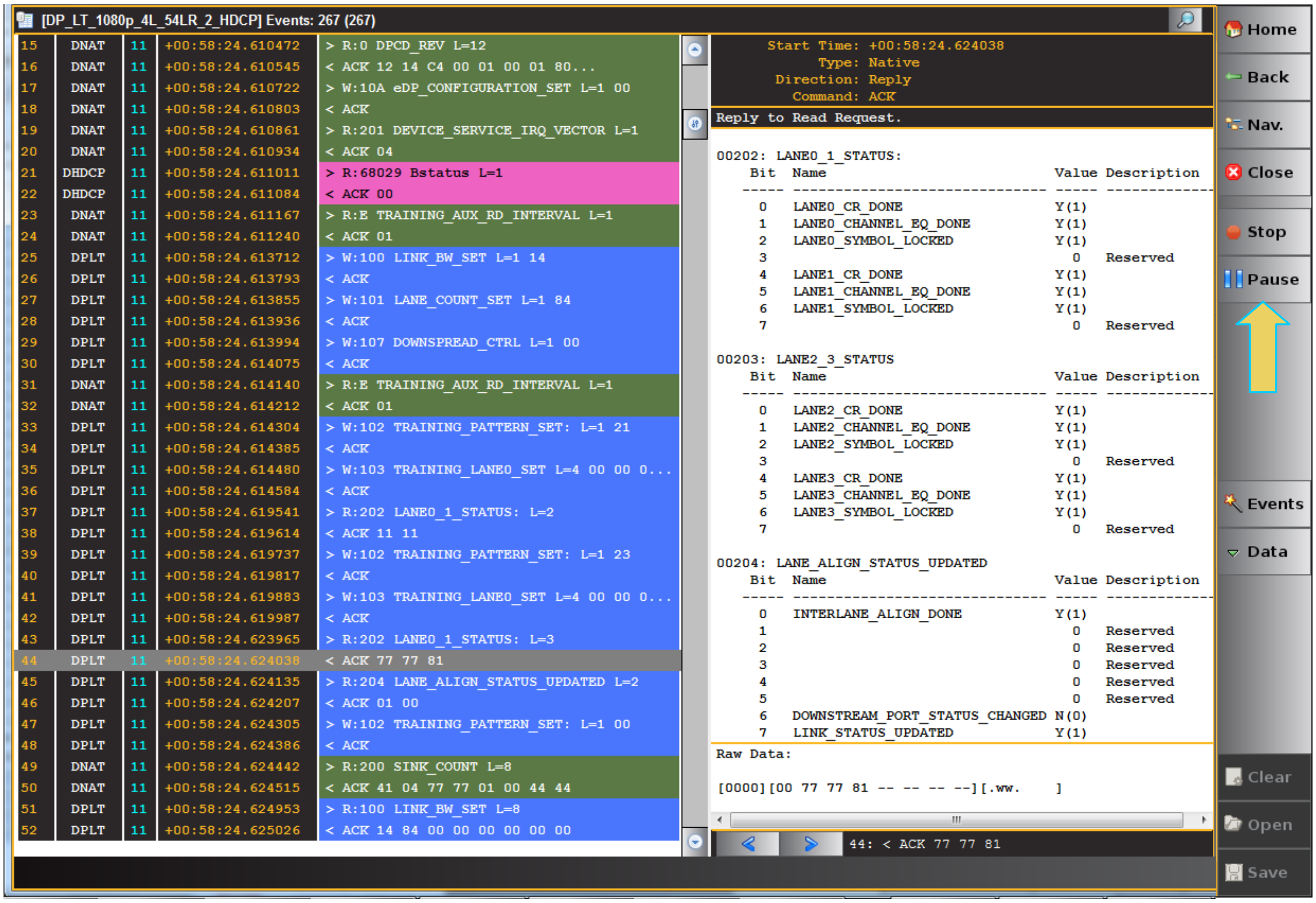
```
Where Src=DP-T60 AND Type=(PD_CTL|PD_DTA|PD-VDM|DP-Native|DP-EDID|DP-LT|...
```

☐ NOT

☑ DP-Native
☑ DP-EDID
☑ DP-LT
☑ DP-HPD
☐ DP-SB
☑ DP-HDCP-MSG
☐ DP-I2C
☑ DP-HDCP
☐ DP-DDC/C
☐ DP-PREAM
☐ DP-MST

5. Take the necessary action—such as a hot plug—to initiate EDID, HDCP or Link Training transactions. You will see the Aux Chan transactions in the ACA panel as shown below.

6. Touch select the **Start** ▶ Start button on the ACA Menu panel on the right to initiate the viewing of the DP Aux Chan transactions. An example showing monitored data is shown below. You can stop or pause the collection at any time using the buttons on the ACA menu panel on the right. These are indicated in the screen example below.

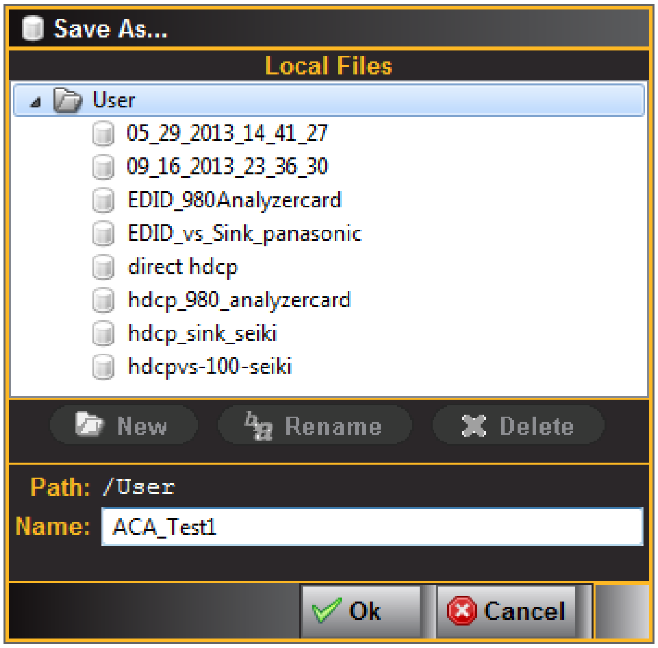


```
[DP_LT_1080p_4L_54LR_2_HDCP] Events: 267 (267)
15  DNAT   11  +00:58:24.610472  > R:0 DPCD_REV L=12
16  DNAT   11  +00:58:24.610545  < ACK 12 14 C4 00 01 00 01 80...
17  DNAT   11  +00:58:24.610722  > W:10A eDP_CONFIGURATION_SET L=1 00
18  DNAT   11  +00:58:24.610803  < ACK
19  DNAT   11  +00:58:24.610861  > R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
20  DNAT   11  +00:58:24.610934  < ACK 04
21  DHDCP  11  +00:58:24.611011  > R:68029 Bstatus L=1
22  DHDCP  11  +00:58:24.611084  < ACK 00
23  DNAT   11  +00:58:24.611167  > R:E TRAINING_AUX_RD_INTERVAL L=1
24  DNAT   11  +00:58:24.611240  < ACK 01
25  DPLT   11  +00:58:24.613712  > W:100 LINK_BW_SET L=1 14
26  DPLT   11  +00:58:24.613793  < ACK
27  DPLT   11  +00:58:24.613855  > W:101 LANE_COUNT_SET L=1 84
28  DPLT   11  +00:58:24.613936  < ACK
29  DPLT   11  +00:58:24.613994  > W:107 DOWNSPREAD_CTRL L=1 00
30  DPLT   11  +00:58:24.614075  < ACK
31  DNAT   11  +00:58:24.614140  > R:E TRAINING_AUX_RD_INTERVAL L=1
32  DNAT   11  +00:58:24.614212  < ACK 01
33  DPLT   11  +00:58:24.614304  > W:102 TRAINING_PATTERN_SET: L=1 21
34  DPLT   11  +00:58:24.614385  < ACK
35  DPLT   11  +00:58:24.614480  > W:103 TRAINING_LANE0_SET L=4 00 00 0...
36  DPLT   11  +00:58:24.614584  < ACK
37  DPLT   11  +00:58:24.619541  > R:202 LANE0_1_STATUS: L=2
38  DPLT   11  +00:58:24.619614  < ACK 11 11
39  DPLT   11  +00:58:24.619737  > W:102 TRAINING_PATTERN_SET: L=1 23
40  DPLT   11  +00:58:24.619817  < ACK
41  DPLT   11  +00:58:24.619883  > W:103 TRAINING_LANE0_SET L=4 00 00 0...
42  DPLT   11  +00:58:24.619987  < ACK
43  DPLT   11  +00:58:24.623965  > R:202 LANE0_1_STATUS: L=3
44  DPLT   11  +00:58:24.624038  < ACK 77 77 81
45  DPLT   11  +00:58:24.624135  > R:204 LANE_ALIGN_STATUS_UPDATED L=2
46  DPLT   11  +00:58:24.624207  < ACK 01 00
47  DPLT   11  +00:58:24.624305  > W:102 TRAINING_PATTERN_SET: L=1 00
48  DPLT   11  +00:58:24.624386  < ACK
49  DNAT   11  +00:58:24.624442  > R:200 SINK_COUNT L=8
50  DNAT   11  +00:58:24.624515  < ACK 41 04 77 77 01 00 44 44
51  DPLT   11  +00:58:24.624953  > R:100 LINK_BW_SET L=8
52  DPLT   11  +00:58:24.625026  < ACK 14 84 00 00 00 00 00 00
```

```
    Start Time: +00:58:24.624038
          Type: Native
     Direction: Reply
       Command: ACK
Reply to Read Request.

00202: LANE0_1_STATUS:
    Bit  Name                            Value Description
   ----- ------------------------------  ----- ------------
     0   LANE0_CR_DONE                   Y(1)
     1   LANE0_CHANNEL_EQ_DONE           Y(1)
     2   LANE0_SYMBOL_LOCKED             Y(1)
     3                                     0   Reserved
     4   LANE1_CR_DONE                   Y(1)
     5   LANE1_CHANNEL_EQ_DONE           Y(1)
     6   LANE1_SYMBOL_LOCKED             Y(1)
     7                                     0   Reserved

00203: LANE2_3_STATUS
    Bit  Name                            Value Description
   ----- ------------------------------  ----- ------------
     0   LANE2_CR_DONE                   Y(1)
     1   LANE2_CHANNEL_EQ_DONE           Y(1)
     2   LANE2_SYMBOL_LOCKED             Y(1)
     3                                     0   Reserved
     4   LANE3_CR_DONE                   Y(1)
     5   LANE3_CHANNEL_EQ_DONE           Y(1)
     6   LANE3_SYMBOL_LOCKED             Y(1)
     7                                     0   Reserved

00204: LANE_ALIGN_STATUS_UPDATED
    Bit  Name                            Value Description
   ----- ------------------------------  ----- ------------
     0   INTERLANE_ALIGN_DONE            Y(1)
     1                                     0   Reserved
     2                                     0   Reserved
     3                                     0   Reserved
     4                                     0   Reserved
     5                                     0   Reserved
     6   DOWNSTREAM_PORT_STATUS_CHANGED  N(0)
     7   LINK_STATUS_UPDATED             Y(1)
Raw Data:

[0000][00 77 77 81 -- -- -- --][.ww.    ]

44: < ACK 77 77 81
```

Important Note: You can filter and search through the ACA traces. Procedures for searching and sorting are provided in a separate subsection further below.

7. Click on **Save to Instrument** or **Save to PC** depending on whether you are working with the external ACA Remote Control utility or the embedded Aux Channel Analyzer. A dialog box appears (below). Enter a name and then click on **OK**.



Path: /User

Name: ACA_Test1

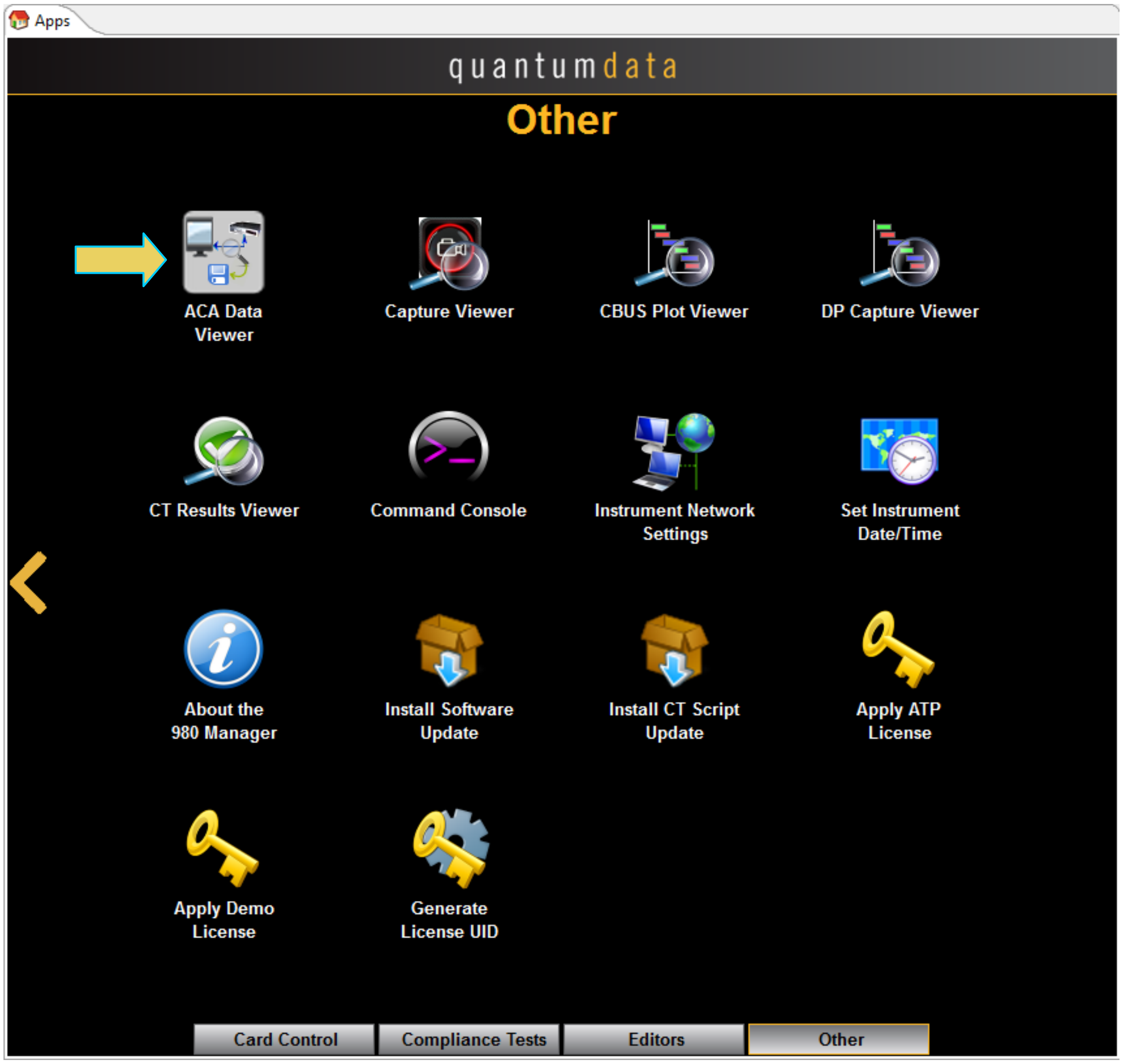
Please note that in order to use the **ACA Data Viewer** utility (next subsection) on your PC to view the traces or the ACA viewer on the 980 embedded display with the powerful searching and filtering features, you must save the file. If you are working on the embedded **Aux Channel Analyzer** viewer but prefer to use **ACA Data Viewer** on the external 980 GUI Manager, you will have to transfer the saved file to your PC using the external 980 GUI Manager.

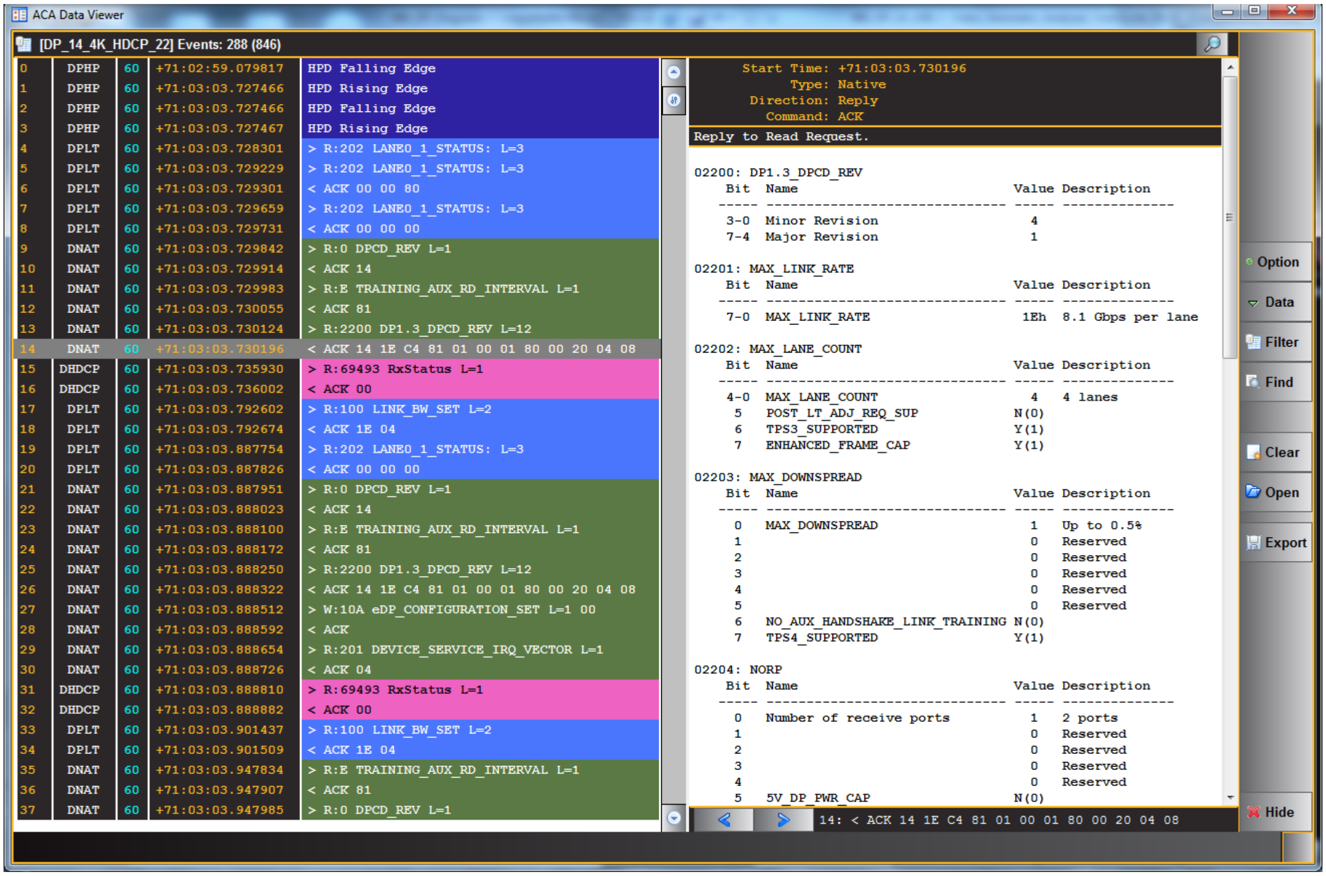
7.6 ACA Data Viewer – Viewing Stored Aux Channel Data

This subsection describes the **ACA Data Viewer** utility used for viewing DisplayPort Aux Channel transactions that have been stored on the PC hosting the *external* 980 GUI Manager. You can use the **ACA** utility on the *embedded* display to view ACA trace files stored on the 980 instrument itself. The operation of the two ACA utilities is similar. The screen examples used in this subsection are from the **ACA Data Viewer** utility but the general operation is similar to the embedded version.

7.6.1 ACA Data Viewer – Panel Description

The **ACA Remote Control** panel application is available on the *external* 980 GUI Manager. It enables you to collect and view the ACA transactions in real time from a remotely connected PC with the 980 GUI Manager application. The control panel elements are described in the table below.



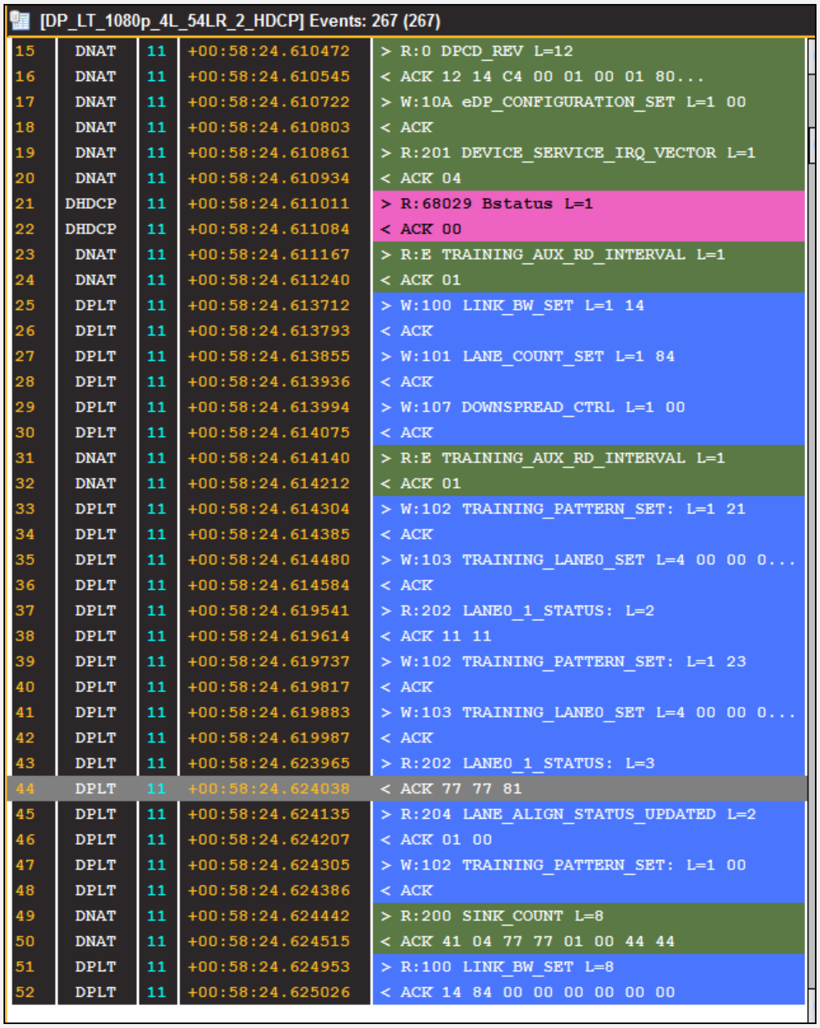


[DP_14_4K_HDCP_22] Events: 288 (846)

```
0   DPHP   60  +71:02:59.079817  HPD Falling Edge
1   DPHP   60  +71:03:03.727466  HPD Rising Edge
2   DPHP   60  +71:03:03.727466  HPD Falling Edge
3   DPHP   60  +71:03:03.727467  HPD Rising Edge
4   DPLT   60  +71:03:03.728301  > R:202 LANE0_1_STATUS: L=3
5   DPLT   60  +71:03:03.729229  > R:202 LANE0_1_STATUS: L=3
6   DPLT   60  +71:03:03.729301  < ACK 00 00 80
7   DPLT   60  +71:03:03.729659  > R:202 LANE0_1_STATUS: L=3
8   DPLT   60  +71:03:03.729731  < ACK 00 00 00
9   DNAT   60  +71:03:03.729842  > R:0 DPCD_REV L=1
10  DNAT   60  +71:03:03.729914  < ACK 14
11  DNAT   60  +71:03:03.729983  > R:E TRAINING_AUX_RD_INTERVAL L=1
12  DNAT   60  +71:03:03.730055  < ACK 81
13  DNAT   60  +71:03:03.730124  > R:2200 DP1.3_DPCD_REV L=12
14  DNAT   60  +71:03:03.730196  < ACK 14 1E C4 81 01 00 01 80 00 20 04 08
15  DHDCP  60  +71:03:03.735930  > R:69493 RxStatus L=1
16  DHDCP  60  +71:03:03.736002  < ACK 00
17  DPLT   60  +71:03:03.792602  > R:100 LINK_BW_SET L=2
18  DPLT   60  +71:03:03.792674  < ACK 1E 04
19  DPLT   60  +71:03:03.887754  > R:202 LANE0_1_STATUS: L=3
20  DPLT   60  +71:03:03.887826  < ACK 00 00 00
21  DNAT   60  +71:03:03.887951  > R:0 DPCD_REV L=1
22  DNAT   60  +71:03:03.888023  < ACK 14
23  DNAT   60  +71:03:03.888100  > R:E TRAINING_AUX_RD_INTERVAL L=1
24  DNAT   60  +71:03:03.888172  < ACK 81
25  DNAT   60  +71:03:03.888250  > R:2200 DP1.3_DPCD_REV L=12
26  DNAT   60  +71:03:03.888322  < ACK 14 1E C4 81 01 00 01 80 00 20 04 08
27  DNAT   60  +71:03:03.888512  > W:10A eDP_CONFIGURATION_SET L=1 00
28  DNAT   60  +71:03:03.888592  < ACK
29  DNAT   60  +71:03:03.888654  > R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
30  DNAT   60  +71:03:03.888726  < ACK 04
31  DHDCP  60  +71:03:03.888810  > R:69493 RxStatus L=1
32  DHDCP  60  +71:03:03.888882  < ACK 00
33  DPLT   60  +71:03:03.901437  > R:100 LINK_BW_SET L=2
34  DPLT   60  +71:03:03.901509  < ACK 1E 04
35  DNAT   60  +71:03:03.947834  > R:E TRAINING_AUX_RD_INTERVAL L=1
36  DNAT   60  +71:03:03.947907  < ACK 81
37  DNAT   60  +71:03:03.947985  > R:0 DPCD_REV L=1
```

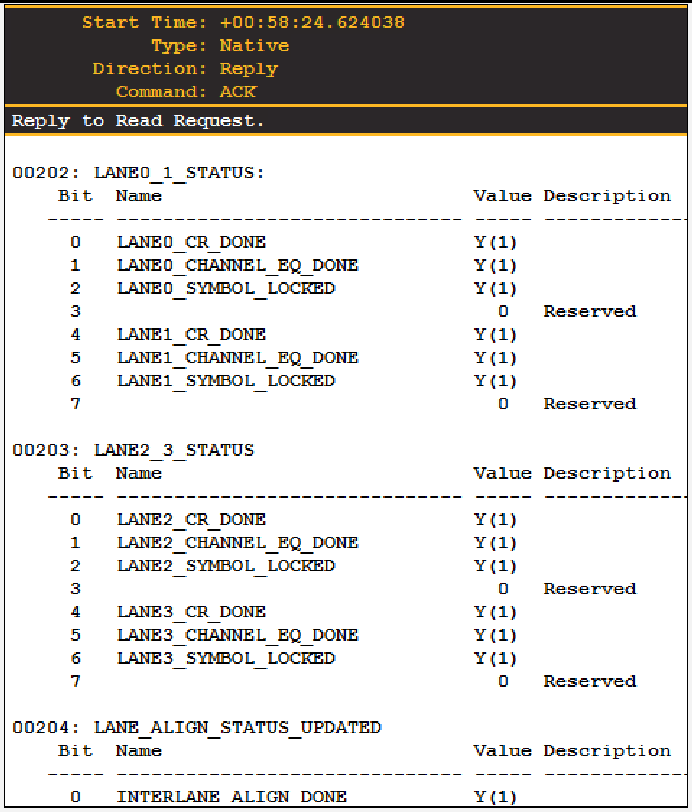
```
      Start Time: +71:03:03.730196
            Type: Native
       Direction: Reply
         Command: ACK
Reply to Read Request.

02200: DP1.3_DPCD_REV
    Bit   Name                          Value Description
   ----- ------------------------------ ----- -------------
    3-0  Minor Revision                   4
    7-4  Major Revision                   1

02201: MAX_LINK_RATE
    Bit   Name                          Value Description
   ----- ------------------------------ ----- -------------
    7-0  MAX_LINK_RATE                   1Eh  8.1 Gbps per lane

02202: MAX_LANE_COUNT
    Bit   Name                          Value Description
   ----- ------------------------------ ----- -------------
    4-0  MAX_LANE_COUNT                   4    4 lanes
     5   POST_LT_ADJ_REQ_SUP            N(0)
     6   TPS3_SUPPORTED                 Y(1)
     7   ENHANCED_FRAME_CAP             Y(1)

02203: MAX_DOWNSPREAD
    Bit   Name                          Value Description
   ----- ------------------------------ ----- -------------
     0   MAX_DOWNSPREAD                   1    Up to 0.5%
     1                                    0    Reserved
     2                                    0    Reserved
     3                                    0    Reserved
     4                                    0    Reserved
     5                                    0    Reserved
     6   NO_AUX_HANDSHAKE_LINK_TRAINING N(0)
     7   TPS4_SUPPORTED                 Y(1)

02204: NORP
    Bit   Name                          Value Description
   ----- ------------------------------ ----- -------------
     0   Number of receive ports          1    2 ports
     1                                    0    Reserved
     2                                    0    Reserved
     3                                    0    Reserved
     4                                    0    Reserved
     5   5V_DP_PWR_CAP                  N(0)
```

```
14: < ACK 14 1E C4 81 01 00 01 80 00 20 04 08
```

ACA Data Viewer	Information / Function
ACA Data Viewer - Trace Panel 	The following information is provided in the ACA Remote Control Panel data dialog box for each event: - **Item number** – This is a unique sequence number of the transaction. - **Type** – The type of Aux Chan transaction; either EDID, HDCP DPLT (Link Training), DNAT (DP native Aux transactions). - **980 Card Type, Interface number**. - **Time stamp** (optional viewing field) – Shows the timestamp of each transaction. Can either be absolute time based (shown) on the 980 system clock or relative time (Time-deltas) referenced from the initial transaction in the trace. - **Transaction Description** – A description of the transaction.
Details Panel	The data that is displayed in the Details panel will vary depending on the type of record. following information is provided in the ACA Event Details dialog box: - **Start Time** – This the start time of the transaction in microseconds from a reference time determined when the capture of real time data began. - **Type** – The type of Aux Chan transaction; either EDID, HDCP DPLT (Link Training), DNAT (DP native Aux transactions).

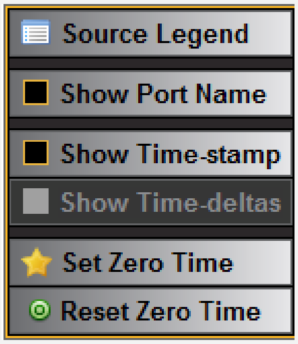
ACA Data Viewer - Trace Panel

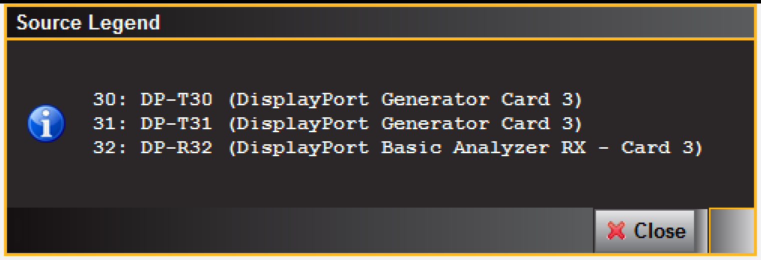
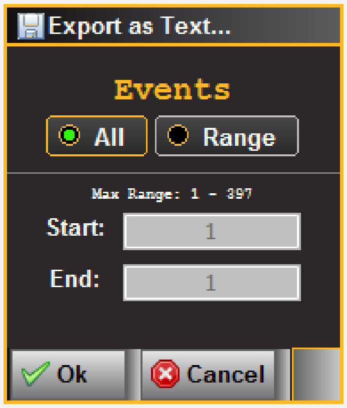
```
[DP_LT_1080p_4L_54LR_2_HDCP] Events: 267 (267)
15  DNAT   11  +00:58:24.610472  > R:0 DPCD_REV L=12
16  DNAT   11  +00:58:24.610545  < ACK 12 14 C4 00 01 00 01 80...
17  DNAT   11  +00:58:24.610722  > W:10A eDP_CONFIGURATION_SET L=1 00
18  DNAT   11  +00:58:24.610803  < ACK
19  DNAT   11  +00:58:24.610861  > R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
20  DNAT   11  +00:58:24.610934  < ACK 04
21  DHDCP  11  +00:58:24.611011  > R:68029 Bstatus L=1
22  DHDCP  11  +00:58:24.611084  < ACK 00
23  DNAT   11  +00:58:24.611167  > R:E TRAINING_AUX_RD_INTERVAL L=1
24  DNAT   11  +00:58:24.611240  < ACK 01
25  DPLT   11  +00:58:24.613712  > W:100 LINK_BW_SET L=1 14
26  DPLT   11  +00:58:24.613793  < ACK
27  DPLT   11  +00:58:24.613855  > W:101 LANE_COUNT_SET L=1 84
28  DPLT   11  +00:58:24.613936  < ACK
29  DPLT   11  +00:58:24.613994  > W:107 DOWNSPREAD_CTRL L=1 00
30  DPLT   11  +00:58:24.614075  < ACK
31  DNAT   11  +00:58:24.614140  > R:E TRAINING_AUX_RD_INTERVAL L=1
32  DNAT   11  +00:58:24.614212  < ACK 01
33  DPLT   11  +00:58:24.614304  > W:102 TRAINING_PATTERN_SET: L=1 21
34  DPLT   11  +00:58:24.614385  < ACK
35  DPLT   11  +00:58:24.614480  > W:103 TRAINING_LANE0_SET L=4 00 00 0...
36  DPLT   11  +00:58:24.614584  < ACK
37  DPLT   11  +00:58:24.619541  > R:202 LANE0_1_STATUS: L=2
38  DPLT   11  +00:58:24.619614  < ACK 11 11
39  DPLT   11  +00:58:24.619737  > W:102 TRAINING_PATTERN_SET: L=1 23
40  DPLT   11  +00:58:24.619817  < ACK
41  DPLT   11  +00:58:24.619883  > W:103 TRAINING_LANE0_SET L=4 00 00 0...
42  DPLT   11  +00:58:24.619987  < ACK
43  DPLT   11  +00:58:24.623965  > R:202 LANE0_1_STATUS: L=3
44  DPLT   11  +00:58:24.624038  < ACK 77 77 81
45  DPLT   11  +00:58:24.624135  > R:204 LANE_ALIGN_STATUS_UPDATED L=2
46  DPLT   11  +00:58:24.624207  < ACK 01 00
47  DPLT   11  +00:58:24.624305  > W:102 TRAINING_PATTERN_SET: L=1 00
48  DPLT   11  +00:58:24.624386  < ACK
49  DNAT   11  +00:58:24.624442  > R:200 SINK_COUNT L=8
50  DNAT   11  +00:58:24.624515  < ACK 41 04 77 77 01 00 44 44
51  DPLT   11  +00:58:24.624953  > R:100 LINK_BW_SET L=8
52  DPLT   11  +00:58:24.625026  < ACK 14 84 00 00 00 00 00 00
```

ACA Data Viewer	Information / Function
	**Note**: The information in the Details panel will vary depending on the type of log record that is selected. ▪ **Duration** – The duration in milliseconds of the transaction. ▪ **Direction** – The direction of the transaction either a request or a reply. ▪ **Maximum I2C Rate** – The rate that the I2C channel clock is operating. ▪ **Details** (text) – The contents of the transaction in human readable text. ▪ **Details** (hex) – The contents of the transaction in hex data.
	There are some control arrows and a status panel on the bottom of the ACA Event Details panel. These are as follows: ▪ Left arrow – The left arrow allows you to see the details of the next transaction. ▪ Right arrow – The right arrow allows you to see the details of the previous transaction. ▪ Status field – Shows the sequence number and the description of the selected transaction.

```
      Start Time: +00:58:24.624038
            Type: Native
       Direction: Reply
         Command: ACK
Reply to Read Request.

00202: LANE0_1_STATUS:
    Bit  Name                           Value Description
   ----- ------------------------------ ----- ------------
     0   LANE0_CR_DONE                  Y(1)
     1   LANE0_CHANNEL_EQ_DONE          Y(1)
     2   LANE0_SYMBOL_LOCKED            Y(1)
     3                                    0   Reserved
     4   LANE1_CR_DONE                  Y(1)
     5   LANE1_CHANNEL_EQ_DONE          Y(1)
     6   LANE1_SYMBOL_LOCKED            Y(1)
     7                                    0   Reserved

00203: LANE2_3_STATUS
    Bit  Name                           Value Description
   ----- ------------------------------ ----- ------------
     0   LANE2_CR_DONE                  Y(1)
     1   LANE2_CHANNEL_EQ_DONE          Y(1)
     2   LANE2_SYMBOL_LOCKED            Y(1)
     3                                    0   Reserved
     4   LANE3_CR_DONE                  Y(1)
     5   LANE3_CHANNEL_EQ_DONE          Y(1)
     6   LANE3_SYMBOL_LOCKED            Y(1)
     7                                    0   Reserved

00204: LANE_ALIGN_STATUS_UPDATED
    Bit  Name                           Value Description
   ----- ------------------------------ ----- ------------
     0   INTERLANE_ALIGN_DONE           Y(1)
```

```
44: < ACK 77 77 81
```

ACA Data Viewer	**Information / Function**
	There is a menu associated with the ACA Remote Control Info panel. It is location on the right side of the panel: ▪ "Viewing Glass" – This icon is on the upper left of the ACA window. It is not part of the control menu. When activated it displays a pop up window that enables you to display the text in Small, Medium, or Large text. ▪ **Options** – Opens up a flyout menu. Described below. ▪ **Data** – Opens up a flyout checkbox enabling you to sort the log records by time. ▪ **Clear** – Clears the ACA Trace panel. ▪ **Open** – Enables you to open an ACA trace file stored on your PC. ▪ **Export** – Enables you to export the entire trace file or a range of records in the trace file, to a text file. See dialog box below left.
Options Flyout Menu 	The **Options** flyout menu items are described below. ▪ **Source Legend** – Window that lists the ports and their definition on each available module in the 980 system. ▪ **Show Port Name** – Checkbox enabling you to display or not display the Port number. ▪ **Time-stamp** – Checkbox enabling you to show or not show the timestamps for each transaction. ▪ **Time-deltas** – Checkbox enabling

ACA Data Viewer	Information / Function
 Source Legend 30: DP-T30 (DisplayPort Generator Card 3) 31: DP-T31 (DisplayPort Generator Card 3) 32: DP-R32 (DisplayPort Basic Analyzer RX - Card 3) 	you to show the time stamps relative to the previous transaction. ▪ **Set Zero Time** – Enables you to set a log record to zero. Subsequent log records are relative to this new zero time record. ▪ **Reset Zero Time** – Resets the initial record in the active log in the ACA Trace window to zero.
Export as Text  Max Range: 1 - 397 Start: 1 End: 1 	The **Export as Text** dialog box elements are described below. ▪ **All** – Radio button to specify that you wish to export the entire ACA trace file to a text file stored on your PC. ▪ **Range** – Checkbox enabling you to display or not display the Port number. ▪ **Start** – Field available only when Range radio button is active to specify the first record of the range of records to include in the export operation. ▪ **End** – Field available only when Range radio button is active to specify the last record of the range of records to include in the export operation. ▪ **OK** – Button to initiate the export. ▪ **Cancel** – Cancel the export operation.

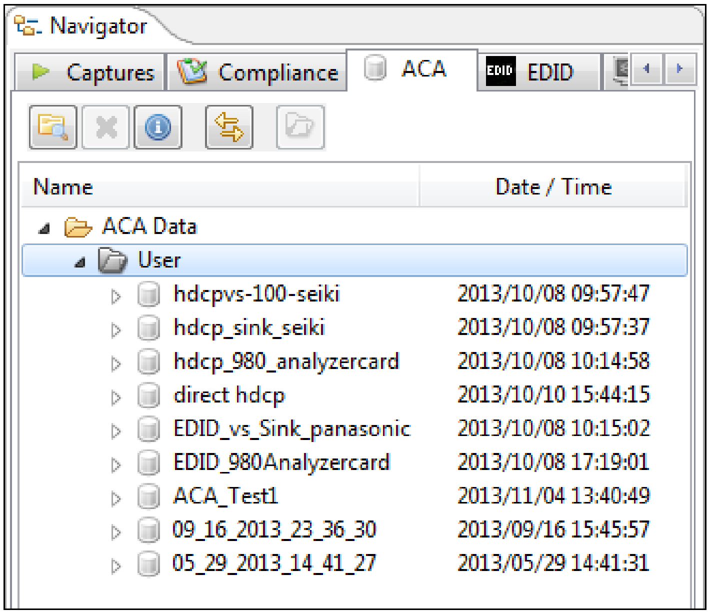
7.7 Viewing Stored DP Aux Chan traces on a PC with the ACA Data Viewer utility

This subsection describes how you can view ACA traces using the ACA viewer off-line on your PC with the **ACA Data Viewer** utility. In order to view the ACA files on your PC with the 980 GUI Manager application you will first have to transfer them to the PC using the **Data Transfer** utility.

The ability to save ACA traces enables you to disseminate them to other subject matter experts for analysis or to Quantum Data for support. You can view the ACA traces without a 980 test instrument. You simply download the 980 GUI Manager from the Quantum Data website on the downloads page.

Transferring ACA trace files from the 980 to a host PC with the 980 GUI Manager:

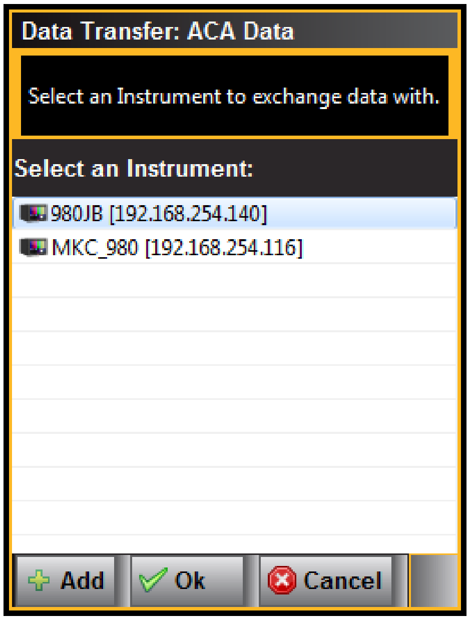
1. Make sure the 980 GUI Manager is installed on your PC. Use the procedures at Downloading and installing the 980 GUI Manager.
2. Access a stored ACA data from the **Navigator** panel and highlight a directory as shown below.



Name	Date / Time
ACA Data	
User	
hdcpvs-100-seiki	2013/10/08 09:57:47
hdcp_sink_seiki	2013/10/08 09:57:37
hdcp_980_analyzercard	2013/10/08 10:14:58
direct hdcp	2013/10/10 15:44:15
EDID_vs_Sink_panasonic	2013/10/08 10:15:02
EDID_980Analyzercard	2013/10/08 17:19:01
ACA_Test1	2013/11/04 13:40:49
09_16_2013_23_36_30	2013/09/16 15:45:57
05_29_2013_14_41_27	2013/05/29 14:41:31

3. Access the **Data Transfer** utility by double clicking on the Transfer Data icon .

   The **Data Transfer: ACA Data** dialog box appears (below) enabling you to select the 980 that you want to transfer data from. Select the desired 980 and click OK. The **Data Transfer: ACA Data** panel will appear.

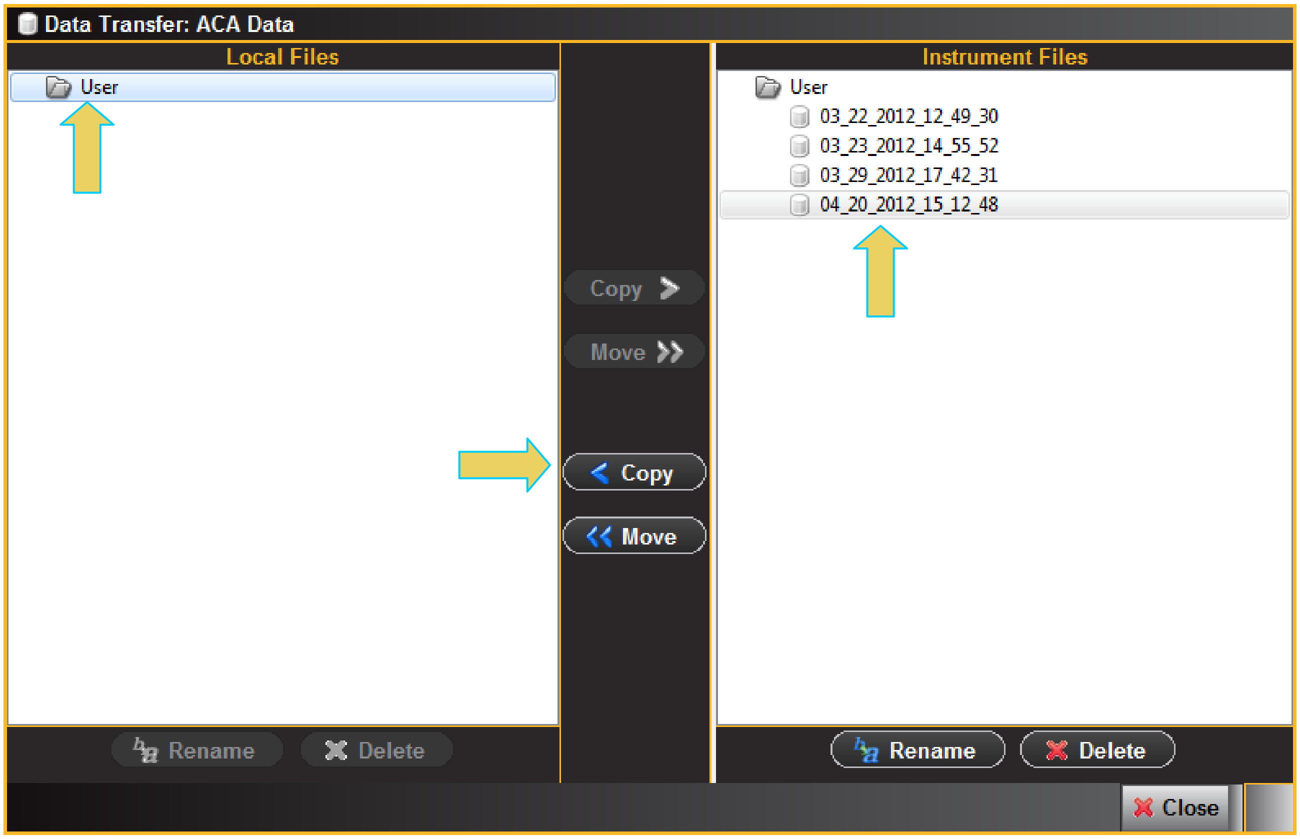


Select an Instrument to exchange data with.

Select an Instrument:

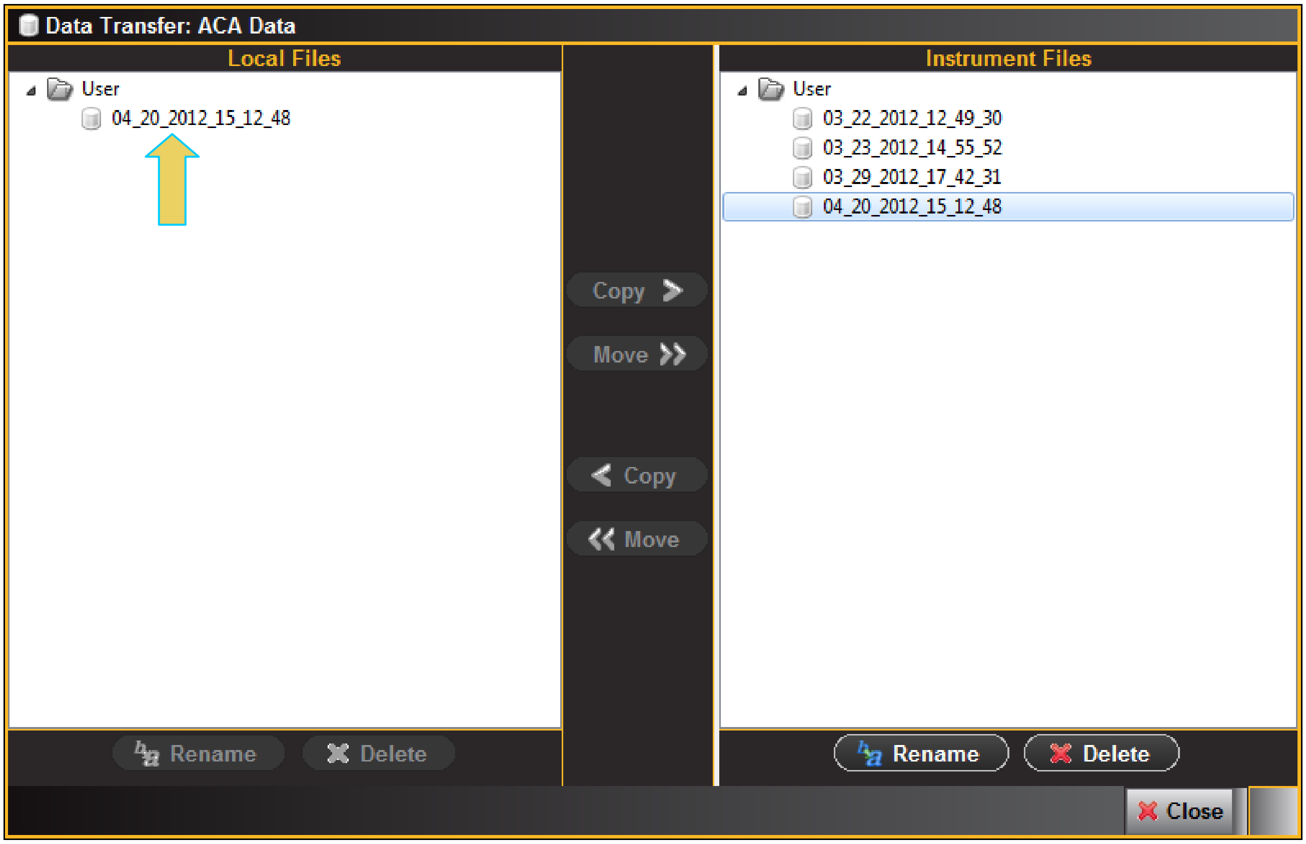
980JB [192.168.254.140]
MKC_980 [192.168.254.116]

4. Access the **Data Transfer** panel by double clicking on the Transfer Data icon .
5. The **Data Transfer** panel appears in context with the ACA files on the 980 (Instrument) under the **Instrument Files** available as shown below.

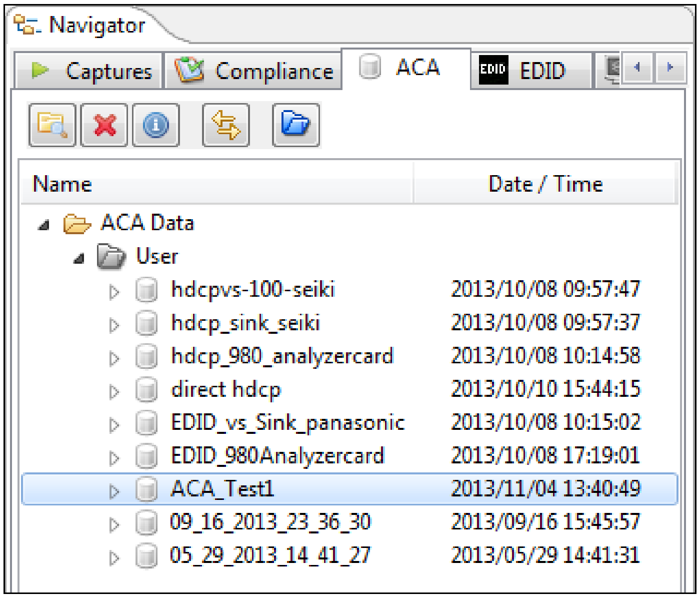


6. Highlight a directory on the **Local Files** side (host PC) and then initiate a **Copy** or **Move**.

   The file appears on the PC host **Local** Files (below).



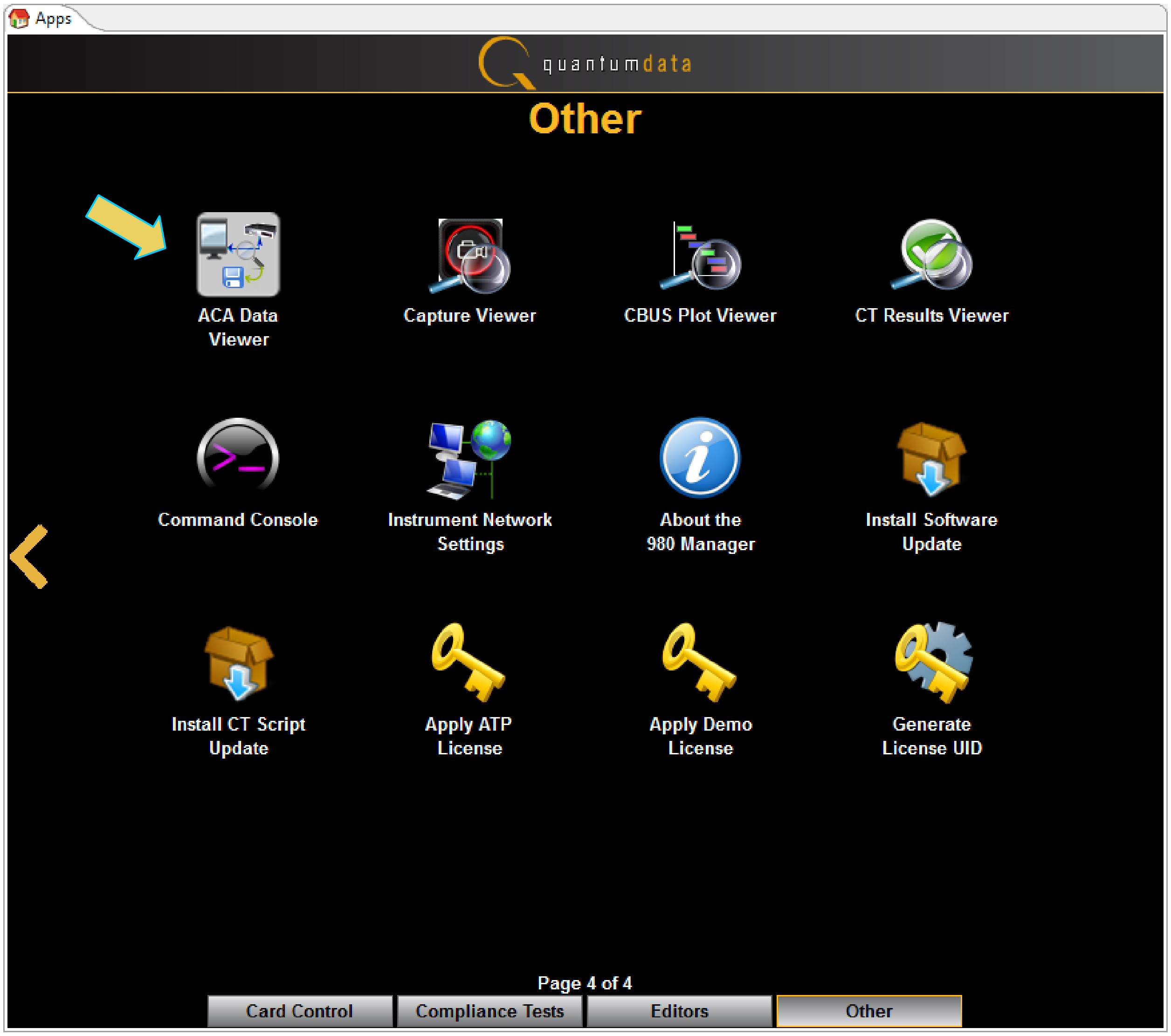
The data appears in the **Navigator** panel under the ACA data as shown below.



Name	Date / Time
ACA Data	
User	
hdcpvs-100-seiki	2013/10/08 09:57:47
hdcp_sink_seiki	2013/10/08 09:57:37
hdcp_980_analyzercard	2013/10/08 10:14:58
direct hdcp	2013/10/10 15:44:15
EDID_vs_Sink_panasonic	2013/10/08 10:15:02
EDID_980Analyzercard	2013/10/08 17:19:01
ACA_Test1	2013/11/04 13:40:49
09_16_2013_23_36_30	2013/09/16 15:45:57
05_29_2013_14_41_27	2013/05/29 14:41:31

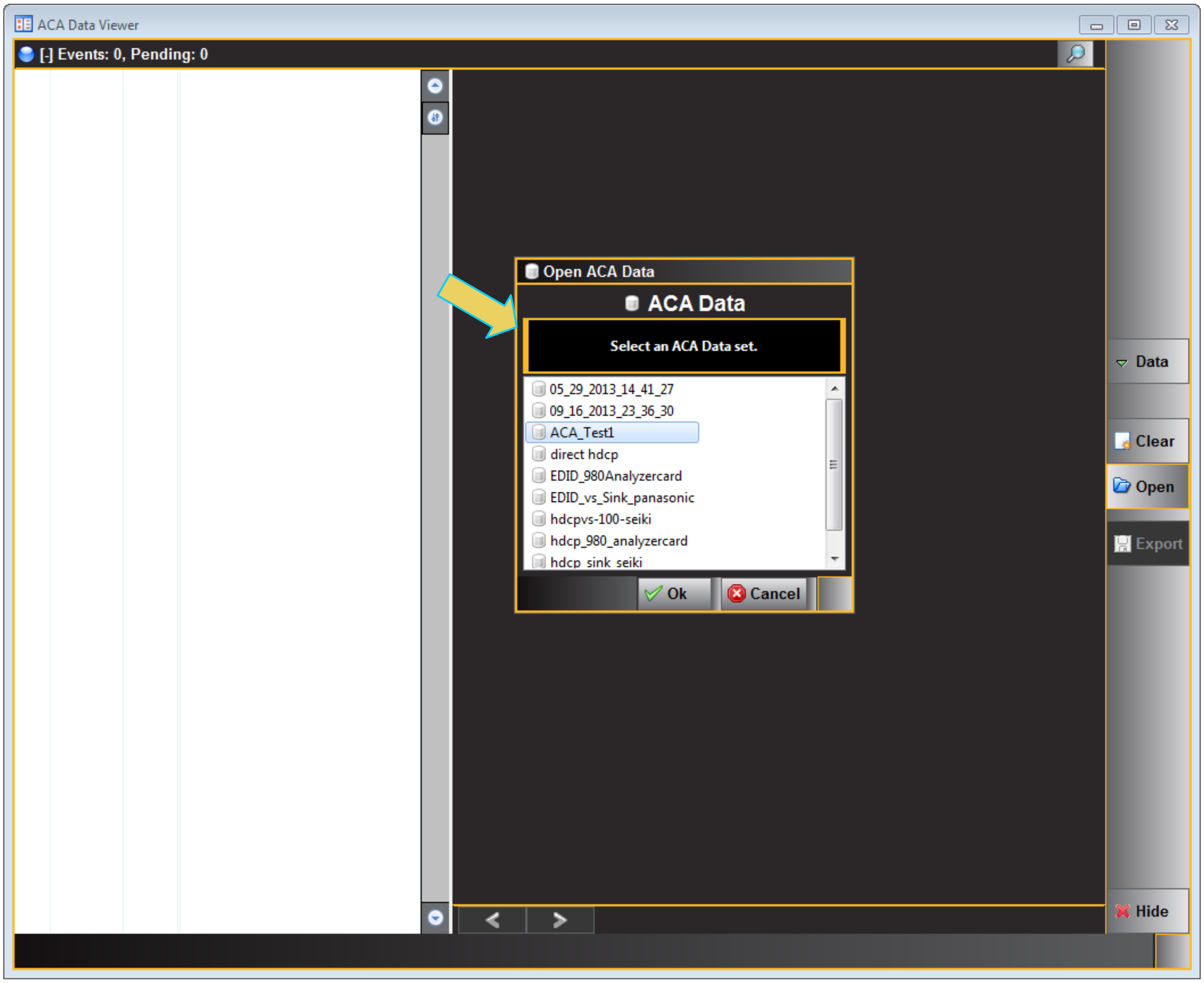
Viewing ACA trace files with the ACA Data Viewer:

1. Open up the ACA panel to view the transferred file. You can access the ACA panel from the **Other** Apps panel (Page 4).



The **Aux Channel Analyzer** panel appears.

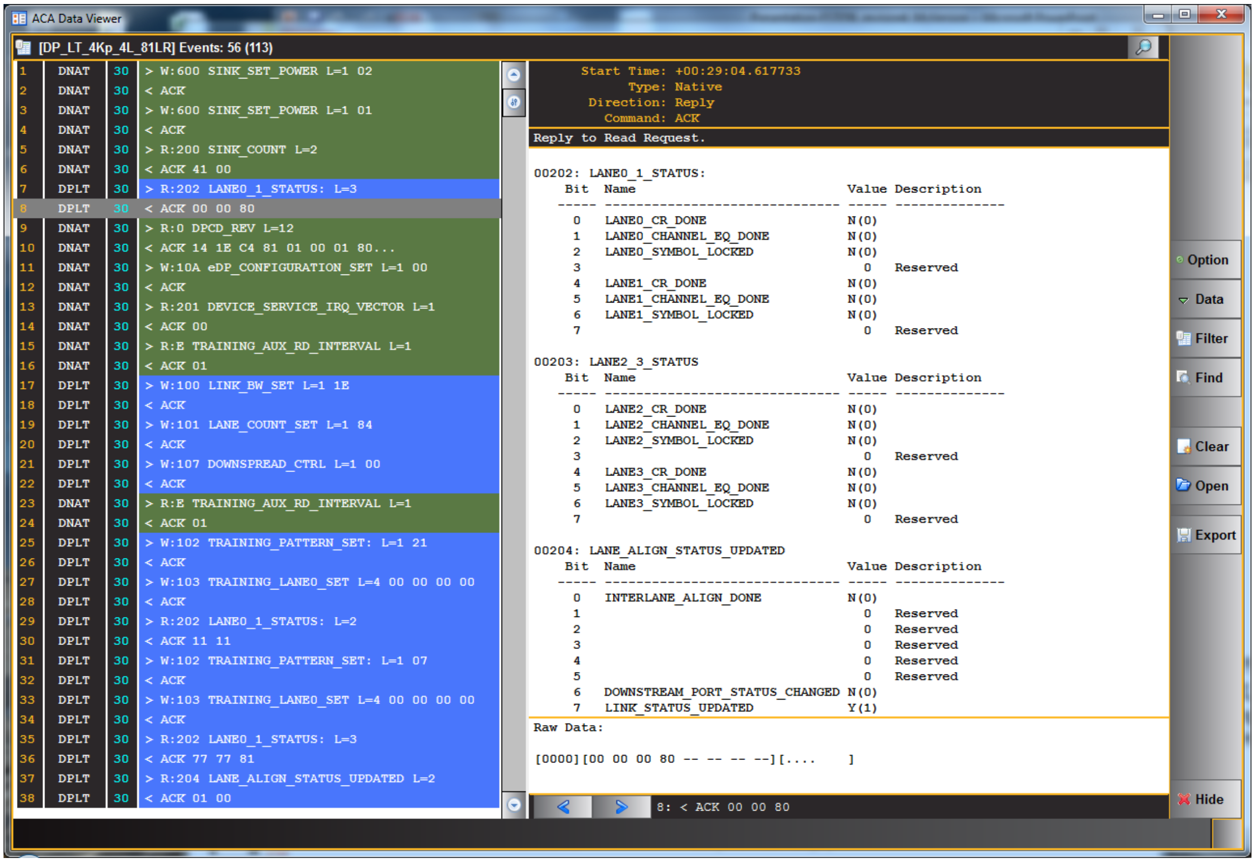
2. Select the **Open** button to open the ACA file as shown below:



Select an ACA Data set.

05_29_2013_14_41_27
09_16_2013_23_36_30
ACA_Test1
direct hdcp
EDID_980Analyzercard
EDID_vs_Sink_panasonic
hdcpvs-100-seiki
hdcp_980_analyzercard
hdcp_sink_seiki

3. Click the **OK** activation button on the Open **ACA Data** dialog box. The ACA trace file will appear in the window.



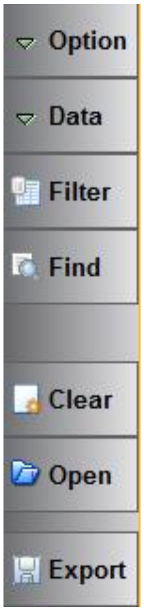
```
1   DNAT  30  > W:600 SINK_SET_POWER L=1 02
2   DNAT  30  < ACK
3   DNAT  30  > W:600 SINK_SET_POWER L=1 01
4   DNAT  30  < ACK
5   DNAT  30  > R:200 SINK_COUNT L=2
6   DNAT  30  < ACK 41 00
7   DPLT  30  > R:202 LANE0_1_STATUS: L=3
8   DPLT  30  < ACK 00 00 80
9   DNAT  30  > R:0 DPCD_REV L=12
10  DNAT  30  < ACK 14 1E C4 81 01 00 01 80...
11  DNAT  30  > W:10A eDP_CONFIGURATION_SET L=1 00
12  DNAT  30  < ACK
13  DNAT  30  > R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
14  DNAT  30  < ACK 00
15  DNAT  30  > R:E TRAINING_AUX_RD_INTERVAL L=1
16  DNAT  30  < ACK 01
17  DPLT  30  > W:100 LINK_BW_SET L=1 1E
18  DPLT  30  < ACK
19  DPLT  30  > W:101 LANE_COUNT_SET L=1 84
20  DPLT  30  < ACK
21  DPLT  30  > W:107 DOWNSPREAD_CTRL L=1 00
22  DPLT  30  < ACK
23  DNAT  30  > R:E TRAINING_AUX_RD_INTERVAL L=1
24  DNAT  30  < ACK 01
25  DPLT  30  > W:102 TRAINING_PATTERN_SET: L=1 21
26  DPLT  30  < ACK
27  DPLT  30  > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
28  DPLT  30  < ACK
29  DPLT  30  > R:202 LANE0_1_STATUS: L=2
30  DPLT  30  < ACK 11 11
31  DPLT  30  > W:102 TRAINING_PATTERN_SET: L=1 07
32  DPLT  30  < ACK
33  DPLT  30  > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
34  DPLT  30  < ACK
35  DPLT  30  > R:202 LANE0_1_STATUS: L=3
36  DPLT  30  < ACK 77 77 81
37  DPLT  30  > R:204 LANE_ALIGN_STATUS_UPDATED L=2
38  DPLT  30  < ACK 01 00
```

```
 Start Time: +00:29:04.617733
       Type: Native
  Direction: Reply
    Command: ACK
Reply to Read Request.

00202: LANE0_1_STATUS:
    Bit  Name                           Value Description
   ----- ------------------------------ ----- -------------
     0   LANE0_CR_DONE                  N(0)
     1   LANE0_CHANNEL_EQ_DONE          N(0)
     2   LANE0_SYMBOL_LOCKED            N(0)
     3                                    0   Reserved
     4   LANE1_CR_DONE                  N(0)
     5   LANE1_CHANNEL_EQ_DONE          N(0)
     6   LANE1_SYMBOL_LOCKED            N(0)
     7                                    0   Reserved

00203: LANE2_3_STATUS
    Bit  Name                           Value Description
   ----- ------------------------------ ----- -------------
     0   LANE2_CR_DONE                  N(0)
     1   LANE2_CHANNEL_EQ_DONE          N(0)
     2   LANE2_SYMBOL_LOCKED            N(0)
     3                                    0   Reserved
     4   LANE3_CR_DONE                  N(0)
     5   LANE3_CHANNEL_EQ_DONE          N(0)
     6   LANE3_SYMBOL_LOCKED            N(0)
     7                                    0   Reserved

00204: LANE_ALIGN_STATUS_UPDATED
    Bit  Name                           Value Description
   ----- ------------------------------ ----- -------------
     0   INTERLANE_ALIGN_DONE           N(0)
     1                                    0   Reserved
     2                                    0   Reserved
     3                                    0   Reserved
     4                                    0   Reserved
     5                                    0   Reserved
     6   DOWNSTREAM_PORT_STATUS_CHANGED N(0)
     7   LINK_STATUS_UPDATED            Y(1)
Raw Data:

[0000][00 00 00 80 -- -- -- --][....    ]

8: < ACK 00 00 80
```

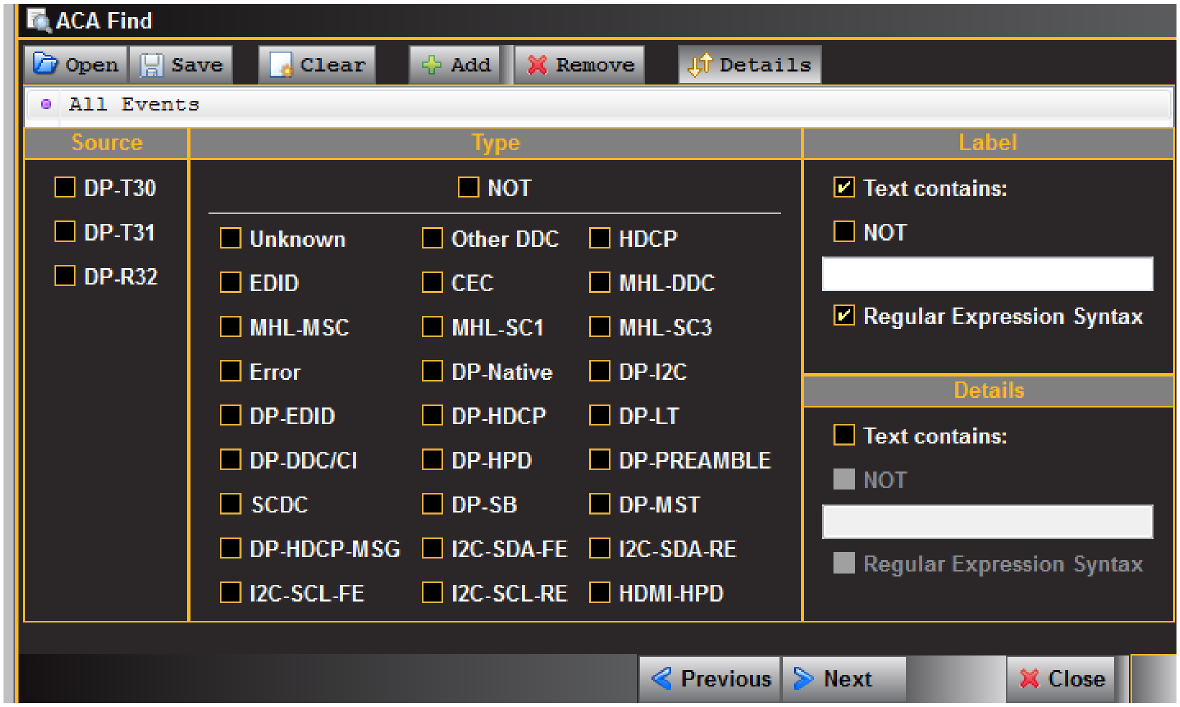
7.8 Using the ACA Find Feature

The **ACA Find** dialog box is accessible through the **Data** pop-out menu shown in the screen example below. The **ACA Find** function enables you to quickly locate different types of events. The ACA Find feature is not available with the **ACA Remote Control** utility. It is only available with the **ACA** feature in the embedded GUI and the **ACA Data Viewer**. If you wish to use the **Find** feature on ACA traces that you have captured using the **ACA Remote Control** utility you have to save the traces as a file and reload them through the **ACA Data Viewer** utility.

You access the **Find** function through the **Data** flyout menu on the control panel of the embedded **ACA utility** and directly from the **Find** button on the control panel of the **ACA Data Viewer**.



The **Find** dialog box is shown below.



Source:
☐ DP-T30
☐ DP-T31
☐ DP-R32

Type:
☐ NOT
☐ Unknown ☐ Other DDC ☐ HDCP
☐ EDID ☐ CEC ☐ MHL-DDC
☐ MHL-MSC ☐ MHL-SC1 ☐ MHL-SC3
☐ Error ☐ DP-Native ☐ DP-I2C
☐ DP-EDID ☐ DP-HDCP ☐ DP-LT
☐ DP-DDC/CI ☐ DP-HPD ☐ DP-PREAMBLE
☐ SCDC ☐ DP-SB ☐ DP-MST
☐ DP-HDCP-MSG ☐ I2C-SDA-FE ☐ I2C-SDA-RE
☐ I2C-SCL-FE ☐ I2C-SCL-RE ☐ HDMI-HPD

Label:
☑ Text contains:
☐ NOT
☑ Regular Expression Syntax

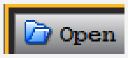
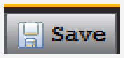
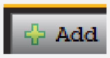
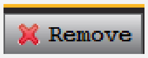
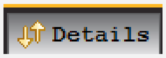
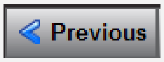
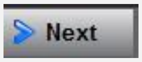
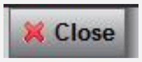
Details:
☐ Text contains:
☐ NOT
☐ Regular Expression Syntax

The **Find** function enables you to select data types in the **Type** field and then search based on text string occurrences in the log record labels or the message details.

Note: For the **ACA** utility on the embedded 980 GUI Manager, you have to Stop the collection of real time trace activity using the Start/Stop button on the right side control panel.

The following table describes the **Find** function buttons, fields and functions.

ACA Find Window

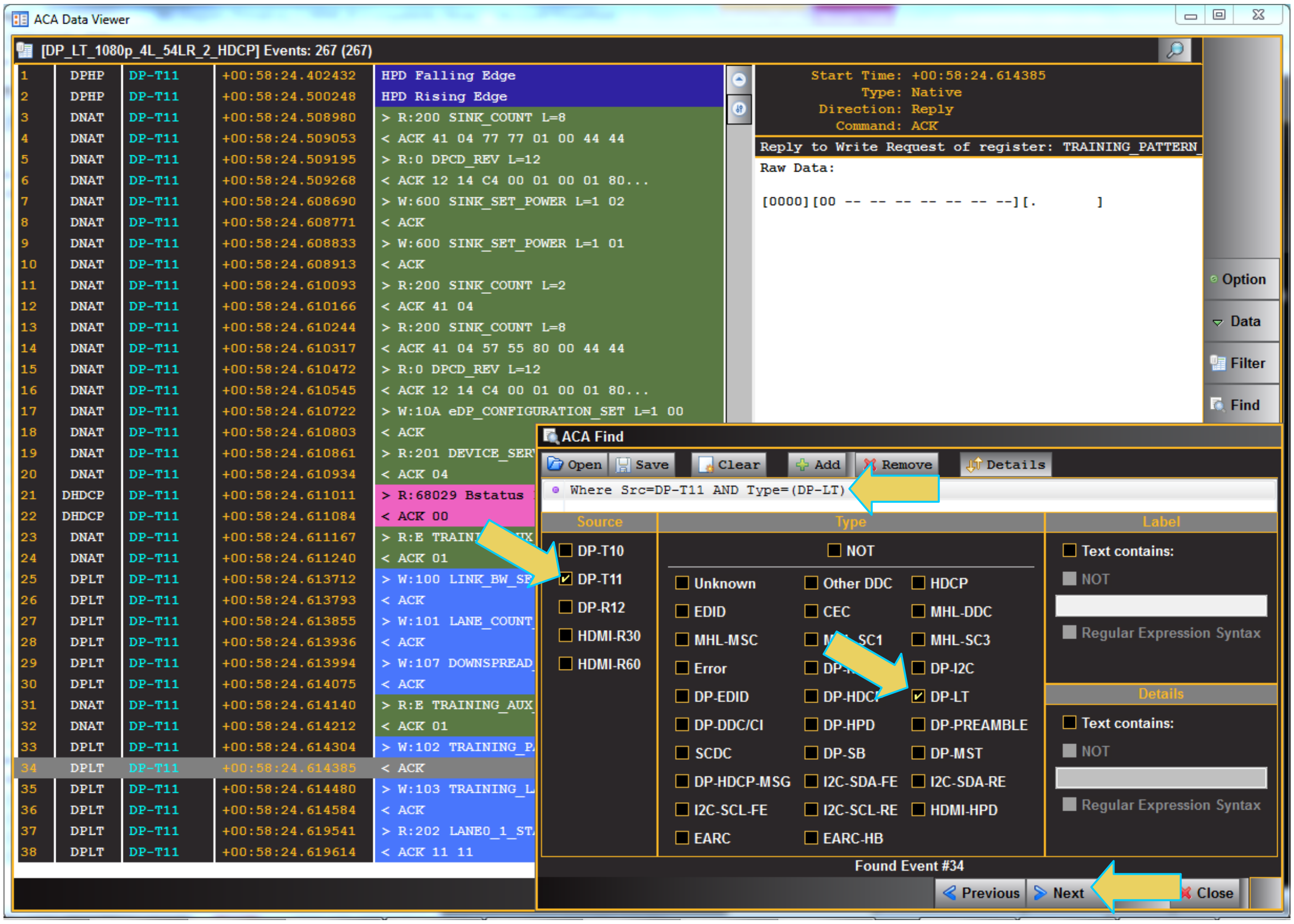
Buttons (Top)	Function	Description
Open 	Opens a stored user created Find configuration.	You can store commonly used search configurations using the Save function and recall them for quick access using the Open button.
Save 	Saves a user created Find configuration.	
Clear 	Clear the existing Find criteria.	You can build up complex Find configurations by concatenating multiple search criteria. When you add multiple configurations they behave as a logical OR function whereby if either of the criteria is True, the search will find an entry. You enter criteria through the embedded touch screen with a pop-up keypad in the ACA real time utility or simply by typing on the external 980 GUI Manager interface. When you are assembling Find configurations you can clear individual configurations by highlighting them in the panel provided and then use the Clear button. You can add through the Add button. You can remove an individual configuration using the Remove button. Example screen shots are shown below.
Add 	Sets the currently defined Find criteria defined in either the Source, Type, Label or Details sub-panels and adds another row for a new Find criteria.	
Remove 	Removes a highlighted Find criterion of an existing Find configuration.	
Details 	Enables or disables the Details panel.	
Buttons (bottom)	**Function**	
Previous 	Enables you to move back to the previous record that meets your search criteria.	
Next 	Enables you to advance to the next record that meets your search criteria.	
Close 	Closes the ACA Find window.	
Fields	**Function**	**Description**
Source	Checkbox to select the port on a particular module that you want to search. Please note that you can collect data in the ACA Trace window from multiple ports.	When you select multiple Source ports they behave as a logical OR function. When you initiate a search, by clicking on the Next or Previous button, the Find function will locate a record matching the criteria. If only the Source (port) is specified the next or previous record from or to that

ACA Find Window		
Buttons (Top)	**Function**	**Description**
		source will be highlighted.
Type	Check boxes enabling you to specify which data types you wish to data types you wish to search through for the string.	When you select multiple data Types they behave as a logical OR function. If only the Type field is specified the next or previous of that data type will be highlighted.
Label	Combination checkboxes and text fields for specifying criteria for text that appears in the Label field of the message. When you enter a criteria in the Label field, it will automatically be added to the set of criteria in the panel above it.	• Text Contains – A checkbox to activate the Label criteria. • Not – A checkbox which when checked will search for records that *do not* meet the criteria in the field beneath it. • Text Field – A text field to enter a string that will be matched (or Not matched). • Regular Expression Syntax – A check box to specify whether the text the Text Field will be treated as plain text or a regular expression. Regular expression syntax is a commonly used set of operators for search text. You can find detailed examples on the web including Wikipedia. If Regular Expression checkbox is checked, you can enter in any regular expression into the text field for a string match.
Details	Combination checkboxes and text fields for specifying criteria for text that appears in the Label field of the message. When you enter a criteria in the Label field, it will automatically be added to the set of criteria in the panel above it.	• Text Contains – A checkbox to activate the Label criteria. • Not – A checkbox which when checked will search for records that *do not* meet the criteria in the field beneath it. • Text Field – A text field to enter a string that will be matched (or Not matched). • Regular Expression Syntax – A check box to specify whether the text the Text Field will be treated as plain text or a regular expression. Regular expression syntax is a commonly used set of operators for search text. You can find detailed examples on the web including Wikipedia. If Regular Expression checkbox is checked, you can enter in any regular expression into the text field for a string match.
Close	Closes the Find window.	

Searching through the ACA trace files with the Find function:

Here are some screen examples of the **Find** function. Note that the screen examples use the **ACA Data Viewer** utility but the embedded **ACA Data Viewer** works the same way. The only difference is the **ACA** embedded utility uses a pop-up keypad.

1. To find all data types from a specific port (interface on the module), enter the following (example uses port T11 transport port 1 or a Link Training transaction).



[DP_LT_1080p_4L_54LR_2_HDCP] Events: 267 (267)

```
1   DPHP   DP-T11  +00:58:24.402432  HPD Falling Edge
2   DPHP   DP-T11  +00:58:24.500248  HPD Rising Edge
3   DNAT   DP-T11  +00:58:24.508980  > R:200 SINK_COUNT L=8
4   DNAT   DP-T11  +00:58:24.509053  < ACK 41 04 77 77 01 00 44 44
5   DNAT   DP-T11  +00:58:24.509195  > R:0 DPCD_REV L=12
6   DNAT   DP-T11  +00:58:24.509268  < ACK 12 14 C4 00 01 00 01 80...
7   DNAT   DP-T11  +00:58:24.608690  > W:600 SINK_SET_POWER L=1 02
8   DNAT   DP-T11  +00:58:24.608771  < ACK
9   DNAT   DP-T11  +00:58:24.608833  > W:600 SINK_SET_POWER L=1 01
10  DNAT   DP-T11  +00:58:24.608913  < ACK
11  DNAT   DP-T11  +00:58:24.610093  > R:200 SINK_COUNT L=2
12  DNAT   DP-T11  +00:58:24.610166  < ACK 41 04
13  DNAT   DP-T11  +00:58:24.610244  > R:200 SINK_COUNT L=8
14  DNAT   DP-T11  +00:58:24.610317  < ACK 41 04 57 55 80 00 44 44
15  DNAT   DP-T11  +00:58:24.610472  > R:0 DPCD_REV L=12
16  DNAT   DP-T11  +00:58:24.610545  < ACK 12 14 C4 00 01 00 01 80...
17  DNAT   DP-T11  +00:58:24.610722  > W:10A eDP_CONFIGURATION_SET L=1 00
18  DNAT   DP-T11  +00:58:24.610803  < ACK
19  DNAT   DP-T11  +00:58:24.610861  > R:201 DEVICE_SER
20  DNAT   DP-T11  +00:58:24.610934  < ACK 04
21  DHDCP  DP-T11  +00:58:24.611011  > R:68029 Bstatus
22  DHDCP  DP-T11  +00:58:24.611084  < ACK 00
23  DNAT   DP-T11  +00:58:24.611167  > R:E TRAIN
24  DNAT   DP-T11  +00:58:24.611240  < ACK 01
25  DPLT   DP-T11  +00:58:24.613712  > W:100 LINK_BW_SE
26  DPLT   DP-T11  +00:58:24.613793  < ACK
27  DPLT   DP-T11  +00:58:24.613855  > W:101 LANE_COUNT_
28  DPLT   DP-T11  +00:58:24.613936  < ACK
29  DPLT   DP-T11  +00:58:24.613994  > W:107 DOWNSPREAD_
30  DPLT   DP-T11  +00:58:24.614075  < ACK
31  DNAT   DP-T11  +00:58:24.614140  > R:E TRAINING_AUX_
32  DNAT   DP-T11  +00:58:24.614212  < ACK 01
33  DPLT   DP-T11  +00:58:24.614304  > W:102 TRAINING_P
34  DPLT   DP-T11  +00:58:24.614385  < ACK
35  DPLT   DP-T11  +00:58:24.614480  > W:103 TRAINING_L
36  DPLT   DP-T11  +00:58:24.614584  < ACK
37  DPLT   DP-T11  +00:58:24.619541  > R:202 LANE0_1_ST
38  DPLT   DP-T11  +00:58:24.619614  < ACK 11 11
```

```
Start Time: +00:58:24.614385
      Type: Native
 Direction: Reply
   Command: ACK
Reply to Write Request of register: TRAINING_PATTERN
Raw Data:

[0000][00 -- -- -- -- -- -- --][.       ]
```

Where Src=DP-T11 AND Type=(DP-LT)

Source:
☐ DP-T10
☑ DP-T11
☐ DP-R12
☐ HDMI-R30
☐ HDMI-R60

Type:
☐ NOT
☐ Unknown
☐ Other DDC
☐ HDCP
☐ EDID
☐ CEC
☐ MHL-DDC
☐ MHL-MSC
☐ MHL-SC1
☐ MHL-SC3
☐ Error
☐ DP-I2C
☐ DP-EDID
☐ DP-HDCP
☑ DP-LT
☐ DP-DDC/CI
☐ DP-HPD
☐ DP-PREAMBLE
☐ SCDC
☐ DP-SB
☐ DP-MST
☐ DP-HDCP-MSG
☐ I2C-SDA-FE
☐ I2C-SDA-RE
☐ I2C-SCL-FE
☐ I2C-SCL-RE
☐ HDMI-HPD
☐ EARC
☐ EARC-HB

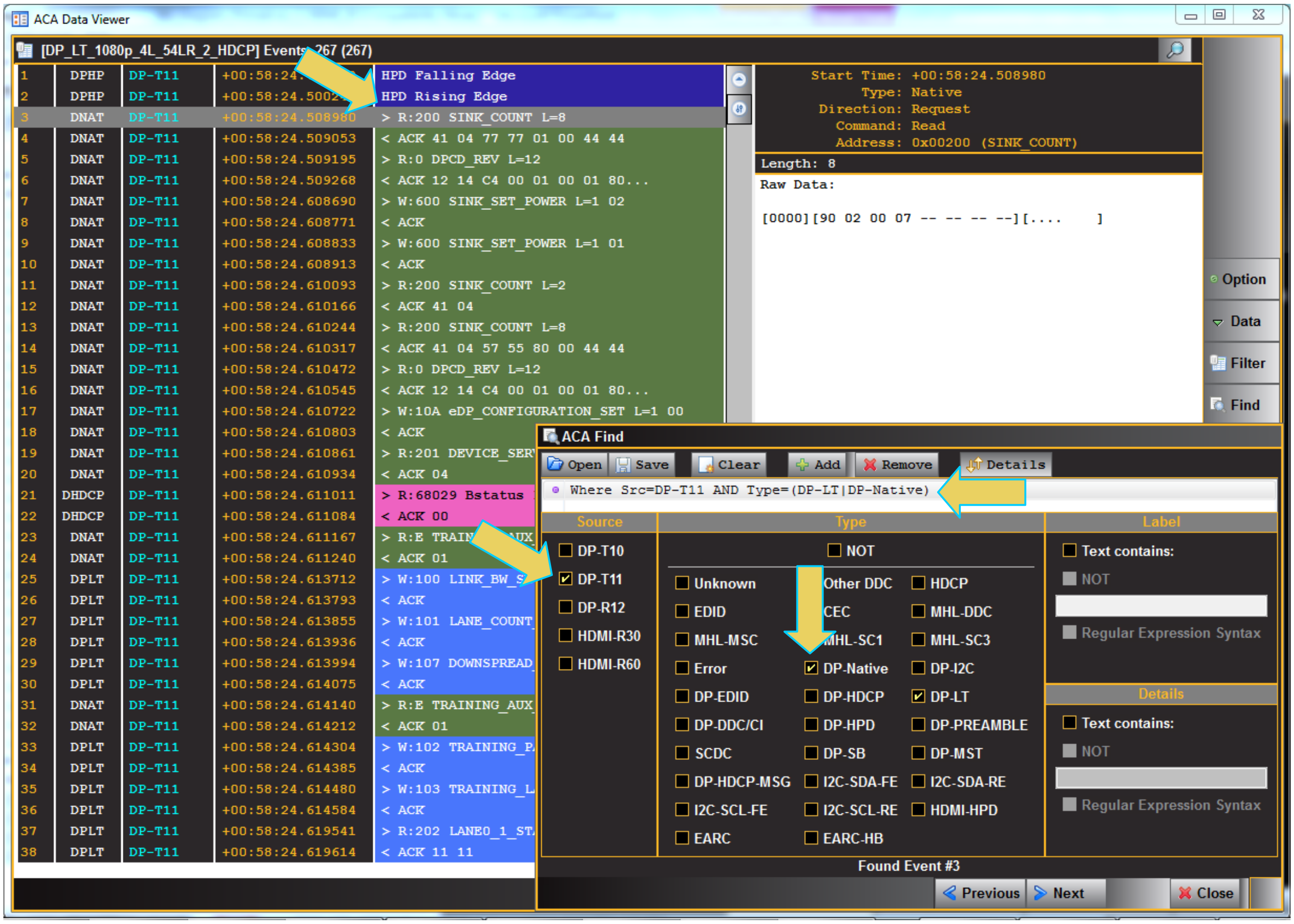
Label:
☐ Text contains:
☐ NOT
☐ Regular Expression Syntax

Details:
☐ Text contains:
☐ NOT
☐ Regular Expression Syntax

Found Event #34

Click on the Next button to advance to the recording meeting that criteria as shown above.

2. To find all data types from a specific port (interface on the module) and that are a DPCD message, enter the following (example uses port T11 transport port 1).



```
1   DPHP   DP-T11  +00:58:24.             HPD Falling Edge
2   DPHP   DP-T11  +00:58:24.5002         HPD Rising Edge
3   DNAT   DP-T11  +00:58:24.508980       > R:200 SINK_COUNT L=8
4   DNAT   DP-T11  +00:58:24.509053       < ACK 41 04 77 77 01 00 44 44
5   DNAT   DP-T11  +00:58:24.509195       > R:0 DPCD_REV L=12
6   DNAT   DP-T11  +00:58:24.509268       < ACK 12 14 C4 00 01 00 01 80...
7   DNAT   DP-T11  +00:58:24.608690       > W:600 SINK_SET_POWER L=1 02
8   DNAT   DP-T11  +00:58:24.608771       < ACK
9   DNAT   DP-T11  +00:58:24.608833       > W:600 SINK_SET_POWER L=1 01
10  DNAT   DP-T11  +00:58:24.608913       < ACK
11  DNAT   DP-T11  +00:58:24.610093       > R:200 SINK_COUNT L=2
12  DNAT   DP-T11  +00:58:24.610166       < ACK 41 04
13  DNAT   DP-T11  +00:58:24.610244       > R:200 SINK_COUNT L=8
14  DNAT   DP-T11  +00:58:24.610317       < ACK 41 04 57 55 80 00 44 44
15  DNAT   DP-T11  +00:58:24.610472       > R:0 DPCD_REV L=12
16  DNAT   DP-T11  +00:58:24.610545       < ACK 12 14 C4 00 01 00 01 80...
17  DNAT   DP-T11  +00:58:24.610722       > W:10A eDP_CONFIGURATION_SET L=1 00
18  DNAT   DP-T11  +00:58:24.610803       < ACK
19  DNAT   DP-T11  +00:58:24.610861       > R:201 DEVICE_SER
20  DNAT   DP-T11  +00:58:24.610934       < ACK 04
21  DHDCP  DP-T11  +00:58:24.611011       > R:68029 Bstatus
22  DHDCP  DP-T11  +00:58:24.611084       < ACK 00
23  DNAT   DP-T11  +00:58:24.611167       > R:E TRAIN    UX
24  DNAT   DP-T11  +00:58:24.611240       < ACK 01
25  DPLT   DP-T11  +00:58:24.613712       > W:100 LINK_BW_S
26  DPLT   DP-T11  +00:58:24.613793       < ACK
27  DPLT   DP-T11  +00:58:24.613855       > W:101 LANE_COUNT_
28  DPLT   DP-T11  +00:58:24.613936       < ACK
29  DPLT   DP-T11  +00:58:24.613994       > W:107 DOWNSPREAD_
30  DPLT   DP-T11  +00:58:24.614075       < ACK
31  DNAT   DP-T11  +00:58:24.614140       > R:E TRAINING_AUX_
32  DNAT   DP-T11  +00:58:24.614212       < ACK 01
33  DPLT   DP-T11  +00:58:24.614304       > W:102 TRAINING_P
34  DPLT   DP-T11  +00:58:24.614385       < ACK
35  DPLT   DP-T11  +00:58:24.614480       > W:103 TRAINING_L
36  DPLT   DP-T11  +00:58:24.614584       < ACK
37  DPLT   DP-T11  +00:58:24.619541       > R:202 LANE0_1_ST
38  DPLT   DP-T11  +00:58:24.619614       < ACK 11 11
```

```
Start Time: +00:58:24.508980
      Type: Native
 Direction: Request
   Command: Read
   Address: 0x00200 (SINK_COUNT)
Length: 8
Raw Data:

[0000][90 02 00 07 -- -- -- --][....    ]
```

```
Where Src=DP-T11 AND Type=(DP-LT|DP-Native)
```

Source
☐ DP-T10
☑ DP-T11
☐ DP-R12
☐ HDMI-R30
☐ HDMI-R60

Type
☐ NOT
☐ Unknown
☐ EDID
☐ MHL-MSC
☐ Error
☐ DP-EDID
☐ DP-DDC/CI
☐ SCDC
☐ DP-HDCP-MSG
☐ I2C-SCL-FE
☐ EARC
☐ Other DDC
☐ CEC
☐ MHL-SC1
☑ DP-Native
☐ DP-HDCP
☐ DP-HPD
☐ DP-SB
☐ I2C-SDA-FE
☐ I2C-SCL-RE
☐ EARC-HB
☐ HDCP
☐ MHL-DDC
☐ MHL-SC3
☐ DP-I2C
☑ DP-LT
☐ DP-PREAMBLE
☐ DP-MST
☐ I2C-SDA-RE
☐ HDMI-HPD

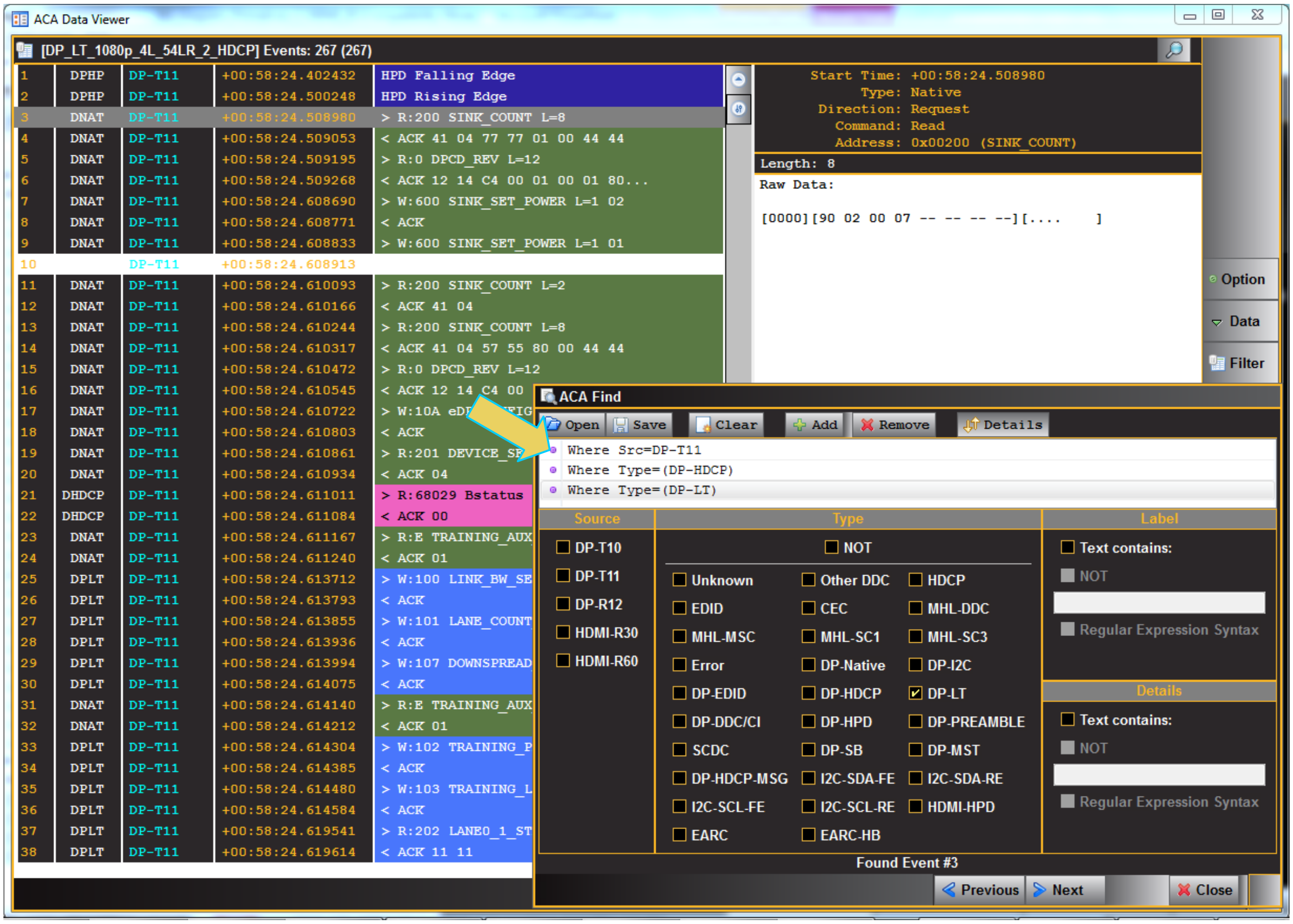
Label
☐ Text contains:
☐ NOT
☐ Regular Expression Syntax

Details
☐ Text contains:
☐ NOT
☐ Regular Expression Syntax

Found Event #3

3. Click on the Next button to advance to the log record meeting that criteria. The result is shown below.

   Note that when you select different data type definitions in the same search configuration, example port type and data Type, the search uses a logical AND function. But if you use two or more distinct definitions, the search will function as a logical OR function as shown on the screen example below.



[DP_LT_1080p_4L_54LR_2_HDCP] Events: 267 (267)

1	DPHP	DP-T11	+00:58:24.402432	HPD Falling Edge
2	DPHP	DP-T11	+00:58:24.500248	HPD Rising Edge
3	DNAT	DP-T11	+00:58:24.508980	> R:200 SINK_COUNT L=8
4	DNAT	DP-T11	+00:58:24.509053	< ACK 41 04 77 77 01 00 44 44
5	DNAT	DP-T11	+00:58:24.509195	> R:0 DPCD_REV L=12
6	DNAT	DP-T11	+00:58:24.509268	< ACK 12 14 C4 00 01 00 01 80...
7	DNAT	DP-T11	+00:58:24.608690	> W:600 SINK_SET_POWER L=1 02
8	DNAT	DP-T11	+00:58:24.608771	< ACK
9	DNAT	DP-T11	+00:58:24.608833	> W:600 SINK_SET_POWER L=1 01
10		DP-T11	+00:58:24.608913	
11	DNAT	DP-T11	+00:58:24.610093	> R:200 SINK_COUNT L=2
12	DNAT	DP-T11	+00:58:24.610166	< ACK 41 04
13	DNAT	DP-T11	+00:58:24.610244	> R:200 SINK_COUNT L=8
14	DNAT	DP-T11	+00:58:24.610317	< ACK 41 04 57 55 80 00 44 44
15	DNAT	DP-T11	+00:58:24.610472	> R:0 DPCD_REV L=12
16	DNAT	DP-T11	+00:58:24.610545	< ACK 12 14 C4 00
17	DNAT	DP-T11	+00:58:24.610722	> W:10A eD
18	DNAT	DP-T11	+00:58:24.610803	< ACK
19	DNAT	DP-T11	+00:58:24.610861	> R:201 DEVICE_S
20	DNAT	DP-T11	+00:58:24.610934	< ACK 04
21	DHDCP	DP-T11	+00:58:24.611011	> R:68029 Bstatus
22	DHDCP	DP-T11	+00:58:24.611084	< ACK 00
23	DNAT	DP-T11	+00:58:24.611167	> R:E TRAINING_AUX
24	DNAT	DP-T11	+00:58:24.611240	< ACK 01
25	DPLT	DP-T11	+00:58:24.613712	> W:100 LINK_BW_SE
26	DPLT	DP-T11	+00:58:24.613793	< ACK
27	DPLT	DP-T11	+00:58:24.613855	> W:101 LANE_COUNT
28	DPLT	DP-T11	+00:58:24.613936	< ACK
29	DPLT	DP-T11	+00:58:24.613994	> W:107 DOWNSPREAD
30	DPLT	DP-T11	+00:58:24.614075	< ACK
31	DNAT	DP-T11	+00:58:24.614140	> R:E TRAINING_AUX
32	DNAT	DP-T11	+00:58:24.614212	< ACK 01
33	DPLT	DP-T11	+00:58:24.614304	> W:102 TRAINING_P
34	DPLT	DP-T11	+00:58:24.614385	< ACK
35	DPLT	DP-T11	+00:58:24.614480	> W:103 TRAINING_L
36	DPLT	DP-T11	+00:58:24.614584	< ACK
37	DPLT	DP-T11	+00:58:24.619541	> R:202 LANE0_1_ST
38	DPLT	DP-T11	+00:58:24.619614	< ACK 11 11

```
 Start Time: +00:58:24.508980
       Type: Native
  Direction: Request
    Command: Read
    Address: 0x00200 (SINK_COUNT)
Length: 8
Raw Data:

[0000][90 02 00 07 -- -- -- --][....    ]
```

- Where Src=DP-T11
- Where Type=(DP-HDCP)
- Where Type=(DP-LT)

Source

☐ DP-T10
☐ DP-T11
☐ DP-R12
☐ HDMI-R30
☐ HDMI-R60

Type

☐ NOT

☐ Unknown	☐ Other DDC	☐ HDCP
☐ EDID	☐ CEC	☐ MHL-DDC
☐ MHL-MSC	☐ MHL-SC1	☐ MHL-SC3
☐ Error	☐ DP-Native	☐ DP-I2C
☐ DP-EDID	☐ DP-HDCP	☑ DP-LT
☐ DP-DDC/CI	☐ DP-HPD	☐ DP-PREAMBLE
☐ SCDC	☐ DP-SB	☐ DP-MST
☐ DP-HDCP-MSG	☐ I2C-SDA-FE	☐ I2C-SDA-RE
☐ I2C-SCL-FE	☐ I2C-SCL-RE	☐ HDMI-HPD
☐ EARC	☐ EARC-HB	

Label

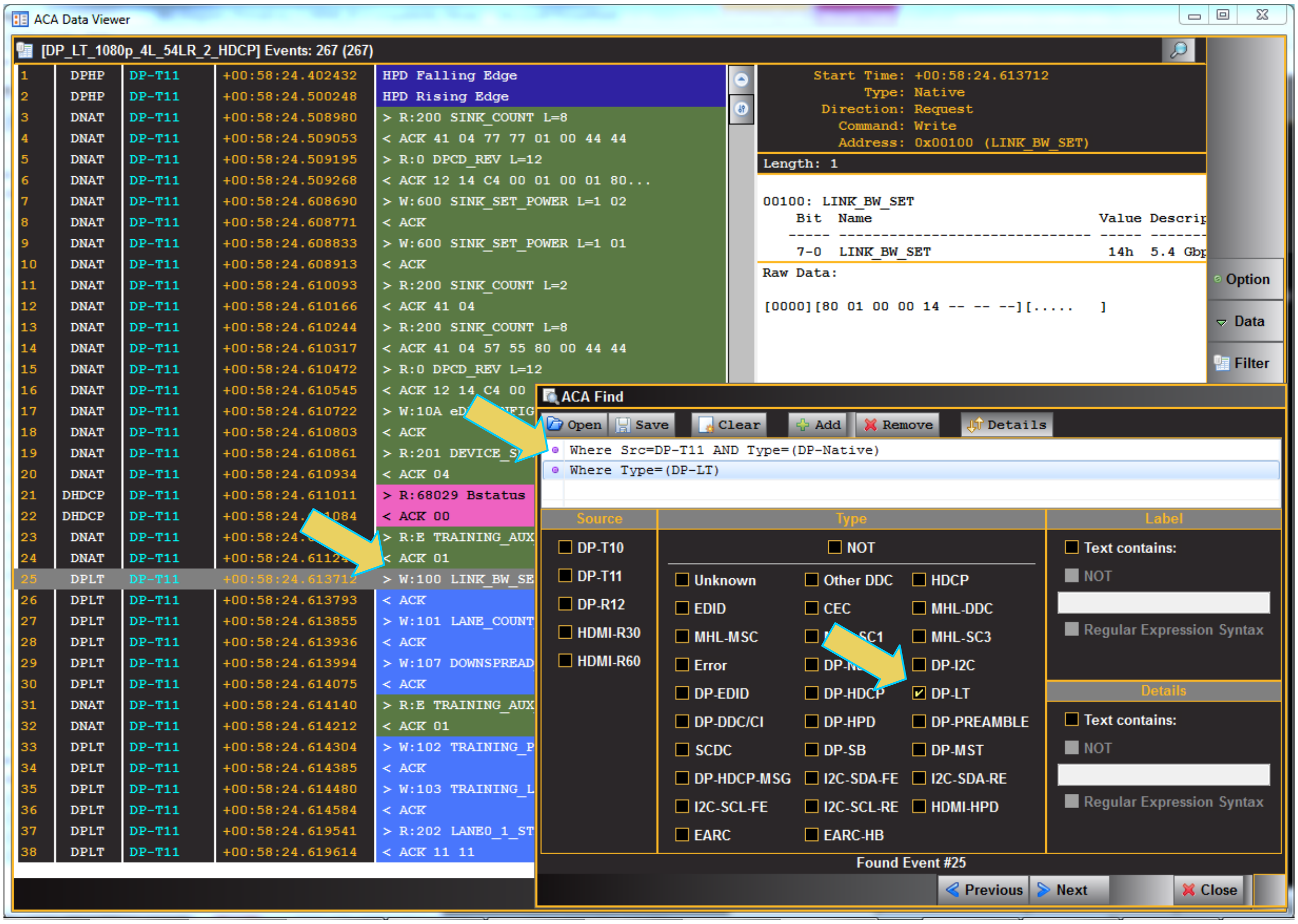
☐ Text contains:
☐ NOT
☐ Regular Expression Syntax

Details

☐ Text contains:
☐ NOT
☐ Regular Expression Syntax

Found Event #3

If you specify one or more data types in the **Type** field and enter a string in the **Label** text field in the same search configuration, the search will behave as a logical OR for the data types and a logical AND with the **Type** and the **Label** field as shown below.



[DP_LT_1080p_4L_54LR_2_HDCP] Events: 267 (267)

```
1   DPHP   DP-T11  +00:58:24.402432  HPD Falling Edge
2   DPHP   DP-T11  +00:58:24.500248  HPD Rising Edge
3   DNAT   DP-T11  +00:58:24.508980  > R:200 SINK_COUNT L=8
4   DNAT   DP-T11  +00:58:24.509053  < ACK 41 04 77 77 01 00 44 44
5   DNAT   DP-T11  +00:58:24.509195  > R:0 DPCD_REV L=12
6   DNAT   DP-T11  +00:58:24.509268  < ACK 12 14 C4 00 01 00 01 80...
7   DNAT   DP-T11  +00:58:24.608690  > W:600 SINK_SET_POWER L=1 02
8   DNAT   DP-T11  +00:58:24.608771  < ACK
9   DNAT   DP-T11  +00:58:24.608833  > W:600 SINK_SET_POWER L=1 01
10  DNAT   DP-T11  +00:58:24.608913  < ACK
11  DNAT   DP-T11  +00:58:24.610093  > R:200 SINK_COUNT L=2
12  DNAT   DP-T11  +00:58:24.610166  < ACK 41 04
13  DNAT   DP-T11  +00:58:24.610244  > R:200 SINK_COUNT L=8
14  DNAT   DP-T11  +00:58:24.610317  < ACK 41 04 57 55 80 00 44 44
15  DNAT   DP-T11  +00:58:24.610472  > R:0 DPCD_REV L=12
16  DNAT   DP-T11  +00:58:24.610545  < ACK 12 14 C4 00
17  DNAT   DP-T11  +00:58:24.610722  > W:10A eD    NFIG
18  DNAT   DP-T11  +00:58:24.610803  < ACK
19  DNAT   DP-T11  +00:58:24.610861  > R:201 DEVICE_S
20  DNAT   DP-T11  +00:58:24.610934  < ACK 04
21  DHDCP  DP-T11  +00:58:24.611011  > R:68029 Bstatus
22  DHDCP  DP-T11  +00:58:24.  1084  < ACK 00
23  DNAT   DP-T11  +00:58:24.        > R:E TRAINING_AUX
24  DNAT   DP-T11  +00:58:24.6112    < ACK 01
25  DPLT   DP-T11  +00:58:24.613712  > W:100 LINK_BW_SE
26  DPLT   DP-T11  +00:58:24.613793  < ACK
27  DPLT   DP-T11  +00:58:24.613855  > W:101 LANE_COUNT
28  DPLT   DP-T11  +00:58:24.613936  < ACK
29  DPLT   DP-T11  +00:58:24.613994  > W:107 DOWNSPREAD
30  DPLT   DP-T11  +00:58:24.614075  < ACK
31  DNAT   DP-T11  +00:58:24.614140  > R:E TRAINING_AUX
32  DNAT   DP-T11  +00:58:24.614212  < ACK 01
33  DPLT   DP-T11  +00:58:24.614304  > W:102 TRAINING_P
34  DPLT   DP-T11  +00:58:24.614385  < ACK
35  DPLT   DP-T11  +00:58:24.614480  > W:103 TRAINING_L
36  DPLT   DP-T11  +00:58:24.614584  < ACK
37  DPLT   DP-T11  +00:58:24.619541  > R:202 LANE0_1_ST
38  DPLT   DP-T11  +00:58:24.619614  < ACK 11 11
```

```
   Start Time: +00:58:24.613712
         Type: Native
    Direction: Request
      Command: Write
      Address: 0x00100 (LINK_BW_SET)
Length: 1

00100: LINK_BW_SET
    Bit  Name                                Value Descrip
   ----- ----------------------------------- ----- -------
    7-0  LINK_BW_SET                           14h  5.4 Gbp
Raw Data:

[0000][80 01 00 00 14 -- -- --][.....   ]
```

```
Where Src=DP-T11 AND Type=(DP-Native)
Where Type=(DP-LT)
```

Source
- ☐ DP-T10
- ☐ DP-T11
- ☐ DP-R12
- ☐ HDMI-R30
- ☐ HDMI-R60

Type

☐ NOT

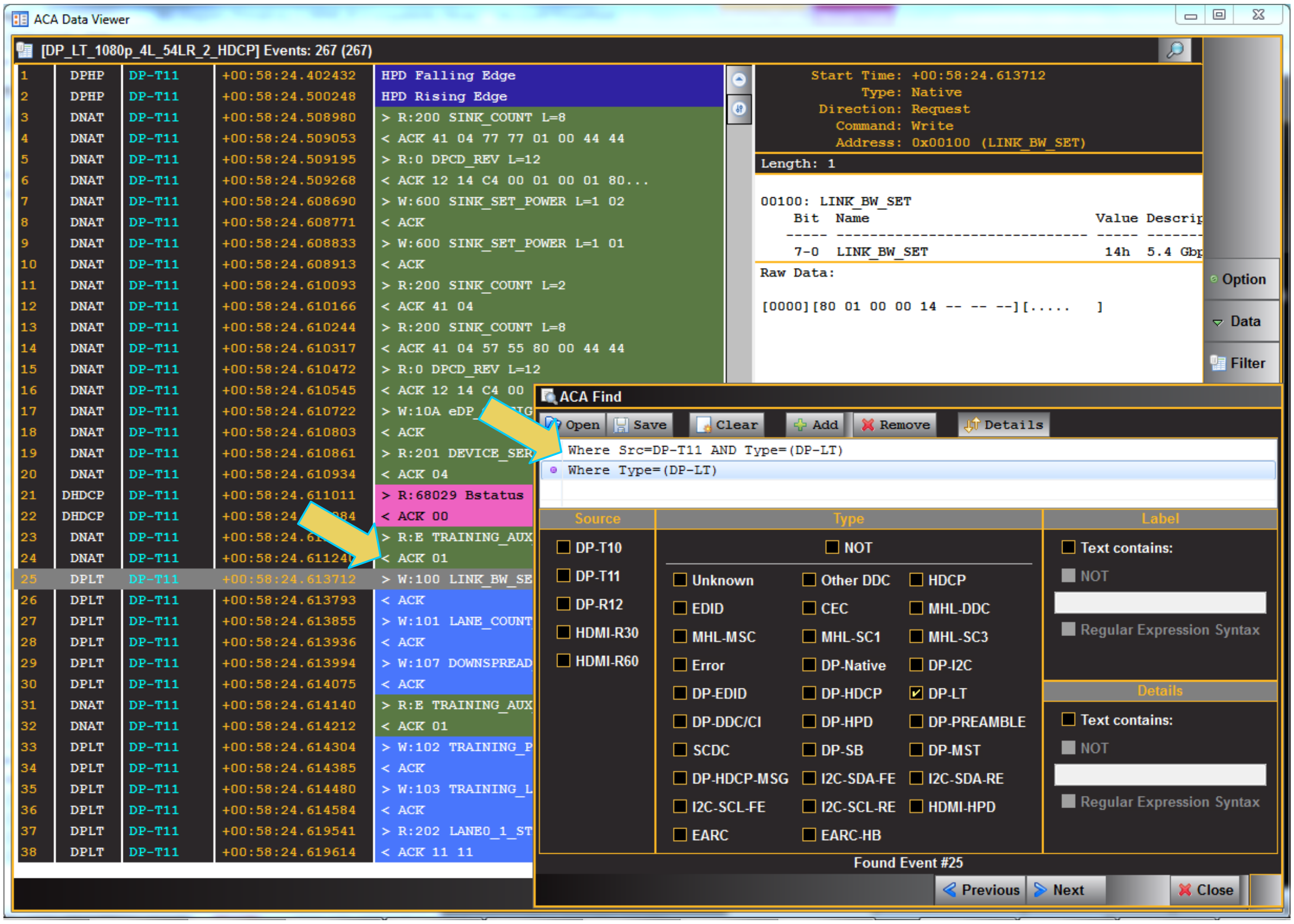
☐ Unknown	☐ Other DDC	☐ HDCP
☐ EDID	☐ CEC	☐ MHL-DDC
☐ MHL-MSC	☐ SC1	☐ MHL-SC3
☐ Error	☐ DP-N	☐ DP-I2C
☐ DP-EDID	☐ DP-HDCP	☑ DP-LT
☐ DP-DDC/CI	☐ DP-HPD	☐ DP-PREAMBLE
☐ SCDC	☐ DP-SB	☐ DP-MST
☐ DP-HDCP-MSG	☐ I2C-SDA-FE	☐ I2C-SDA-RE
☐ I2C-SCL-FE	☐ I2C-SCL-RE	☐ HDMI-HPD
☐ EARC	☐ EARC-HB	

Label
- ☐ Text contains:
- ☐ NOT
- ☐ Regular Expression Syntax

Details
- ☐ Text contains:
- ☐ NOT
- ☐ Regular Expression Syntax

Found Event #25

However, if you enter these same criteria using separate configurations as shown below, the search will behave as a logical OR function.



[DP_LT_1080p_4L_54LR_2_HDCP] Events: 267 (267)

```
1   DPHP   DP-T11  +00:58:24.402432  HPD Falling Edge
2   DPHP   DP-T11  +00:58:24.500248  HPD Rising Edge
3   DNAT   DP-T11  +00:58:24.508980  > R:200 SINK_COUNT L=8
4   DNAT   DP-T11  +00:58:24.509053  < ACK 41 04 77 77 01 00 44 44
5   DNAT   DP-T11  +00:58:24.509195  > R:0 DPCD_REV L=12
6   DNAT   DP-T11  +00:58:24.509268  < ACK 12 14 C4 00 01 00 01 80...
7   DNAT   DP-T11  +00:58:24.608690  > W:600 SINK_SET_POWER L=1 02
8   DNAT   DP-T11  +00:58:24.608771  < ACK
9   DNAT   DP-T11  +00:58:24.608833  > W:600 SINK_SET_POWER L=1 01
10  DNAT   DP-T11  +00:58:24.608913  < ACK
11  DNAT   DP-T11  +00:58:24.610093  > R:200 SINK_COUNT L=2
12  DNAT   DP-T11  +00:58:24.610166  < ACK 41 04
13  DNAT   DP-T11  +00:58:24.610244  > R:200 SINK_COUNT L=8
14  DNAT   DP-T11  +00:58:24.610317  < ACK 41 04 57 55 80 00 44 44
15  DNAT   DP-T11  +00:58:24.610472  > R:0 DPCD_REV L=12
16  DNAT   DP-T11  +00:58:24.610545  < ACK 12 14 C4 00
17  DNAT   DP-T11  +00:58:24.610722  > W:10A eDP_
18  DNAT   DP-T11  +00:58:24.610803  < ACK
19  DNAT   DP-T11  +00:58:24.610861  > R:201 DEVICE_SER
20  DNAT   DP-T11  +00:58:24.610934  < ACK 04
21  DHDCP  DP-T11  +00:58:24.611011  > R:68029 Bstatus
22  DHDCP  DP-T11  +00:58:24.    84  < ACK 00
23  DNAT   DP-T11  +00:58:24.61      > R:E TRAINING_AUX
24  DNAT   DP-T11  +00:58:24.61124   < ACK 01
25  DPLT   DP-T11  +00:58:24.613712  > W:100 LINK_BW_SE
26  DPLT   DP-T11  +00:58:24.613793  < ACK
27  DPLT   DP-T11  +00:58:24.613855  > W:101 LANE_COUNT
28  DPLT   DP-T11  +00:58:24.613936  < ACK
29  DPLT   DP-T11  +00:58:24.613994  > W:107 DOWNSPREAD
30  DPLT   DP-T11  +00:58:24.614075  < ACK
31  DNAT   DP-T11  +00:58:24.614140  > R:E TRAINING_AUX
32  DNAT   DP-T11  +00:58:24.614212  < ACK 01
33  DPLT   DP-T11  +00:58:24.614304  > W:102 TRAINING_P
34  DPLT   DP-T11  +00:58:24.614385  < ACK
35  DPLT   DP-T11  +00:58:24.614480  > W:103 TRAINING_L
36  DPLT   DP-T11  +00:58:24.614584  < ACK
37  DPLT   DP-T11  +00:58:24.619541  > R:202 LANE0_1_ST
38  DPLT   DP-T11  +00:58:24.619614  < ACK 11 11
```

```
     Start Time: +00:58:24.613712
           Type: Native
      Direction: Request
        Command: Write
        Address: 0x00100 (LINK_BW_SET)
Length: 1

00100: LINK_BW_SET
    Bit  Name                              Value Descrip
   ----- -------------------------------- ----- -------
    7-0  LINK_BW_SET                        14h  5.4 Gbp
Raw Data:

[0000][80 01 00 00 14 -- -- --][.....   ]
```

```
Where Src=DP-T11 AND Type=(DP-LT)
Where Type=(DP-LT)
```

Source
- ☐ DP-T10
- ☐ DP-T11
- ☐ DP-R12
- ☐ HDMI-R30
- ☐ HDMI-R60

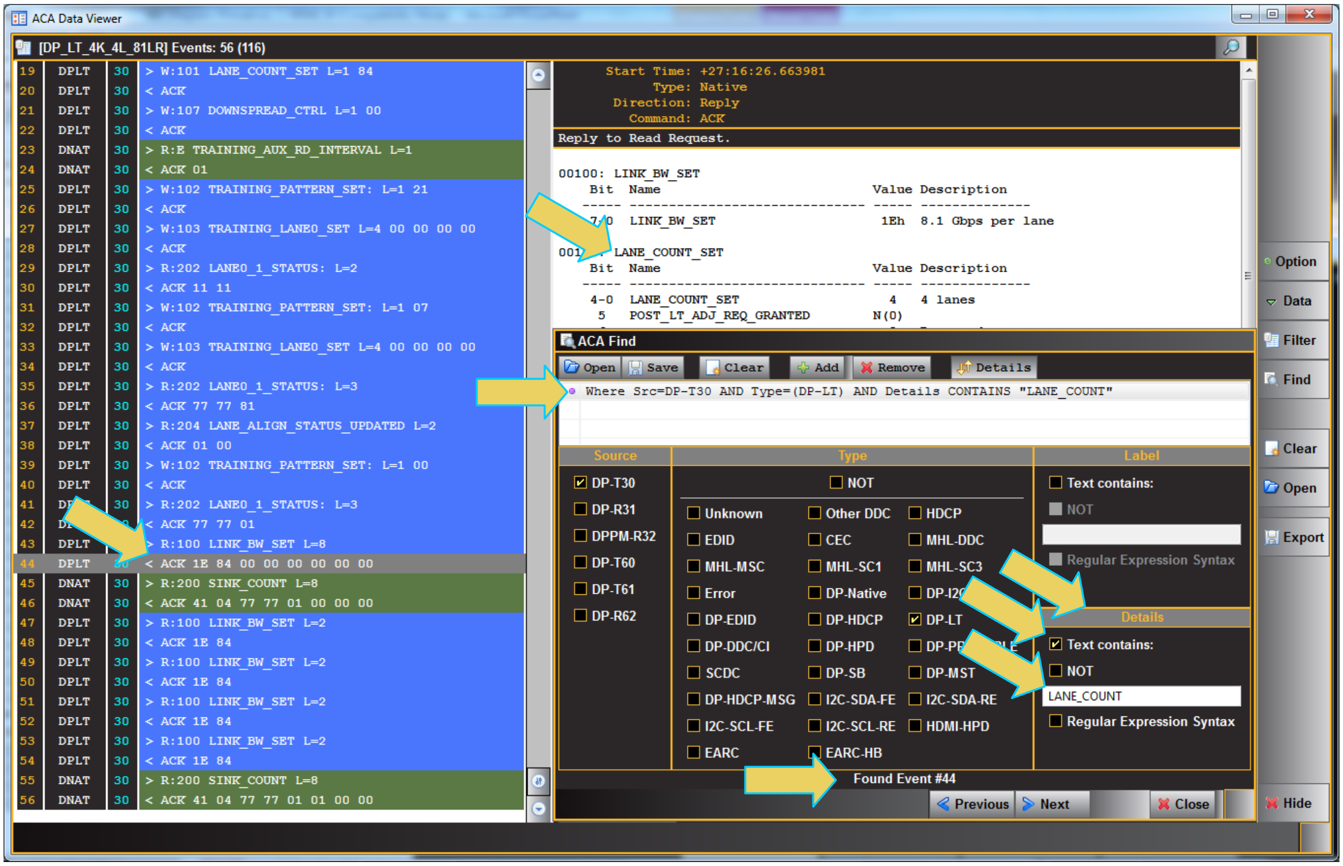
Type
- ☐ NOT
- ☐ Unknown ☐ Other DDC ☐ HDCP
- ☐ EDID ☐ CEC ☐ MHL-DDC
- ☐ MHL-MSC ☐ MHL-SC1 ☐ MHL-SC3
- ☐ Error ☐ DP-Native ☐ DP-I2C
- ☐ DP-EDID ☐ DP-HDCP ☑ DP-LT
- ☐ DP-DDC/CI ☐ DP-HPD ☐ DP-PREAMBLE
- ☐ SCDC ☐ DP-SB ☐ DP-MST
- ☐ DP-HDCP-MSG ☐ I2C-SDA-FE ☐ I2C-SDA-RE
- ☐ I2C-SCL-FE ☐ I2C-SCL-RE ☐ HDMI-HPD
- ☐ EARC ☐ EARC-HB

Label
- ☐ Text contains:
- ☐ NOT
- ☐ Regular Expression Syntax

Details
- ☐ Text contains:
- ☐ NOT
- ☐ Regular Expression Syntax

Found Event #25

You can also search through the **Details** panel of a record. The following examples depicts this. In this example, we have also restricted the search to the DP Tx1 port (DP-T30).



[DP_LT_4K_4L_81LR] Events: 56 (116)

```
19  DPLT  30  > W:101 LANE_COUNT_SET L=1 84
20  DPLT  30  < ACK
21  DPLT  30  > W:107 DOWNSPREAD_CTRL L=1 00
22  DPLT  30  < ACK
23  DNAT  30  > R:E TRAINING_AUX_RD_INTERVAL L=1
24  DNAT  30  < ACK 01
25  DPLT  30  > W:102 TRAINING_PATTERN_SET: L=1 21
26  DPLT  30  < ACK
27  DPLT  30  > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
28  DPLT  30  < ACK
29  DPLT  30  > R:202 LANE0_1_STATUS: L=2
30  DPLT  30  < ACK 11 11
31  DPLT  30  > W:102 TRAINING_PATTERN_SET: L=1 07
32  DPLT  30  < ACK
33  DPLT  30  > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
34  DPLT  30  < ACK
35  DPLT  30  > R:202 LANE0_1_STATUS: L=3
36  DPLT  30  < ACK 77 77 81
37  DPLT  30  > R:204 LANE_ALIGN_STATUS_UPDATED L=2
38  DPLT  30  < ACK 01 00
39  DPLT  30  > W:102 TRAINING_PATTERN_SET: L=1 00
40  DPLT  30  < ACK
41  DP    30  > R:202 LANE0_1_STATUS: L=3
42  D         < ACK 77 77 01
43  DPLT      > R:100 LINK_BW_SET L=8
44  DPLT      < ACK 1E 84 00 00 00 00 00 00
45  DNAT  30  > R:200 SINK_COUNT L=8
46  DNAT  30  < ACK 41 04 77 77 01 00 00 00
47  DPLT  30  > R:100 LINK_BW_SET L=2
48  DPLT  30  < ACK 1E 84
49  DPLT  30  > R:100 LINK_BW_SET L=2
50  DPLT  30  < ACK 1E 84
51  DPLT  30  > R:100 LINK_BW_SET L=2
52  DPLT  30  < ACK 1E 84
53  DPLT  30  > R:100 LINK_BW_SET L=2
54  DPLT  30  < ACK 1E 84
55  DNAT  30  > R:200 SINK_COUNT L=8
56  DNAT  30  < ACK 41 04 77 77 01 01 00 00
```

```
  Start Time: +27:16:26.663981
        Type: Native
   Direction: Reply
     Command: ACK
Reply to Read Request.

00100: LINK_BW_SET
    Bit   Name                           Value Description
   ----- ------------------------------ ----- -------------
    7 0   LINK_BW_SET                     1Eh  8.1 Gbps per lane

001     LANE_COUNT_SET
    Bit   Name                           Value Description
   ----- ------------------------------ ----- -------------
    4-0   LANE_COUNT_SET                   4   4 lanes
     5    POST_LT_ADJ_REQ_GRANTED        N(0)
```

```
Where Src=DP-T30 AND Type=(DP-LT) AND Details CONTAINS "LANE_COUNT"
```

Source

- ☑ DP-T30
- ☐ DP-R31
- ☐ DPPM-R32
- ☐ DP-T60
- ☐ DP-T61
- ☐ DP-R62

Type

☐ NOT

☐ Unknown	☐ Other DDC	☐ HDCP
☐ EDID	☐ CEC	☐ MHL-DDC
☐ MHL-MSC	☐ MHL-SC1	☐ MHL-SC3
☐ Error	☐ DP-Native	☐ DP-I2C
☐ DP-EDID	☐ DP-HDCP	☑ DP-LT
☐ DP-DDC/CI	☐ DP-HPD	☐ DP-P
☐ SCDC	☐ DP-SB	☐ DP-MST
☐ DP-HDCP-MSG	☐ I2C-SDA-FE	☐ I2C-SDA-RE
☐ I2C-SCL-FE	☐ I2C-SCL-RE	☐ HDMI-HPD
☐ EARC	☐ EARC-HB	

Label

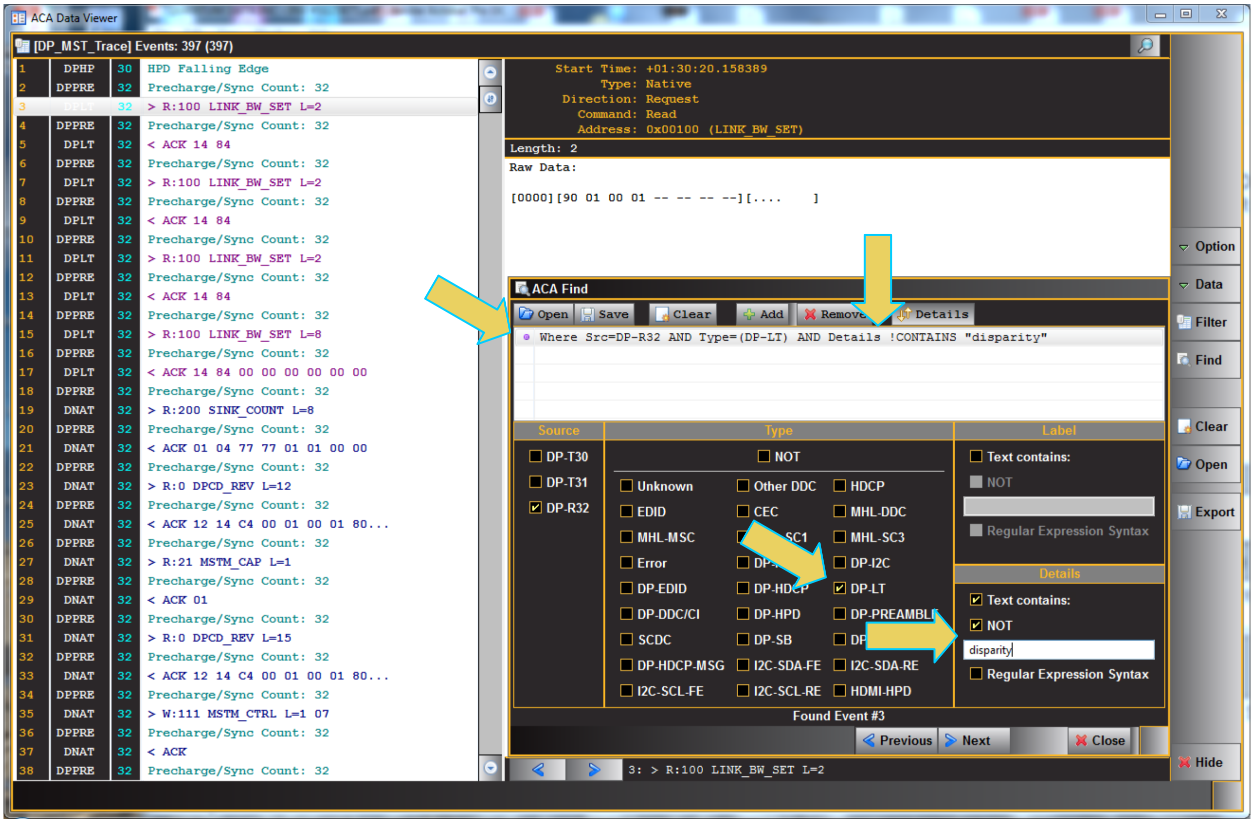
- ☐ Text contains:
- ☐ NOT
- ☐ Regular Expression Syntax

Details

- ☑ Text contains:
- ☐ NOT
- LANE_COUNT
- ☐ Regular Expression Syntax

Found Event #44

You can also conduct a string search with a NOT function to exclude message labels or details that contain a specific string. The following example shows this feature.



[DP_MST_Trace] Events: 397 (397)

```
1   DPHP   30 HPD Falling Edge
2   DPPRE  32 Precharge/Sync Count: 32
3   DPLT   32 > R:100 LINK_BW_SET L=2
4   DPPRE  32 Precharge/Sync Count: 32
5   DPLT   32 < ACK 14 84
6   DPPRE  32 Precharge/Sync Count: 32
7   DPLT   32 > R:100 LINK_BW_SET L=2
8   DPPRE  32 Precharge/Sync Count: 32
9   DPLT   32 < ACK 14 84
10  DPPRE  32 Precharge/Sync Count: 32
11  DPLT   32 > R:100 LINK_BW_SET L=2
12  DPPRE  32 Precharge/Sync Count: 32
13  DPLT   32 < ACK 14 84
14  DPPRE  32 Precharge/Sync Count: 32
15  DPLT   32 > R:100 LINK_BW_SET L=8
16  DPPRE  32 Precharge/Sync Count: 32
17  DPLT   32 < ACK 14 84 00 00 00 00 00 00
18  DPPRE  32 Precharge/Sync Count: 32
19  DNAT   32 > R:200 SINK_COUNT L=8
20  DPPRE  32 Precharge/Sync Count: 32
21  DNAT   32 < ACK 01 04 77 77 01 01 00 00
22  DPPRE  32 Precharge/Sync Count: 32
23  DNAT   32 > R:0 DPCD_REV L=12
24  DPPRE  32 Precharge/Sync Count: 32
25  DNAT   32 < ACK 12 14 C4 00 01 00 01 80...
26  DPPRE  32 Precharge/Sync Count: 32
27  DNAT   32 > R:21 MSTM_CAP L=1
28  DPPRE  32 Precharge/Sync Count: 32
29  DNAT   32 < ACK 01
30  DPPRE  32 Precharge/Sync Count: 32
31  DNAT   32 > R:0 DPCD_REV L=15
32  DPPRE  32 Precharge/Sync Count: 32
33  DNAT   32 < ACK 12 14 C4 00 01 00 01 80...
34  DPPRE  32 Precharge/Sync Count: 32
35  DNAT   32 > W:111 MSTM_CTRL L=1 07
36  DPPRE  32 Precharge/Sync Count: 32
37  DNAT   32 < ACK
38  DPPRE  32 Precharge/Sync Count: 32
```

```
Start Time: +01:30:20.158389
      Type: Native
 Direction: Request
   Command: Read
   Address: 0x00100 (LINK_BW_SET)
Length: 2
Raw Data:

[0000][90 01 00 01 -- -- -- --][....    ]
```

```
Where Src=DP-R32 AND Type=(DP-LT) AND Details !CONTAINS "disparity"
```

Source
- ☐ DP-T30
- ☐ DP-T31
- ☑ DP-R32

Type
- ☐ NOT
- ☐ Unknown ☐ Other DDC ☐ HDCP
- ☐ EDID ☐ CEC ☐ MHL-DDC
- ☐ MHL-MSC ☐ …SC1 ☐ MHL-SC3
- ☐ Error ☐ DP-… ☐ DP-I2C
- ☐ DP-EDID ☐ DP-HDCP ☑ DP-LT
- ☐ DP-DDC/CI ☐ DP-HPD ☐ DP-PREAMBLE
- ☐ SCDC ☐ DP-SB ☐ DP…
- ☐ DP-HDCP-MSG ☐ I2C-SDA-FE ☐ I2C-SDA-RE
- ☐ I2C-SCL-FE ☐ I2C-SCL-RE ☐ HDMI-HPD

Label
- ☐ Text contains:
- ☐ NOT
- ☐ Regular Expression Syntax

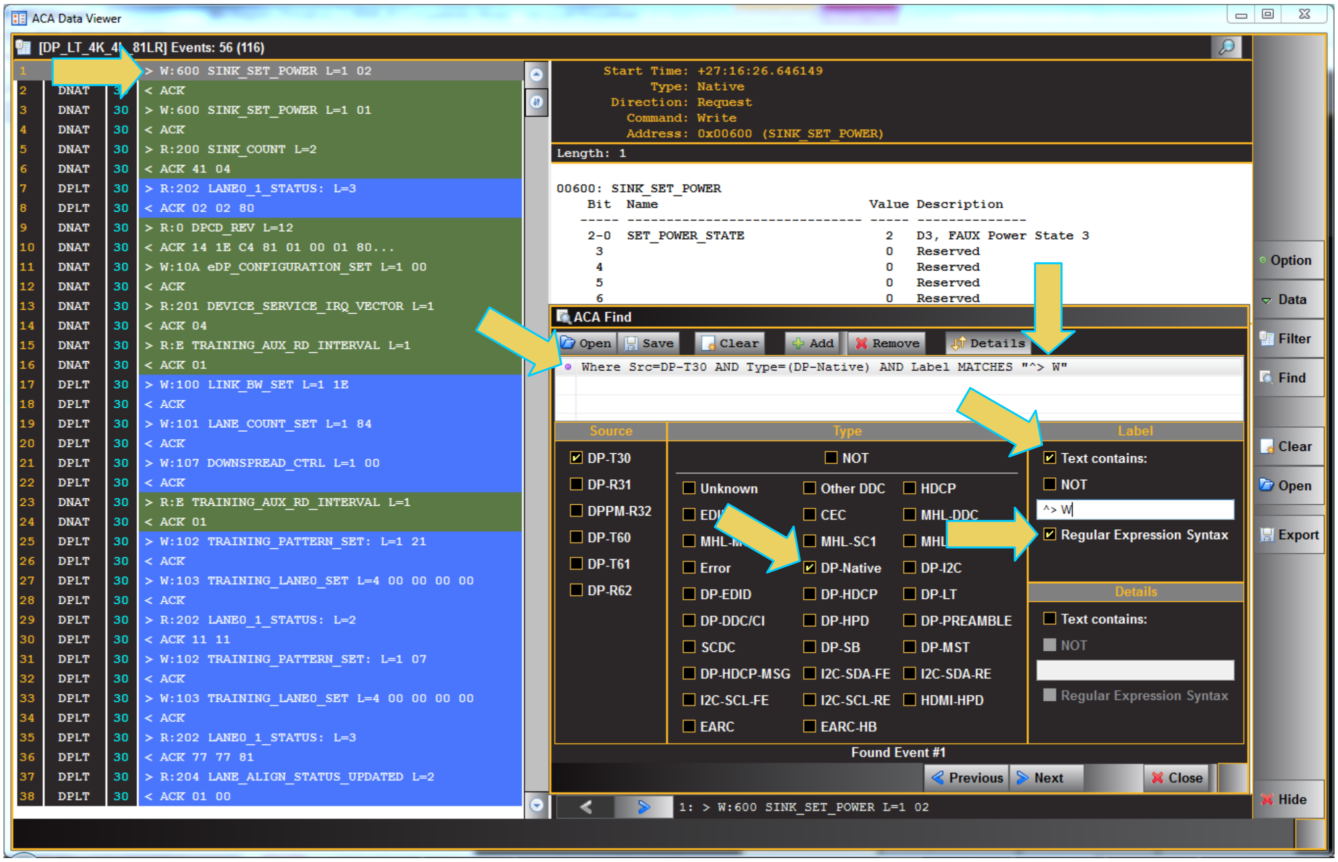
Details
- ☑ Text contains:
- ☑ NOT
- disparity
- ☐ Regular Expression Syntax

Found Event #3

3: > R:100 LINK_BW_SET L=2

You can use regular expressions as well in either the **Label** field or the **Details** field. The following example shows how you can advance to DisplayPort Native transaction that contains the string “^> W” at the beginning (^ operator) of it.

Note: The $ operator would select a **Label** with some text at the end of the **Label**.



```
[DP_LT_4K_4 81LR] Events: 56 (116)
1                 > W:600 SINK_SET_POWER L=1 02
2   DNAT   3      < ACK
3   DNAT   30     > W:600 SINK_SET_POWER L=1 01
4   DNAT   30     < ACK
5   DNAT   30     > R:200 SINK_COUNT L=2
6   DNAT   30     < ACK 41 04
7   DPLT   30     > R:202 LANE0_1_STATUS: L=3
8   DPLT   30     < ACK 02 02 80
9   DNAT   30     > R:0 DPCD_REV L=12
10  DNAT   30     < ACK 14 1E C4 81 01 00 01 80...
11  DNAT   30     > W:10A eDP_CONFIGURATION_SET L=1 00
12  DNAT   30     < ACK
13  DNAT   30     > R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
14  DNAT   30     < ACK 04
15  DNAT   30     > R:E TRAINING_AUX_RD_INTERVAL L=1
16  DNAT   30     < ACK 01
17  DPLT   30     > W:100 LINK_BW_SET L=1 1E
18  DPLT   30     < ACK
19  DPLT   30     > W:101 LANE_COUNT_SET L=1 84
20  DPLT   30     < ACK
21  DPLT   30     > W:107 DOWNSPREAD_CTRL L=1 00
22  DPLT   30     < ACK
23  DNAT   30     > R:E TRAINING_AUX_RD_INTERVAL L=1
24  DNAT   30     < ACK 01
25  DPLT   30     > W:102 TRAINING_PATTERN_SET: L=1 21
26  DPLT   30     < ACK
27  DPLT   30     > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
28  DPLT   30     < ACK
29  DPLT   30     > R:202 LANE0_1_STATUS: L=2
30  DPLT   30     < ACK 11 11
31  DPLT   30     > W:102 TRAINING_PATTERN_SET: L=1 07
32  DPLT   30     < ACK
33  DPLT   30     > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
34  DPLT   30     < ACK
35  DPLT   30     > R:202 LANE0_1_STATUS: L=3
36  DPLT   30     < ACK 77 77 81
37  DPLT   30     > R:204 LANE_ALIGN_STATUS_UPDATED L=2
38  DPLT   30     < ACK 01 00
```

```
  Start Time: +27:16:26.646149
        Type: Native
   Direction: Request
     Command: Write
     Address: 0x00600 (SINK_SET_POWER)
Length: 1

00600: SINK_SET_POWER
    Bit  Name                           Value Description
   ----- ------------------------------ ----- --------------
    2-0  SET_POWER_STATE                  2   D3, FAUX Power State 3
     3                                    0   Reserved
     4                                    0   Reserved
     5                                    0   Reserved
     6                                    0   Reserved
```

```
Where Src=DP-T30 AND Type=(DP-Native) AND Label MATCHES "^> W"
```

Source: ☑ DP-T30 ☐ DP-R31 ☐ DPPM-R32 ☐ DP-T60 ☐ DP-T61 ☐ DP-R62

Type: ☐ NOT
☐ Unknown ☐ Other DDC ☐ HDCP
☐ EDID ☐ CEC ☐ MHL-DDC
☐ MHL-M ☐ MHL-SC1 ☐ MHL
☐ Error ☑ DP-Native ☐ DP-I2C
☐ DP-EDID ☐ DP-HDCP ☐ DP-LT
☐ DP-DDC/CI ☐ DP-HPD ☐ DP-PREAMBLE
☐ SCDC ☐ DP-SB ☐ DP-MST
☐ DP-HDCP-MSG ☐ I2C-SDA-FE ☐ I2C-SDA-RE
☐ I2C-SCL-FE ☐ I2C-SCL-RE ☐ HDMI-HPD
☐ EARC ☐ EARC-HB

Label: ☑ Text contains: ☐ NOT
^> W
☑ Regular Expression Syntax

Details: ☐ Text contains: ☐ NOT ☐ Regular Expression Syntax

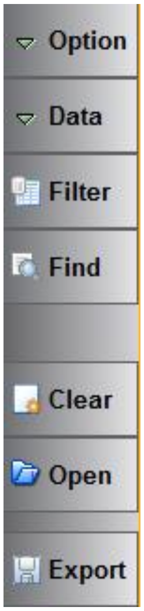
Found Event #1

1: > W:600 SINK_SET_POWER L=1 02

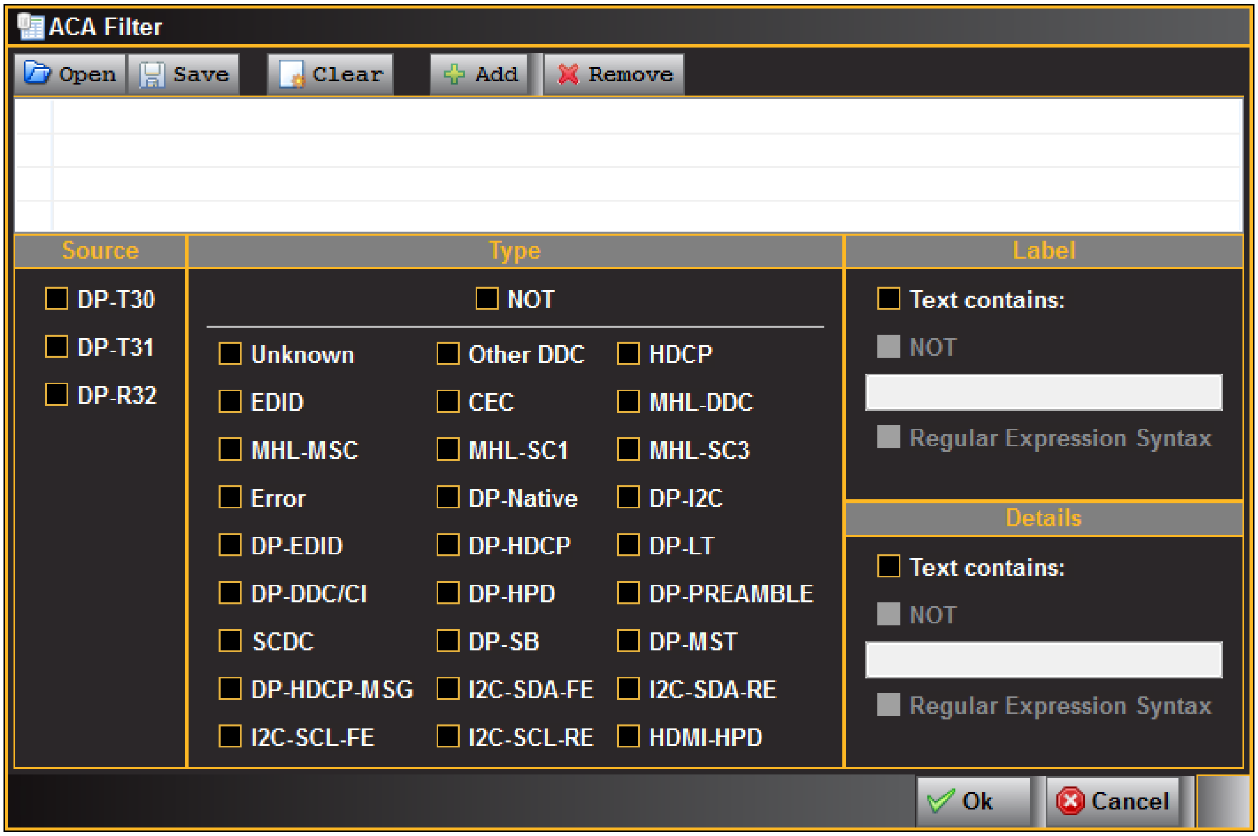
7.9 Using the ACA Filter Feature

The **ACA Filter** dialog box is accessible through the **Data** pop-out menu. The **ACA Filter** function enables you to filter an ACA trace file to view a subset of the log records in a particular file. The ACA Filter feature is not available with the **ACA Remote Control** utility. It is only available with the ACA feature in the embedded GUI (once you have reloaded a stored ACA trace file) and the **ACA Data Viewer**. If you wish to use the Filter feature on ACA traces that you have captured using the **ACA Remote Control** utility you have to save the traces as a file and reload them through the **ACA Data Viewer** utility.

You access the ACA Filter function through the **Data** flyout menu on the control panel of the embedded **ACA utility** and directly from the **Filter** button on the control panel of the **ACA Data Viewer**.



The **ACA Filter** dialog box is shown below.



The **Filter** function enables you to select data types in the **Type** field and then search based on text string occurrences in the log record labels or the message details.

Note: For the **ACA** utility, you have to Stop the collection of real time trace activity using the Start/Stop button on the right side control panel.

The following table describes the **Filter** function buttons, fields and functions.

ACA Filter Window		
Buttons (Top)	**Function**	**Description**
Open Open	Opens a stored user created Filter configuration.	You can store commonly used filter configurations using the Save function and recall them for quick access using the Open button.
Save Save	Saves a user created Filter configuration.	
Clear Clear	Clear the existing Filter criteria.	You can build up complex filter configurations by concatenating multiple filter criteria. When you add multiple configurations they behave as a logical OR function whereby if either of the criteria is True, the filter function will filter an entry. You enter criteria through the embedded touch screen with a pop-up keypad in the ACA real time utility or simply by typing on the external 980 GUI Manager interface. When you are assembling filter configurations you can clear individual configurations by highlighting them in the panel provided and then use the Clear button. You can add through the Add button. You can remove an individual configuration using the Remove button. Example screen shots are shown below.
Add Add	Sets the currently defined Filter criteria defined in either the Source, Type, Label or Details sub-panels and adds another row for a new filter criteria.	
Remove Remove	Removes a highlighted filter criterion of an existing filter configuration.	
Buttons (bottom)	**Function**	
Ok Ok	Initiate the filter and closes the **ACA Filter** window.	
Cancel Cancel	Cancels and closes the filter configuration.	
Fields	**Function**	**Description**
Source	Checkbox to select the port on a particular module that you want to filter. Please note that you can collect data in the ACA Trace window from multiple ports.	When you select multiple Source ports they behave as a logical OR function. When you initiate a search, by clicking on the Next or Previous button, the Filter function will locate a record matching the criteria. If only the Source (port) is specified the next or previous record from or to that source will be highlighted.
Type	Check boxes enabling you to specify which data types you wish to data	When you select multiple data Types they behave as a logical OR function.

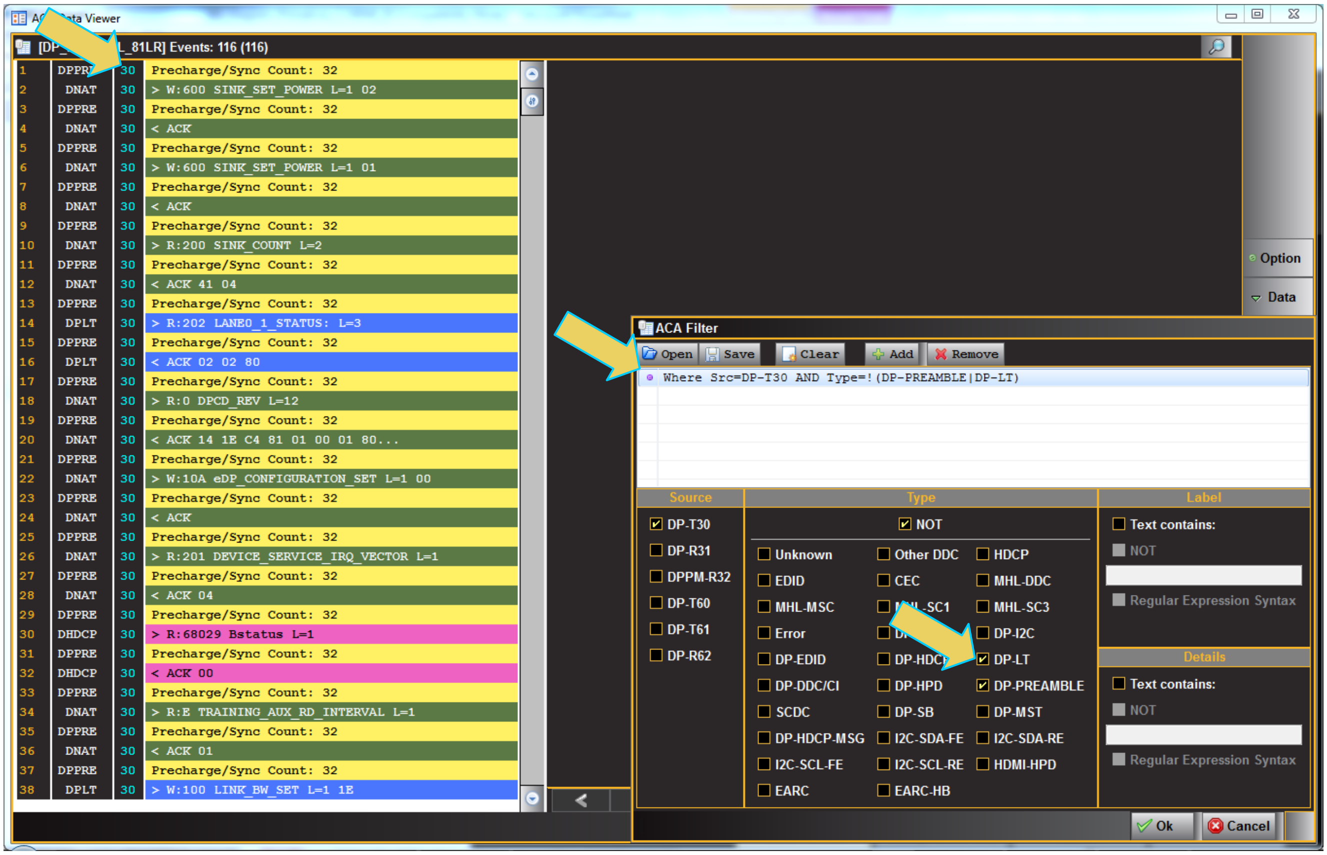
ACA Filter Window		
Buttons (Top)	**Function**	**Description**
	types you wish to filter on based on the string.	If only the Type field is specified the next or previous of that data type will be highlighted.
Label	Combination checkboxes and text fields for specifying criteria for text that appears in the Label field of the message. When you enter a criteria in the Label field, it will automatically be added to the set of criteria in the panel above it.	• Text Contains – A checkbox to activate the Label criteria. • Not – A checkbox which when checked will filter for records that *do not* meet the criteria in the field beneath it. • Text Field – A text field to enter a string that will be matched (or Not matched). • Regular Expression Syntax – A check box to specify whether the text the Text Field will be treated as plain text or a regular expression. Regular expression syntax is a commonly used set of operators for filtering the text. You can find detailed examples on the web including Wikipedia. If Regular Expression checkbox is checked, you can enter in any regular expression into the text field for a string match.
Details	Combination checkboxes and text fields for specifying criteria for text that appears in the Label field of the message. When you enter a criteria in the Label field, it will automatically be added to the set of criteria in the panel above it.	• Text Contains – A checkbox to activate the Label criteria. • Not – A checkbox which when checked will search for records that *do not* meet the criteria in the field beneath it. • Text Field – A text field to enter a string that will be matched (or Not matched). • Regular Expression Syntax – A check box to specify whether the text the Text Field will be treated as plain text or a regular expression. Regular expression syntax is a commonly used set of operators for filtering the text. You can find detailed examples on the web including Wikipedia. If Regular Expression checkbox is checked, you can enter in any regular expression into the text field for a string match.
Close	Closes the Filter window.	

Here are some screen examples of the **Filter** function. Note that the screen examples use the **ACA Data Viewer** utility but the embedded **ACA Data Viewer** works the same way. The only difference is the **ACA** embedded utility uses a pop-up keypad.

Filtering the ACA trace files with the Filter function:

Here are some screen examples of the **Filter** function. Note that the screen examples use the **ACA Data Viewer** utility but the embedded **ACA Data Viewer** works the same way. The only difference is the **ACA** embedded utility uses a pop-up keypad.

1. To filter out all DP Link Training and Preamble messages.



```
1   DPPR   30  Precharge/Sync Count: 32
2    DNAT  30  > W:600 SINK_SET_POWER L=1 02
3   DPPRE  30  Precharge/Sync Count: 32
4    DNAT  30  < ACK
5   DPPRE  30  Precharge/Sync Count: 32
6    DNAT  30  > W:600 SINK_SET_POWER L=1 01
7   DPPRE  30  Precharge/Sync Count: 32
8    DNAT  30  < ACK
9   DPPRE  30  Precharge/Sync Count: 32
10   DNAT  30  > R:200 SINK_COUNT L=2
11  DPPRE  30  Precharge/Sync Count: 32
12   DNAT  30  < ACK 41 04
13  DPPRE  30  Precharge/Sync Count: 32
14   DPLT  30  > R:202 LANE0_1_STATUS: L=3
15  DPPRE  30  Precharge/Sync Count: 32
16   DPLT  30  < ACK 02 02 80
17  DPPRE  30  Precharge/Sync Count: 32
18   DNAT  30  > R:0 DPCD_REV L=12
19  DPPRE  30  Precharge/Sync Count: 32
20   DNAT  30  < ACK 14 1E C4 81 01 00 01 80...
21  DPPRE  30  Precharge/Sync Count: 32
22   DNAT  30  > W:10A eDP_CONFIGURATION_SET L=1 00
23  DPPRE  30  Precharge/Sync Count: 32
24   DNAT  30  < ACK
25  DPPRE  30  Precharge/Sync Count: 32
26   DNAT  30  > R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
27  DPPRE  30  Precharge/Sync Count: 32
28   DNAT  30  < ACK 04
29  DPPRE  30  Precharge/Sync Count: 32
30  DHDCP  30  > R:68029 Bstatus L=1
31  DPPRE  30  Precharge/Sync Count: 32
32  DHDCP  30  < ACK 00
33  DPPRE  30  Precharge/Sync Count: 32
34   DNAT  30  > R:E TRAINING_AUX_RD_INTERVAL L=1
35  DPPRE  30  Precharge/Sync Count: 32
36   DNAT  30  < ACK 01
37  DPPRE  30  Precharge/Sync Count: 32
38   DPLT  30  > W:100 LINK_BW_SET L=1 1E
```

```
Where Src=DP-T30 AND Type=!(DP-PREAMBLE|DP-LT)
```

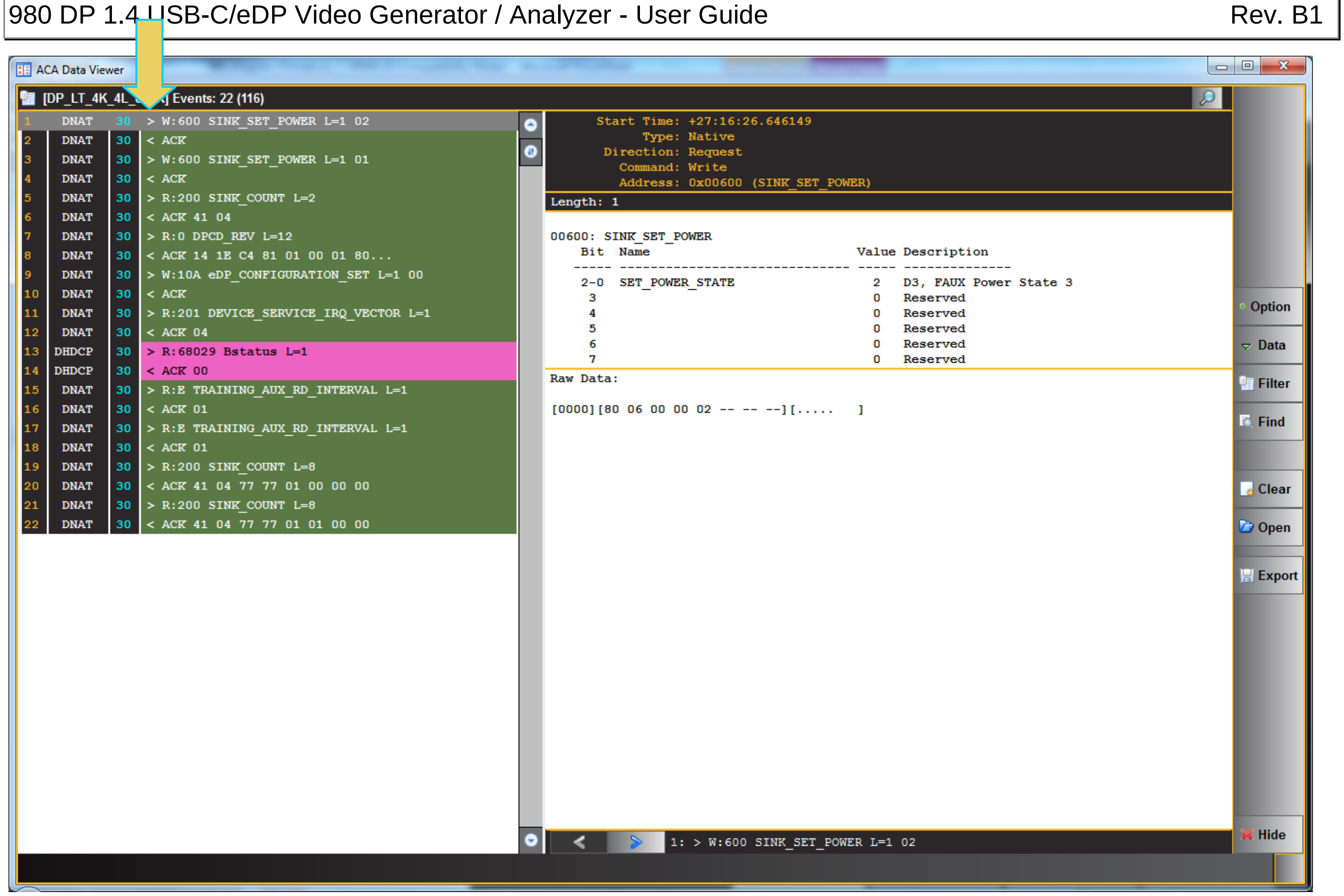
Source
- ☑ DP-T30
- ☐ DP-R31
- ☐ DPPM-R32
- ☐ DP-T60
- ☐ DP-T61
- ☐ DP-R62

Type
- ☑ NOT
- ☐ Unknown
- ☐ EDID
- ☐ MHL-MSC
- ☐ Error
- ☐ DP-EDID
- ☐ DP-DDC/CI
- ☐ SCDC
- ☐ DP-HDCP-MSG
- ☐ I2C-SCL-FE
- ☐ EARC
- ☐ Other DDC
- ☐ CEC
- ☐ L-SC1
- ☐ D
- ☐ DP-HDC
- ☐ DP-HPD
- ☐ DP-SB
- ☐ I2C-SDA-FE
- ☐ I2C-SCL-RE
- ☐ EARC-HB
- ☐ HDCP
- ☐ MHL-DDC
- ☐ MHL-SC3
- ☐ DP-I2C
- ☑ DP-LT
- ☑ DP-PREAMBLE
- ☐ DP-MST
- ☐ I2C-SDA-RE
- ☐ HDMI-HPD

Label
- ☐ Text contains:
- ☐ NOT
- ☐ Regular Expression Syntax

Details
- ☐ Text contains:
- ☐ NOT
- ☐ Regular Expression Syntax

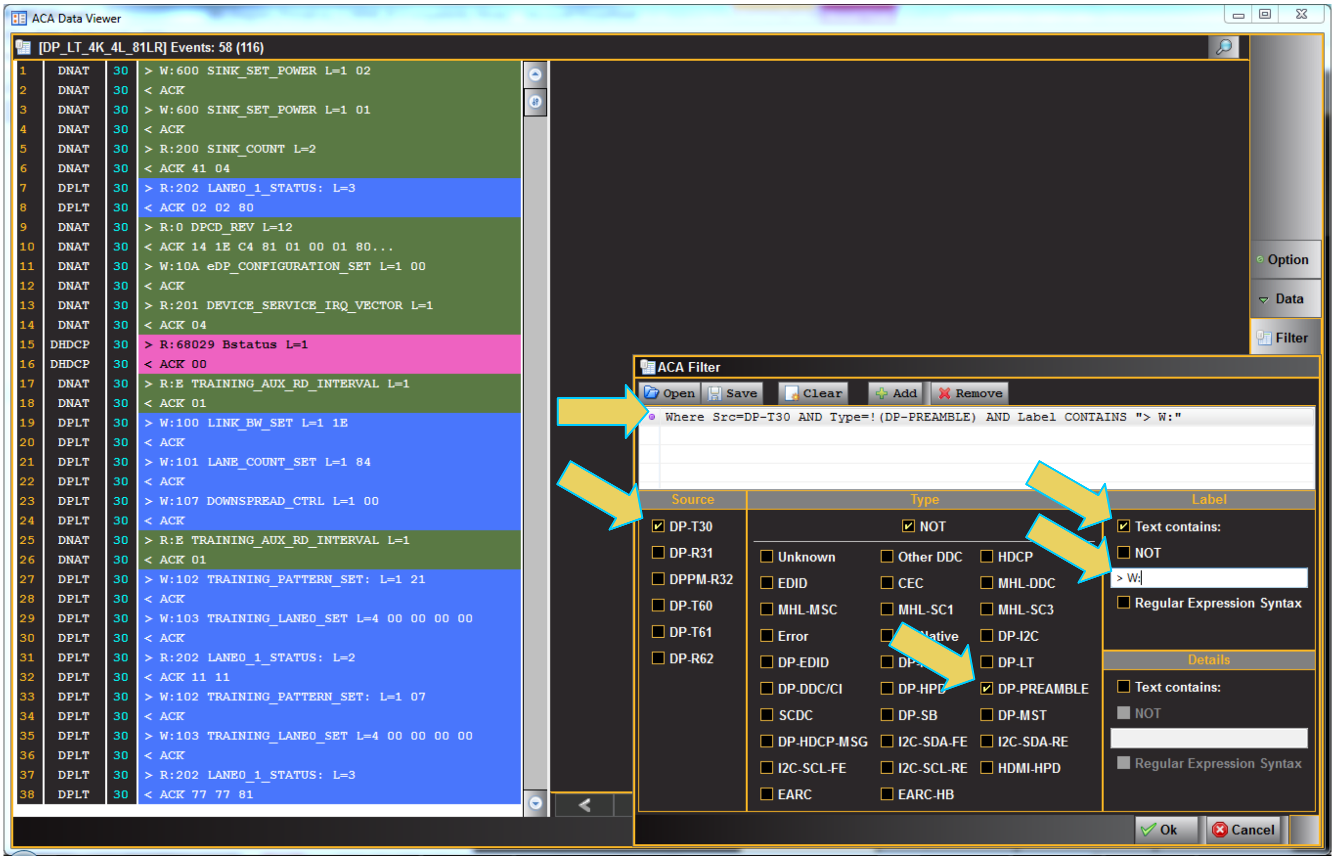
Click on the **Ok** button to initiate the filter. The result is shown below.



```
[DP_LT_4K_4L_   ] Events: 22 (116)
1   DNAT   30  > W:600 SINK_SET_POWER L=1 02
2   DNAT   30  < ACK
3   DNAT   30  > W:600 SINK_SET_POWER L=1 01
4   DNAT   30  < ACK
5   DNAT   30  > R:200 SINK_COUNT L=2
6   DNAT   30  < ACK 41 04
7   DNAT   30  > R:0 DPCD_REV L=12
8   DNAT   30  < ACK 14 1E C4 81 01 00 01 80...
9   DNAT   30  > W:10A eDP_CONFIGURATION_SET L=1 00
10  DNAT   30  < ACK
11  DNAT   30  > R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
12  DNAT   30  < ACK 04
13  DHDCP  30  > R:68029 Bstatus L=1
14  DHDCP  30  < ACK 00
15  DNAT   30  > R:E TRAINING_AUX_RD_INTERVAL L=1
16  DNAT   30  < ACK 01
17  DNAT   30  > R:E TRAINING_AUX_RD_INTERVAL L=1
18  DNAT   30  < ACK 01
19  DNAT   30  > R:200 SINK_COUNT L=8
20  DNAT   30  < ACK 41 04 77 77 01 00 00 00
21  DNAT   30  > R:200 SINK_COUNT L=8
22  DNAT   30  < ACK 41 04 77 77 01 01 00 00
```

```
     Start Time: +27:16:26.646149
           Type: Native
      Direction: Request
        Command: Write
        Address: 0x00600 (SINK_SET_POWER)
Length: 1

00600: SINK_SET_POWER
    Bit  Name                              Value Description
   ----- --------------------------------  ----- --------------
    2-0  SET_POWER_STATE                     2   D3, FAUX Power State 3
     3                                       0   Reserved
     4                                       0   Reserved
     5                                       0   Reserved
     6                                       0   Reserved
     7                                       0   Reserved
Raw Data:

[0000][80 06 00 00 02 -- -- --][.....   ]

1: > W:600 SINK_SET_POWER L=1 02
```

2. To filter using both a port selection and multiple DisplayPort Type selections as a logical AND function including text strings use the following configuration.



ACA Data Viewer

[DP_LT_4K_4L_81LR] Events: 58 (116)

```
1   DNAT   30  > W:600 SINK_SET_POWER L=1 02
2   DNAT   30  < ACK
3   DNAT   30  > W:600 SINK_SET_POWER L=1 01
4   DNAT   30  < ACK
5   DNAT   30  > R:200 SINK_COUNT L=2
6   DNAT   30  < ACK 41 04
7   DPLT   30  > R:202 LANE0_1_STATUS: L=3
8   DPLT   30  < ACK 02 02 80
9   DNAT   30  > R:0 DPCD_REV L=12
10  DNAT   30  < ACK 14 1E C4 81 01 00 01 80...
11  DNAT   30  > W:10A eDP_CONFIGURATION_SET L=1 00
12  DNAT   30  < ACK
13  DNAT   30  > R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
14  DNAT   30  < ACK 04
15  DHDCP  30  > R:68029 Bstatus L=1
16  DHDCP  30  < ACK 00
17  DNAT   30  > R:E TRAINING_AUX_RD_INTERVAL L=1
18  DNAT   30  < ACK 01
19  DPLT   30  > W:100 LINK_BW_SET L=1 1E
20  DPLT   30  < ACK
21  DPLT   30  > W:101 LANE_COUNT_SET L=1 84
22  DPLT   30  < ACK
23  DPLT   30  > W:107 DOWNSPREAD_CTRL L=1 00
24  DPLT   30  < ACK
25  DNAT   30  > R:E TRAINING_AUX_RD_INTERVAL L=1
26  DNAT   30  < ACK 01
27  DPLT   30  > W:102 TRAINING_PATTERN_SET: L=1 21
28  DPLT   30  < ACK
29  DPLT   30  > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
30  DPLT   30  < ACK
31  DPLT   30  > R:202 LANE0_1_STATUS: L=2
32  DPLT   30  < ACK 11 11
33  DPLT   30  > W:102 TRAINING_PATTERN_SET: L=1 07
34  DPLT   30  < ACK
35  DPLT   30  > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
36  DPLT   30  < ACK
37  DPLT   30  > R:202 LANE0_1_STATUS: L=3
38  DPLT   30  < ACK 77 77 81
```

ACA Filter

```
Where Src=DP-T30 AND Type=!(DP-PREAMBLE) AND Label CONTAINS "> W:"
```

Source: ☑ DP-T30 ☐ DP-R31 ☐ DPPM-R32 ☐ DP-T60 ☐ DP-T61 ☐ DP-R62

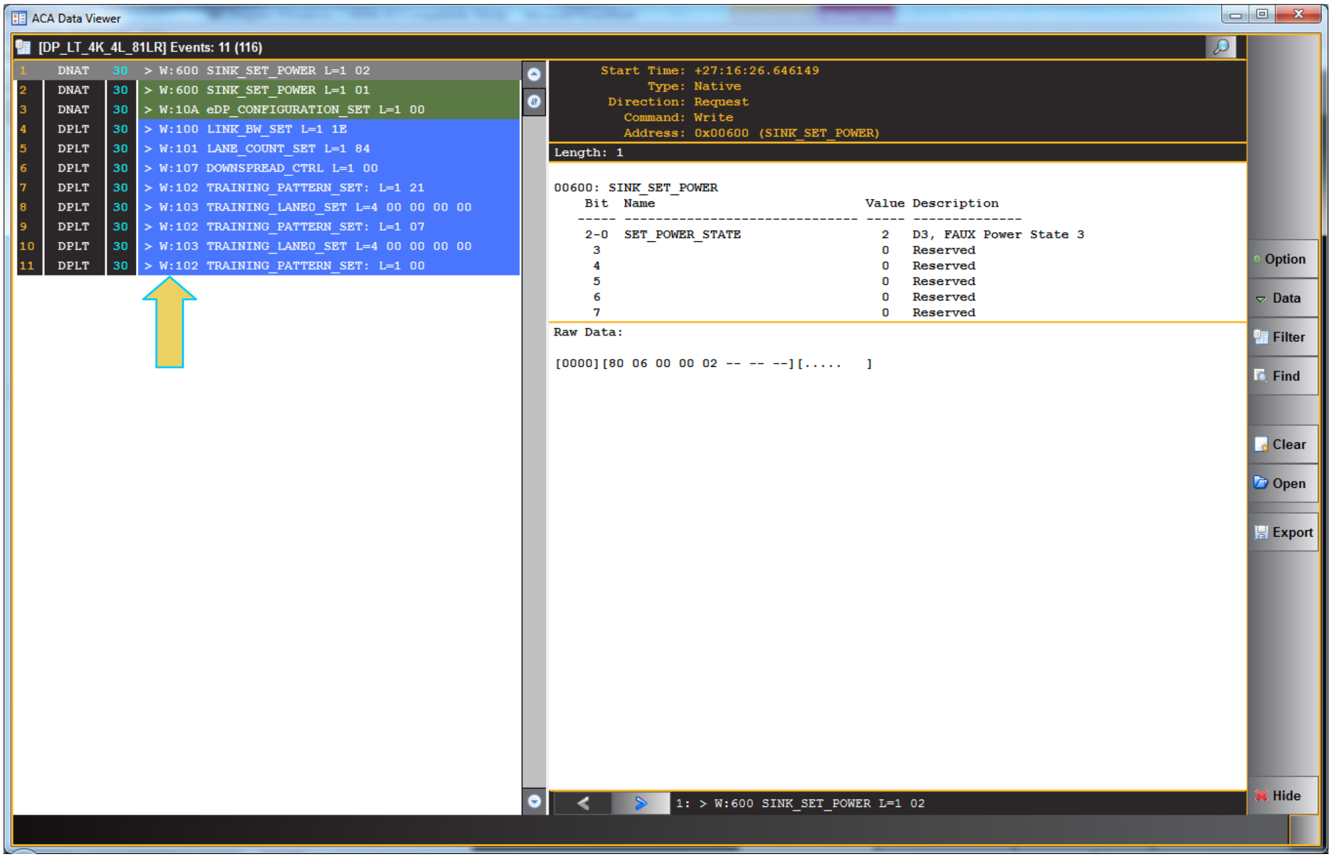
Type: ☑ NOT

☐ Unknown ☐ Other DDC ☐ HDCP
☐ EDID ☐ CEC ☐ MHL-DDC
☐ MHL-MSC ☐ MHL-SC1 ☐ MHL-SC3
☐ Error ☐ Native ☐ DP-I2C
☐ DP-EDID ☐ DP- ☐ DP-LT
☐ DP-DDC/CI ☐ DP-HPD ☑ DP-PREAMBLE
☐ SCDC ☐ DP-SB ☐ DP-MST
☐ DP-HDCP-MSG ☐ I2C-SDA-FE ☐ I2C-SDA-RE
☐ I2C-SCL-FE ☐ I2C-SCL-RE ☐ HDMI-HPD
☐ EARC ☐ EARC-HB

Label: ☑ Text contains: ☐ NOT
> W:
☐ Regular Expression Syntax

Details: ☐ Text contains: ☐ NOT ☐ Regular Expression Syntax

The result of this filtering configuration is shown below.



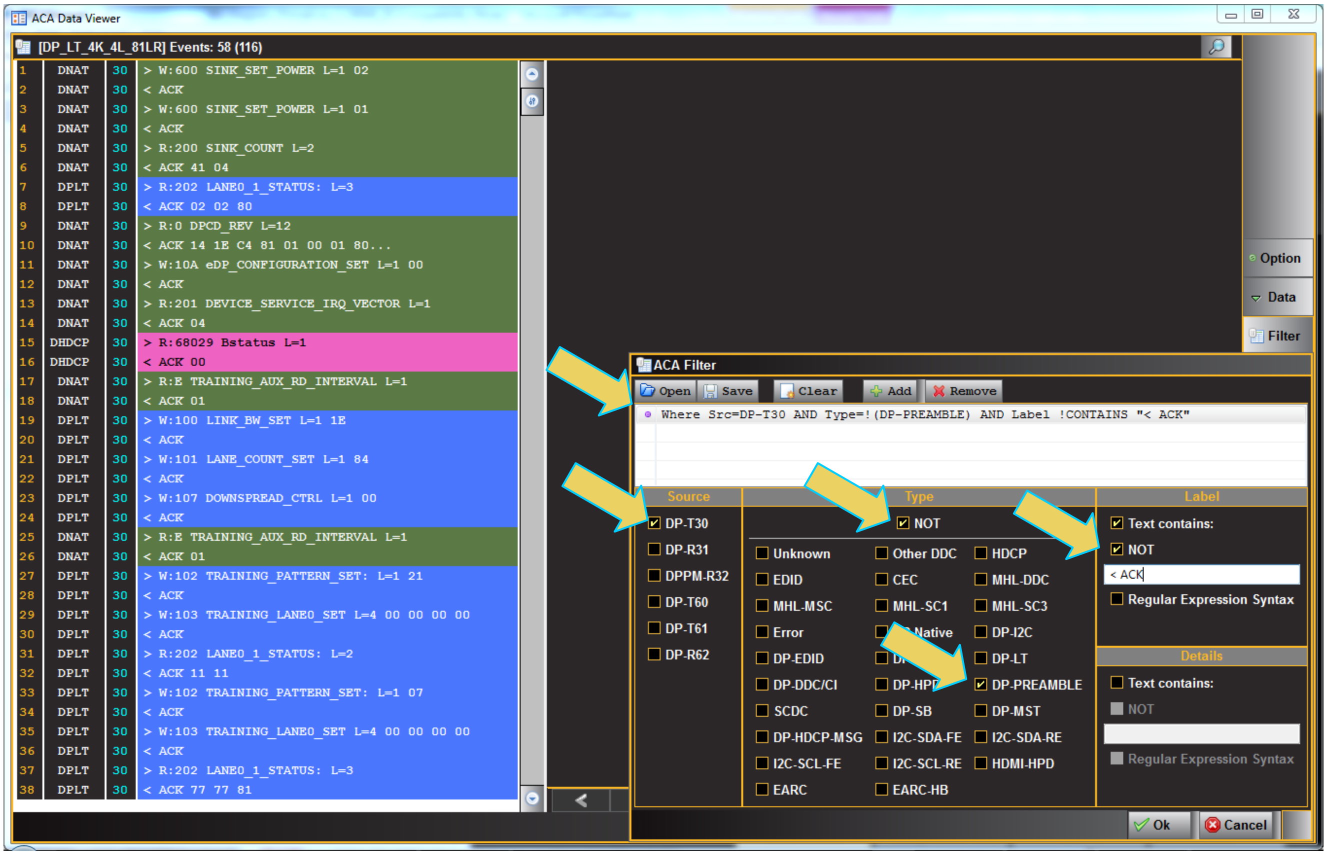
[DP_LT_4K_4L_81LR] Events: 11 (116)

```
1   DNAT  30  > W:600 SINK_SET_POWER L=1 02
2   DNAT  30  > W:600 SINK_SET_POWER L=1 01
3   DNAT  30  > W:10A eDP_CONFIGURATION_SET L=1 00
4   DPLT  30  > W:100 LINK_BW_SET L=1 1E
5   DPLT  30  > W:101 LANE_COUNT_SET L=1 84
6   DPLT  30  > W:107 DOWNSPREAD_CTRL L=1 00
7   DPLT  30  > W:102 TRAINING_PATTERN_SET: L=1 21
8   DPLT  30  > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
9   DPLT  30  > W:102 TRAINING_PATTERN_SET: L=1 07
10  DPLT  30  > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
11  DPLT  30  > W:102 TRAINING_PATTERN_SET: L=1 00
```

```
 Start Time: +27:16:26.646149
       Type: Native
  Direction: Request
    Command: Write
    Address: 0x00600 (SINK_SET_POWER)
Length: 1

00600: SINK_SET_POWER
    Bit  Name                            Value Description
   ----- ------------------------------ ----- --------------
    2-0  SET_POWER_STATE                  2    D3, FAUX Power State 3
     3                                    0    Reserved
     4                                    0    Reserved
     5                                    0    Reserved
     6                                    0    Reserved
     7                                    0    Reserved
Raw Data:

[0000][80 06 00 00 02 -- -- --][.....    ]
```

```
1: > W:600 SINK_SET_POWER L=1 02
```

3. To filter using text strings with a logical NOT function in the message **Label**, use the NOT checkbox on the Label section of the **ACA Filter** window. The following example uses the same filter as the previous example but with a logical NOT function.



[DP_LT_4K_4L_81LR] Events: 58 (116)

```
1   DNAT   30  > W:600 SINK_SET_POWER L=1 02
2   DNAT   30  < ACK
3   DNAT   30  > W:600 SINK_SET_POWER L=1 01
4   DNAT   30  < ACK
5   DNAT   30  > R:200 SINK_COUNT L=2
6   DNAT   30  < ACK 41 04
7   DPLT   30  > R:202 LANE0_1_STATUS: L=3
8   DPLT   30  < ACK 02 02 80
9   DNAT   30  > R:0 DPCD_REV L=12
10  DNAT   30  < ACK 14 1E C4 81 01 00 01 80...
11  DNAT   30  > W:10A eDP_CONFIGURATION_SET L=1 00
12  DNAT   30  < ACK
13  DNAT   30  > R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
14  DNAT   30  < ACK 04
15  DHDCP  30  > R:68029 Bstatus L=1
16  DHDCP  30  < ACK 00
17  DNAT   30  > R:E TRAINING_AUX_RD_INTERVAL L=1
18  DNAT   30  < ACK 01
19  DPLT   30  > W:100 LINK_BW_SET L=1 1E
20  DPLT   30  < ACK
21  DPLT   30  > W:101 LANE_COUNT_SET L=1 84
22  DPLT   30  < ACK
23  DPLT   30  > W:107 DOWNSPREAD_CTRL L=1 00
24  DPLT   30  < ACK
25  DNAT   30  > R:E TRAINING_AUX_RD_INTERVAL L=1
26  DNAT   30  < ACK 01
27  DPLT   30  > W:102 TRAINING_PATTERN_SET: L=1 21
28  DPLT   30  < ACK
29  DPLT   30  > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
30  DPLT   30  < ACK
31  DPLT   30  > R:202 LANE0_1_STATUS: L=2
32  DPLT   30  < ACK 11 11
33  DPLT   30  > W:102 TRAINING_PATTERN_SET: L=1 07
34  DPLT   30  < ACK
35  DPLT   30  > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
36  DPLT   30  < ACK
37  DPLT   30  > R:202 LANE0_1_STATUS: L=3
38  DPLT   30  < ACK 77 77 81
```

ACA Filter

```
Where Src=DP-T30 AND Type=!(DP-PREAMBLE) AND Label !CONTAINS "< ACK"
```

Source

- ☑ DP-T30
- ☐ DP-R31
- ☐ DPPM-R32
- ☐ DP-T60
- ☐ DP-T61
- ☐ DP-R62

Type

☑ NOT

- ☐ Unknown
- ☐ EDID
- ☐ MHL-MSC
- ☐ Error
- ☐ DP-EDID
- ☐ DP-DDC/CI
- ☐ SCDC
- ☐ DP-HDCP-MSG
- ☐ I2C-SCL-FE
- ☐ EARC
- ☐ Other DDC
- ☐ CEC
- ☐ MHL-SC1
- ☐ Native
- ☐ D
- ☐ DP-HPD
- ☐ DP-SB
- ☐ I2C-SDA-FE
- ☐ I2C-SCL-RE
- ☐ EARC-HB
- ☐ HDCP
- ☐ MHL-DDC
- ☐ MHL-SC3
- ☐ DP-I2C
- ☐ DP-LT
- ☑ DP-PREAMBLE
- ☐ DP-MST
- ☐ I2C-SDA-RE
- ☐ HDMI-HPD

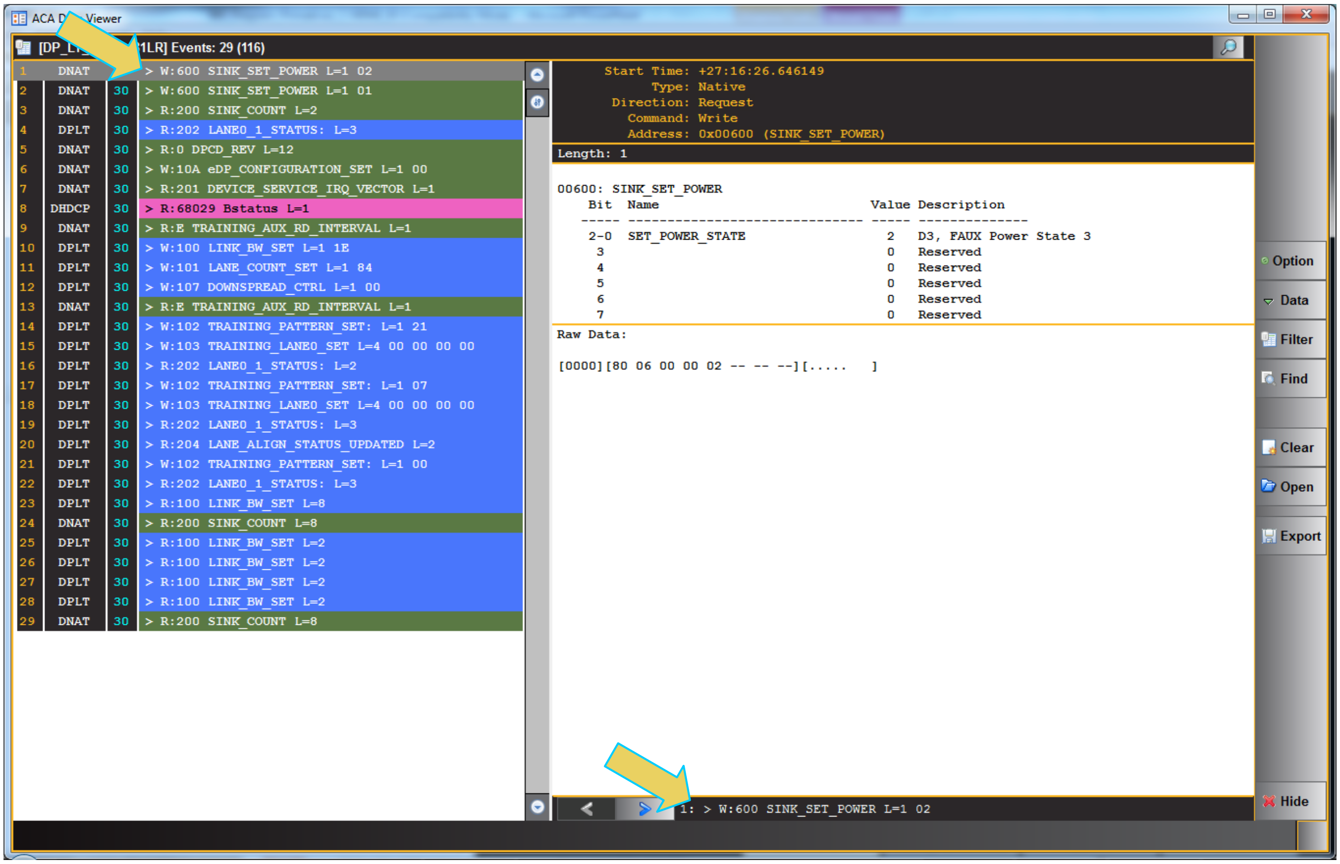
Label

- ☑ Text contains:
- ☑ NOT
- < ACK
- ☐ Regular Expression Syntax

Details

- ☐ Text contains:
- ☐ NOT
- ☐ Regular Expression Syntax

The result of the above filter criteria would be the following.

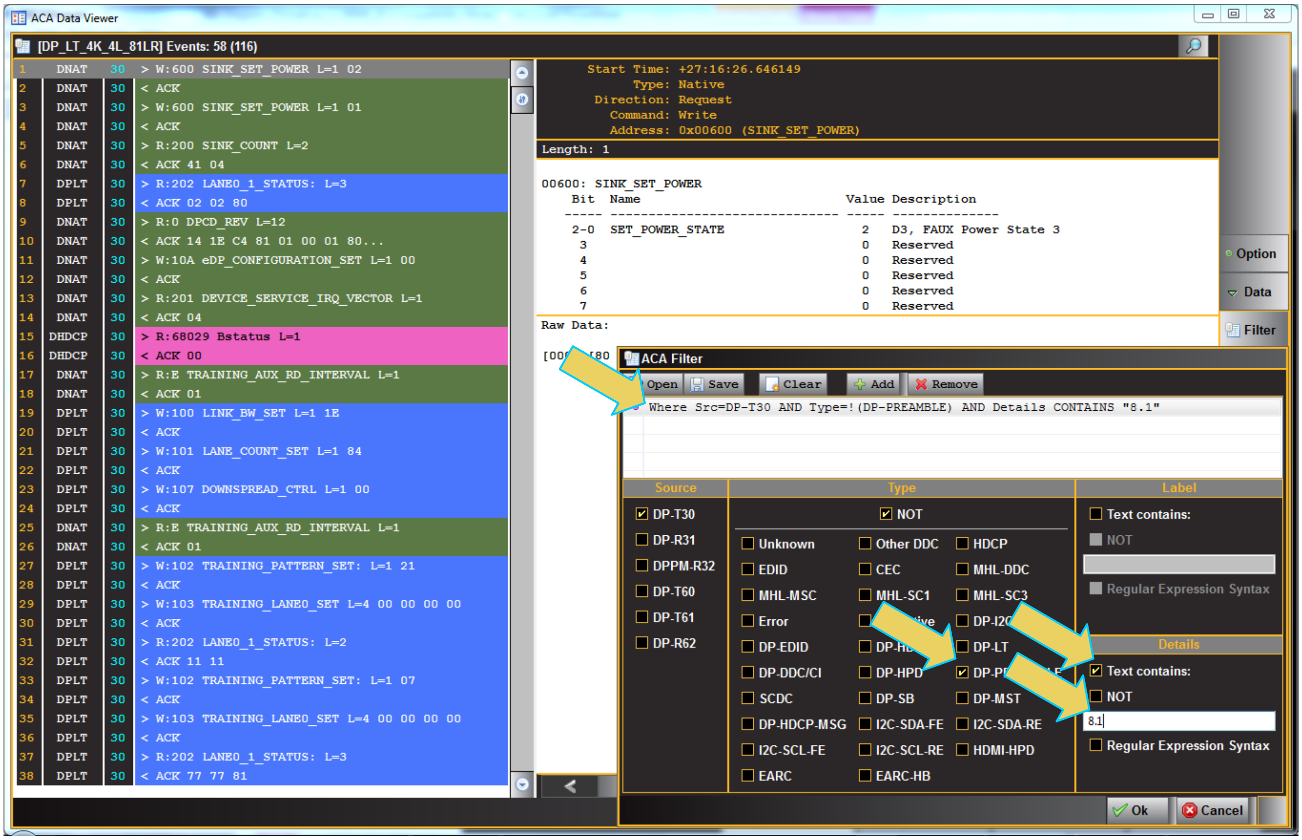


```
1   DNAT       > W:600 SINK_SET_POWER L=1 02
2   DNAT   30  > W:600 SINK_SET_POWER L=1 01
3   DNAT   30  > R:200 SINK_COUNT L=2
4   DPLT   30  > R:202 LANE0_1_STATUS: L=3
5   DNAT   30  > R:0 DPCD_REV L=12
6   DNAT   30  > W:10A eDP_CONFIGURATION_SET L=1 00
7   DNAT   30  > R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
8   DHDCP  30  > R:68029 Bstatus L=1
9   DNAT   30  > R:E TRAINING_AUX_RD_INTERVAL L=1
10  DPLT   30  > W:100 LINK_BW_SET L=1 1E
11  DPLT   30  > W:101 LANE_COUNT_SET L=1 84
12  DPLT   30  > W:107 DOWNSPREAD_CTRL L=1 00
13  DNAT   30  > R:E TRAINING_AUX_RD_INTERVAL L=1
14  DPLT   30  > W:102 TRAINING_PATTERN_SET: L=1 21
15  DPLT   30  > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
16  DPLT   30  > R:202 LANE0_1_STATUS: L=2
17  DPLT   30  > W:102 TRAINING_PATTERN_SET: L=1 07
18  DPLT   30  > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
19  DPLT   30  > R:202 LANE0_1_STATUS: L=3
20  DPLT   30  > R:204 LANE_ALIGN_STATUS_UPDATED L=2
21  DPLT   30  > W:102 TRAINING_PATTERN_SET: L=1 00
22  DPLT   30  > R:202 LANE0_1_STATUS: L=3
23  DPLT   30  > R:100 LINK_BW_SET L=8
24  DNAT   30  > R:200 SINK_COUNT L=8
25  DPLT   30  > R:100 LINK_BW_SET L=2
26  DPLT   30  > R:100 LINK_BW_SET L=2
27  DPLT   30  > R:100 LINK_BW_SET L=2
28  DPLT   30  > R:100 LINK_BW_SET L=2
29  DNAT   30  > R:200 SINK_COUNT L=8
```

```
      Start Time: +27:16:26.646149
            Type: Native
       Direction: Request
         Command: Write
         Address: 0x00600 (SINK_SET_POWER)
Length: 1

00600: SINK_SET_POWER
    Bit  Name                          Value Description
   ----- ----------------------------- ----- -------------
    2-0  SET_POWER_STATE                 2   D3, FAUX Power State 3
     3                                   0   Reserved
     4                                   0   Reserved
     5                                   0   Reserved
     6                                   0   Reserved
     7                                   0   Reserved
Raw Data:

[0000][80 06 00 00 02 -- -- --][.....   ]
```

```
1: > W:600 SINK_SET_POWER L=1 02
```

4. To filter using text strings in the message details, use the checkbox on the **Details** section of the **ACA Filter** window. The following example uses filters using a text string in the **Details** field.



[DP_LT_4K_4L_81LR] Events: 58 (116)

```
1   DNAT   30  > W:600 SINK_SET_POWER L=1 02
2   DNAT   30  < ACK
3   DNAT   30  > W:600 SINK_SET_POWER L=1 01
4   DNAT   30  < ACK
5   DNAT   30  > R:200 SINK_COUNT L=2
6   DNAT   30  < ACK 41 04
7   DPLT   30  > R:202 LANE0_1_STATUS: L=3
8   DPLT   30  < ACK 02 02 80
9   DNAT   30  > R:0 DPCD_REV L=12
10  DNAT   30  < ACK 14 1E C4 81 01 00 01 80...
11  DNAT   30  > W:10A eDP_CONFIGURATION_SET L=1 00
12  DNAT   30  < ACK
13  DNAT   30  > R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
14  DNAT   30  < ACK 04
15  DHDCP  30  > R:68029 Bstatus L=1
16  DHDCP  30  < ACK 00
17  DNAT   30  > R:E TRAINING_AUX_RD_INTERVAL L=1
18  DNAT   30  < ACK 01
19  DPLT   30  > W:100 LINK_BW_SET L=1 1E
20  DPLT   30  < ACK
21  DPLT   30  > W:101 LANE_COUNT_SET L=1 84
22  DPLT   30  < ACK
23  DPLT   30  > W:107 DOWNSPREAD_CTRL L=1 00
24  DPLT   30  < ACK
25  DNAT   30  > R:E TRAINING_AUX_RD_INTERVAL L=1
26  DNAT   30  < ACK 01
27  DPLT   30  > W:102 TRAINING_PATTERN_SET: L=1 21
28  DPLT   30  < ACK
29  DPLT   30  > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
30  DPLT   30  < ACK
31  DPLT   30  > R:202 LANE0_1_STATUS: L=2
32  DPLT   30  < ACK 11 11
33  DPLT   30  > W:102 TRAINING_PATTERN_SET: L=1 07
34  DPLT   30  < ACK
35  DPLT   30  > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
36  DPLT   30  < ACK
37  DPLT   30  > R:202 LANE0_1_STATUS: L=3
38  DPLT   30  < ACK 77 77 81
```

```
  Start Time: +27:16:26.646149
        Type: Native
   Direction: Request
     Command: Write
     Address: 0x00600 (SINK_SET_POWER)
Length: 1

00600: SINK_SET_POWER
    Bit  Name                            Value Description
   ----- ------------------------------- ----- --------------
    2-0  SET_POWER_STATE                   2   D3, FAUX Power State 3
     3                                     0   Reserved
     4                                     0   Reserved
     5                                     0   Reserved
     6                                     0   Reserved
     7                                     0   Reserved
Raw Data:

[00( [80
```

```
Where Src=DP-T30 AND Type=!(DP-PREAMBLE) AND Details CONTAINS "8.1"
```

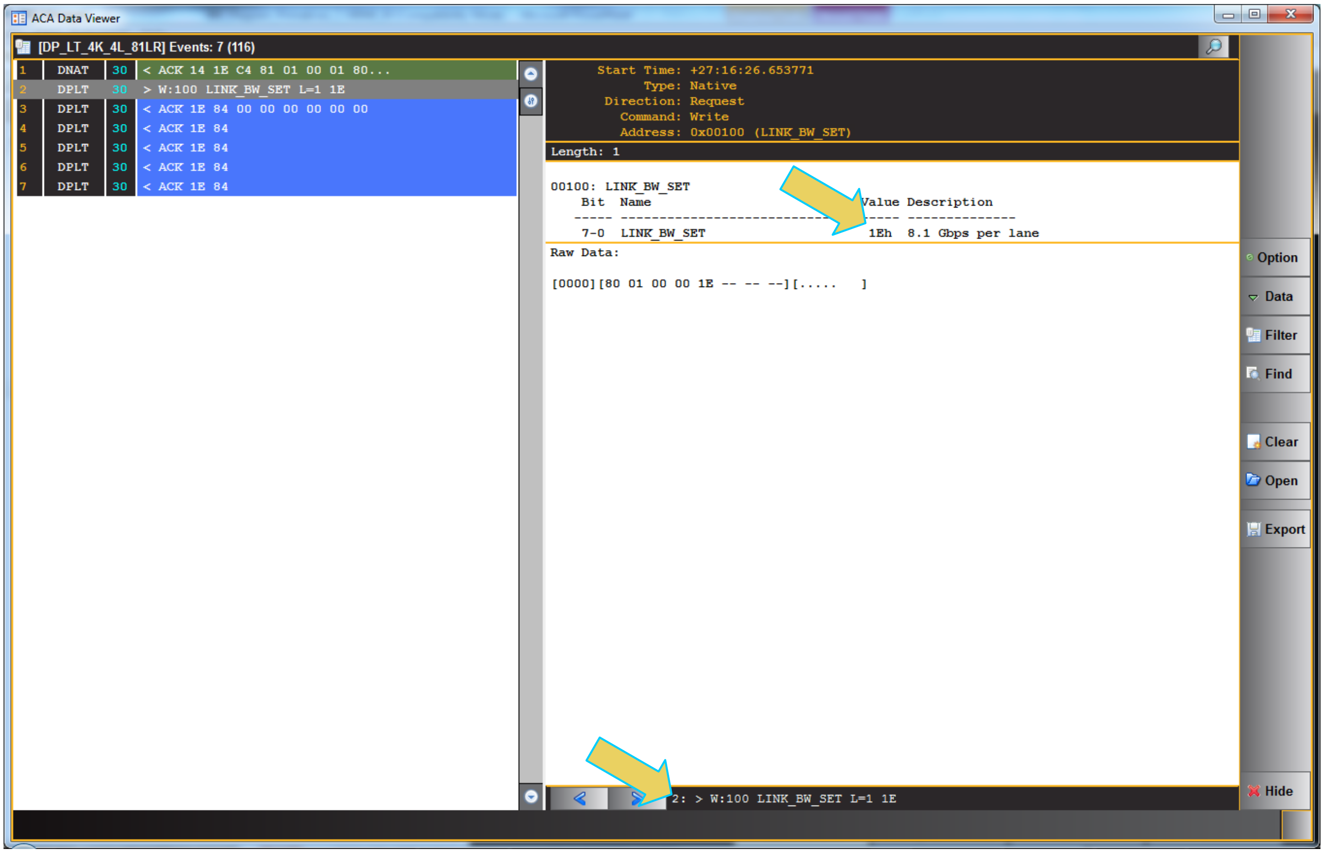
Source:
- ☑ DP-T30
- ☐ DP-R31
- ☐ DPPM-R32
- ☐ DP-T60
- ☐ DP-T61
- ☐ DP-R62

Type:
- ☑ NOT
- ☐ Unknown ☐ Other DDC ☐ HDCP
- ☐ EDID ☐ CEC ☐ MHL-DDC
- ☐ MHL-MSC ☐ MHL-SC1 ☐ MHL-SC3
- ☐ Error ☐ ive ☐ DP-I2C
- ☐ DP-EDID ☐ DP-H ☐ DP-LT
- ☐ DP-DDC/CI ☐ DP-HPD ☑ DP-P E
- ☐ SCDC ☐ DP-SB ☐ DP-MST
- ☐ DP-HDCP-MSG ☐ I2C-SDA-FE ☐ I2C-SDA-RE
- ☐ I2C-SCL-FE ☐ I2C-SCL-RE ☐ HDMI-HPD
- ☐ EARC ☐ EARC-HB

Label:
- ☐ Text contains:
- ☐ NOT
- ☐ Regular Expression Syntax

Details:
- ☑ Text contains:
- ☐ NOT
- 8.1
- ☐ Regular Expression Syntax

The result of the above filter criteria would be the following.



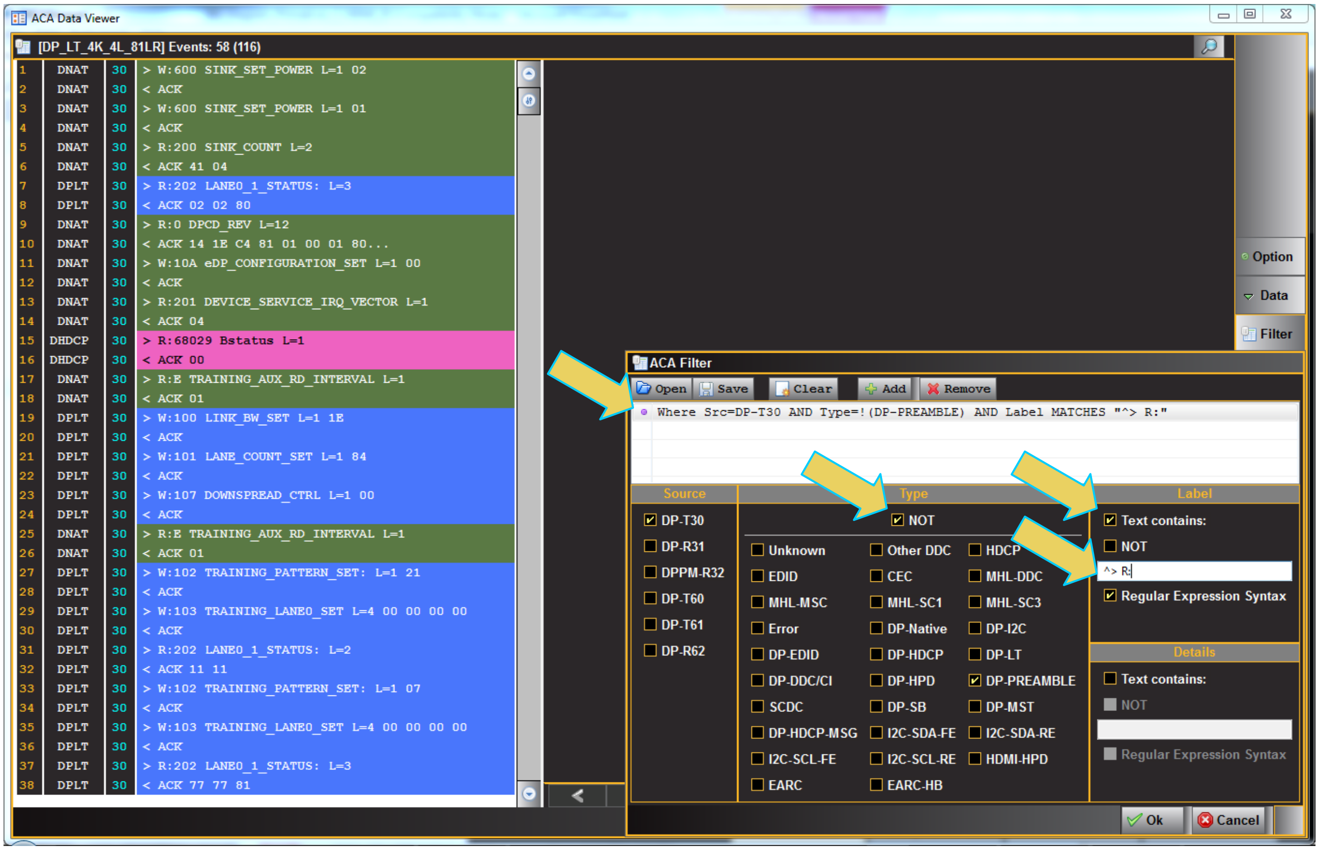
[DP_LT_4K_4L_81LR] Events: 7 (116)

```
1   DNAT   30  < ACK 14 1E C4 81 01 00 01 80...
2   DPLT   30  > W:100 LINK_BW_SET L=1 1E
3   DPLT   30  < ACK 1E 84 00 00 00 00 00 00
4   DPLT   30  < ACK 1E 84
5   DPLT   30  < ACK 1E 84
6   DPLT   30  < ACK 1E 84
7   DPLT   30  < ACK 1E 84
```

```
      Start Time: +27:16:26.653771
            Type: Native
       Direction: Request
         Command: Write
         Address: 0x00100 (LINK_BW_SET)
Length: 1

00100: LINK_BW_SET
    Bit  Name                                Value Description
   -----  -------------------------------- ----- -------------
    7-0  LINK_BW_SET                          1Eh   8.1 Gbps per lane
Raw Data:

[0000][80 01 00 00 1E -- -- --][.....   ]
```

```
2: > W:100 LINK_BW_SET L=1 1E
```

5. To filter using regular expression text in the message label, text strings in the message details, use the **Regular Expression Syntax** checkbox on the **Label** section of the **ACA Filter** window. Refer to the following example. Note that the (^) operator filters for text strings that begin with the text you enter after it, in this case, “> R:”



[DP_LT_4K_4L_81LR] Events: 58 (116)

```
1   DNAT   30  > W:600 SINK_SET_POWER L=1 02
2   DNAT   30  < ACK
3   DNAT   30  > W:600 SINK_SET_POWER L=1 01
4   DNAT   30  < ACK
5   DNAT   30  > R:200 SINK_COUNT L=2
6   DNAT   30  < ACK 41 04
7   DPLT   30  > R:202 LANE0_1_STATUS: L=3
8   DPLT   30  < ACK 02 02 80
9   DNAT   30  > R:0 DPCD_REV L=12
10  DNAT   30  < ACK 14 1E C4 81 01 00 01 80...
11  DNAT   30  > W:10A eDP_CONFIGURATION_SET L=1 00
12  DNAT   30  < ACK
13  DNAT   30  > R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
14  DNAT   30  < ACK 04
15  DHDCP  30  > R:68029 Bstatus L=1
16  DHDCP  30  < ACK 00
17  DNAT   30  > R:E TRAINING_AUX_RD_INTERVAL L=1
18  DNAT   30  < ACK 01
19  DPLT   30  > W:100 LINK_BW_SET L=1 1E
20  DPLT   30  < ACK
21  DPLT   30  > W:101 LANE_COUNT_SET L=1 84
22  DPLT   30  < ACK
23  DPLT   30  > W:107 DOWNSPREAD_CTRL L=1 00
24  DPLT   30  < ACK
25  DNAT   30  > R:E TRAINING_AUX_RD_INTERVAL L=1
26  DNAT   30  < ACK 01
27  DPLT   30  > W:102 TRAINING_PATTERN_SET: L=1 21
28  DPLT   30  < ACK
29  DPLT   30  > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
30  DPLT   30  < ACK
31  DPLT   30  > R:202 LANE0_1_STATUS: L=2
32  DPLT   30  < ACK 11 11
33  DPLT   30  > W:102 TRAINING_PATTERN_SET: L=1 07
34  DPLT   30  < ACK
35  DPLT   30  > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
36  DPLT   30  < ACK
37  DPLT   30  > R:202 LANE0_1_STATUS: L=3
38  DPLT   30  < ACK 77 77 81
```

```
Where Src=DP-T30 AND Type=!(DP-PREAMBLE) AND Label MATCHES "^> R:"
```

Source

☑ DP-T30
☐ DP-R31
☐ DPPM-R32
☐ DP-T60
☐ DP-T61
☐ DP-R62

Type

☑ NOT

☐ Unknown ☐ Other DDC ☐ HDCP
☐ EDID ☐ CEC ☐ MHL-DDC
☐ MHL-MSC ☐ MHL-SC1 ☐ MHL-SC3
☐ Error ☐ DP-Native ☐ DP-I2C
☐ DP-EDID ☐ DP-HDCP ☐ DP-LT
☐ DP-DDC/CI ☐ DP-HPD ☑ DP-PREAMBLE
☐ SCDC ☐ DP-SB ☐ DP-MST
☐ DP-HDCP-MSG ☐ I2C-SDA-FE ☐ I2C-SDA-RE
☐ I2C-SCL-FE ☐ I2C-SCL-RE ☐ HDMI-HPD
☐ EARC ☐ EARC-HB

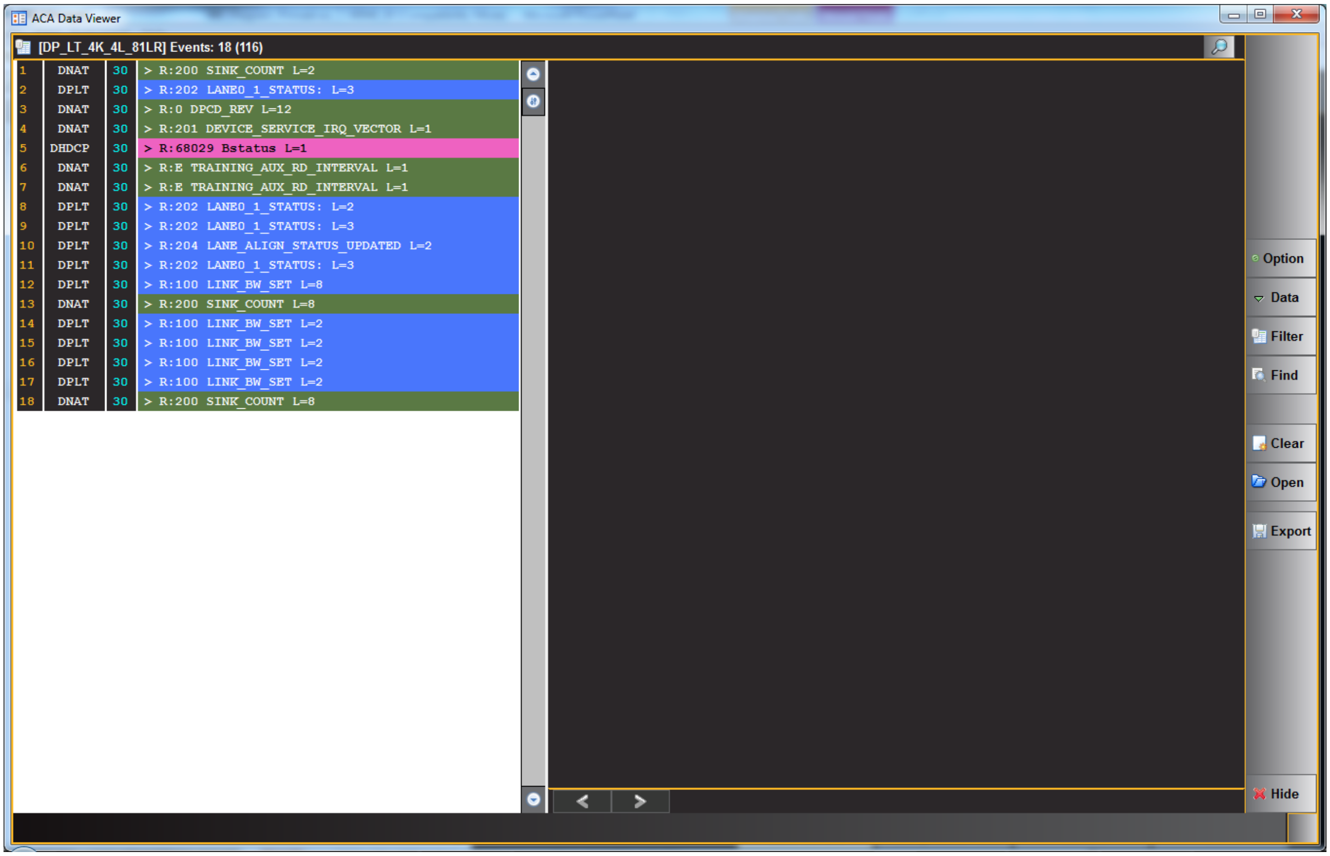
Label

☑ Text contains:
☐ NOT
^> R:
☑ Regular Expression Syntax

Details

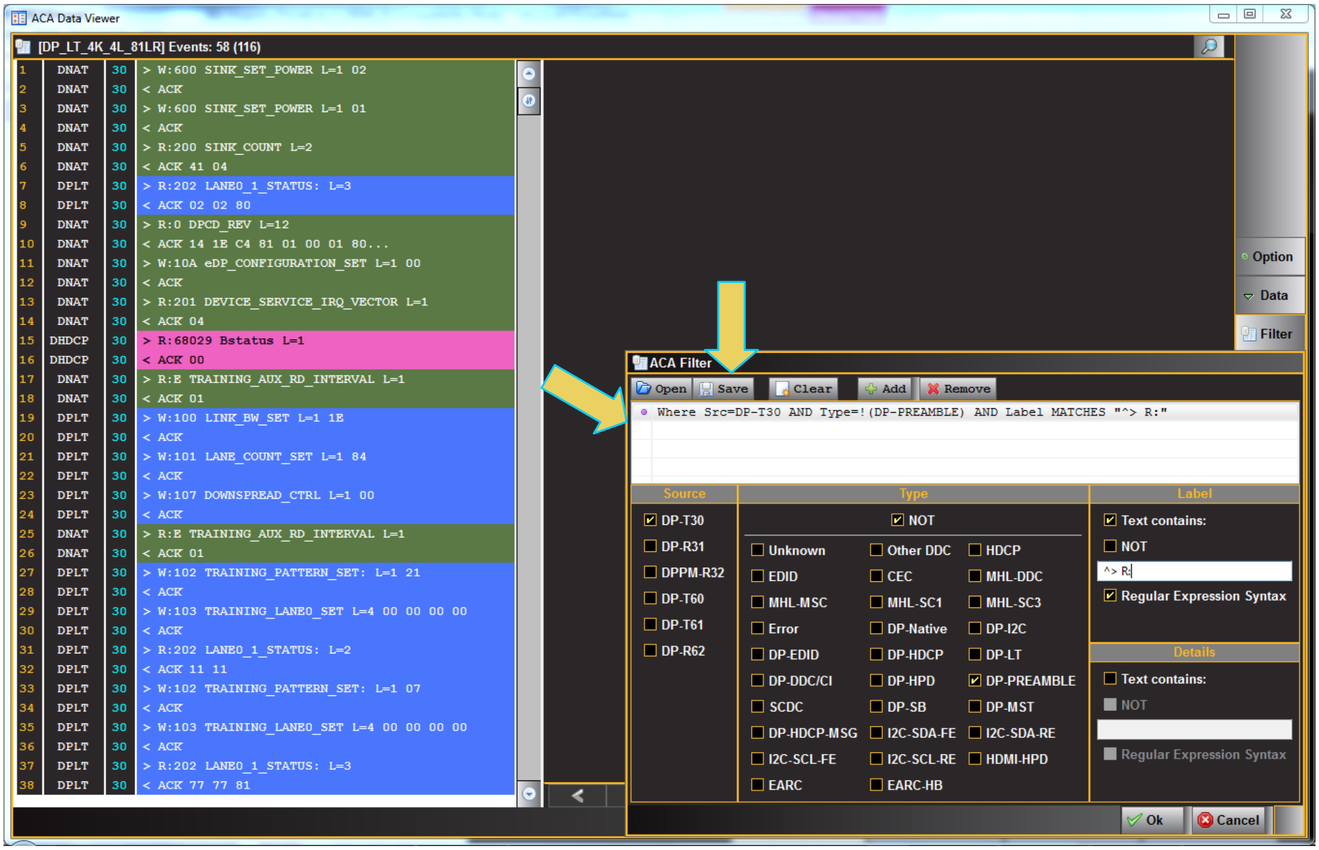
☐ Text contains:
☐ NOT
☐ Regular Expression Syntax

The result of the above filter criteria would be the following.



```
1   DNAT   30  > R:200 SINK_COUNT L=2
2   DPLT   30  > R:202 LANE0_1_STATUS: L=3
3   DNAT   30  > R:0 DPCD_REV L=12
4   DNAT   30  > R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
5   DHDCP  30  > R:68029 Bstatus L=1
6   DNAT   30  > R:E TRAINING_AUX_RD_INTERVAL L=1
7   DNAT   30  > R:E TRAINING_AUX_RD_INTERVAL L=1
8   DPLT   30  > R:202 LANE0_1_STATUS: L=2
9   DPLT   30  > R:202 LANE0_1_STATUS: L=3
10  DPLT   30  > R:204 LANE_ALIGN_STATUS_UPDATED L=2
11  DPLT   30  > R:202 LANE0_1_STATUS: L=3
12  DPLT   30  > R:100 LINK_BW_SET L=8
13  DNAT   30  > R:200 SINK_COUNT L=8
14  DPLT   30  > R:100 LINK_BW_SET L=2
15  DPLT   30  > R:100 LINK_BW_SET L=2
16  DPLT   30  > R:100 LINK_BW_SET L=2
17  DPLT   30  > R:100 LINK_BW_SET L=2
18  DNAT   30  > R:200 SINK_COUNT L=8
```

6. To save a filter configuration for quick recall, use the **Save** button.



[DP_LT_4K_4L_81LR] Events: 58 (116)

```
1   DNAT   30  > W:600 SINK_SET_POWER L=1 02
2   DNAT   30  < ACK
3   DNAT   30  > W:600 SINK_SET_POWER L=1 01
4   DNAT   30  < ACK
5   DNAT   30  > R:200 SINK_COUNT L=2
6   DNAT   30  < ACK 41 04
7   DPLT   30  > R:202 LANE0_1_STATUS: L=3
8   DPLT   30  < ACK 02 02 80
9   DNAT   30  > R:0 DPCD_REV L=12
10  DNAT   30  < ACK 14 1E C4 81 01 00 01 80...
11  DNAT   30  > W:10A eDP_CONFIGURATION_SET L=1 00
12  DNAT   30  < ACK
13  DNAT   30  > R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
14  DNAT   30  < ACK 04
15  DHDCP  30  > R:68029 Bstatus L=1
16  DHDCP  30  < ACK 00
17  DNAT   30  > R:E TRAINING_AUX_RD_INTERVAL L=1
18  DNAT   30  < ACK 01
19  DPLT   30  > W:100 LINK_BW_SET L=1 1E
20  DPLT   30  < ACK
21  DPLT   30  > W:101 LANE_COUNT_SET L=1 84
22  DPLT   30  < ACK
23  DPLT   30  > W:107 DOWNSPREAD_CTRL L=1 00
24  DPLT   30  < ACK
25  DNAT   30  > R:E TRAINING_AUX_RD_INTERVAL L=1
26  DNAT   30  < ACK 01
27  DPLT   30  > W:102 TRAINING_PATTERN_SET: L=1 21
28  DPLT   30  < ACK
29  DPLT   30  > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
30  DPLT   30  < ACK
31  DPLT   30  > R:202 LANE0_1_STATUS: L=2
32  DPLT   30  < ACK 11 11
33  DPLT   30  > W:102 TRAINING_PATTERN_SET: L=1 07
34  DPLT   30  < ACK
35  DPLT   30  > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
36  DPLT   30  < ACK
37  DPLT   30  > R:202 LANE0_1_STATUS: L=3
38  DPLT   30  < ACK 77 77 81
```

```
Where Src=DP-T30 AND Type=!(DP-PREAMBLE) AND Label MATCHES "^> R:"
```

Source: ☑ DP-T30 ☐ DP-R31 ☐ DPPM-R32 ☐ DP-T60 ☐ DP-T61 ☐ DP-R62

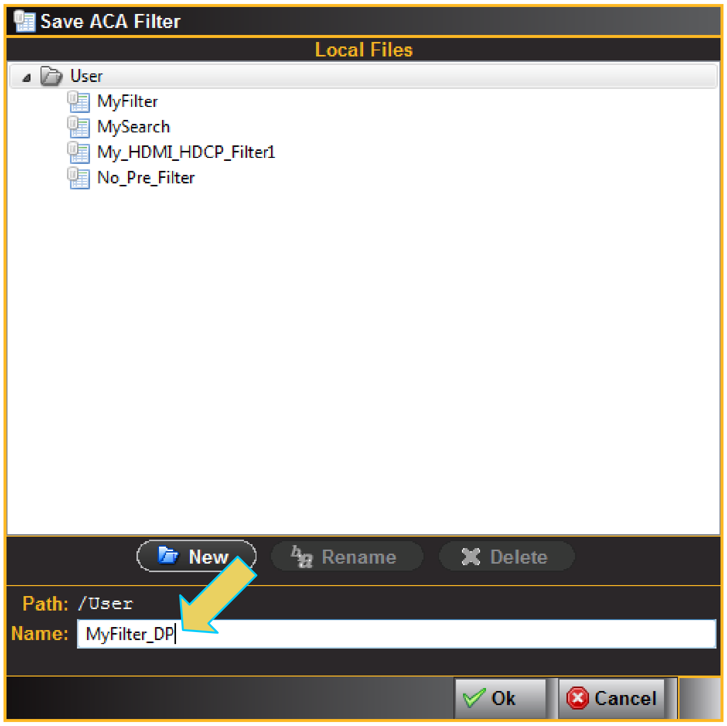
Type: ☑ NOT

☐ Unknown ☐ Other DDC ☐ HDCP
☐ EDID ☐ CEC ☐ MHL-DDC
☐ MHL-MSC ☐ MHL-SC1 ☐ MHL-SC3
☐ Error ☐ DP-Native ☐ DP-I2C
☐ DP-EDID ☐ DP-HDCP ☐ DP-LT
☐ DP-DDC/CI ☐ DP-HPD ☑ DP-PREAMBLE
☐ SCDC ☐ DP-SB ☐ DP-MST
☐ DP-HDCP-MSG ☐ I2C-SDA-FE ☐ I2C-SDA-RE
☐ I2C-SCL-FE ☐ I2C-SCL-RE ☐ HDMI-HPD
☐ EARC ☐ EARC-HB

Label: ☑ Text contains: ☐ NOT ^> R: ☑ Regular Expression Syntax

Details: ☐ Text contains: ☐ NOT ☐ Regular Expression Syntax

A dialog box appears as shown below. Enter a name and click on **Ok**.



Path: /User

Name: MyFilter_DP

8 Embedded DisplayPort (eDP)

The 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module support several eDP features such as fast link training, alternate scrambler seed, Advanced Link Power Management (ALPM) and backlight control through control pins. A pin header is available to provide access to the backlight Tx control test feature. The module offers the hardware necessary to support a variety of optional eDP features.

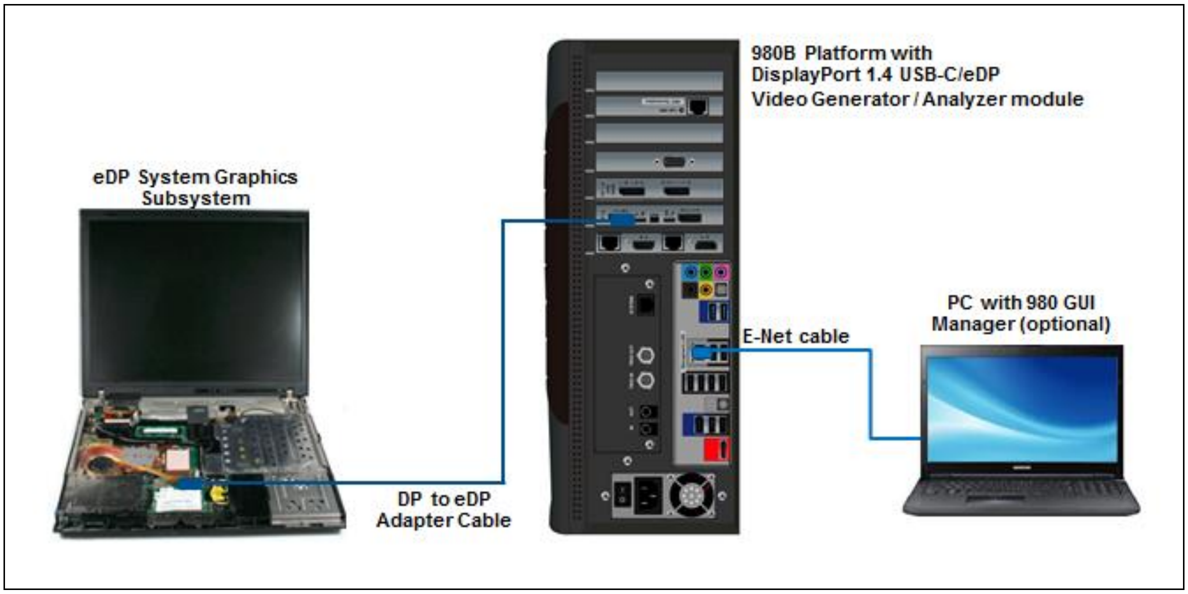
Note: The eDP features are optional and require purchase of a license to activate.

This section provides descriptions and procedural information of the eDP features supported by the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module.

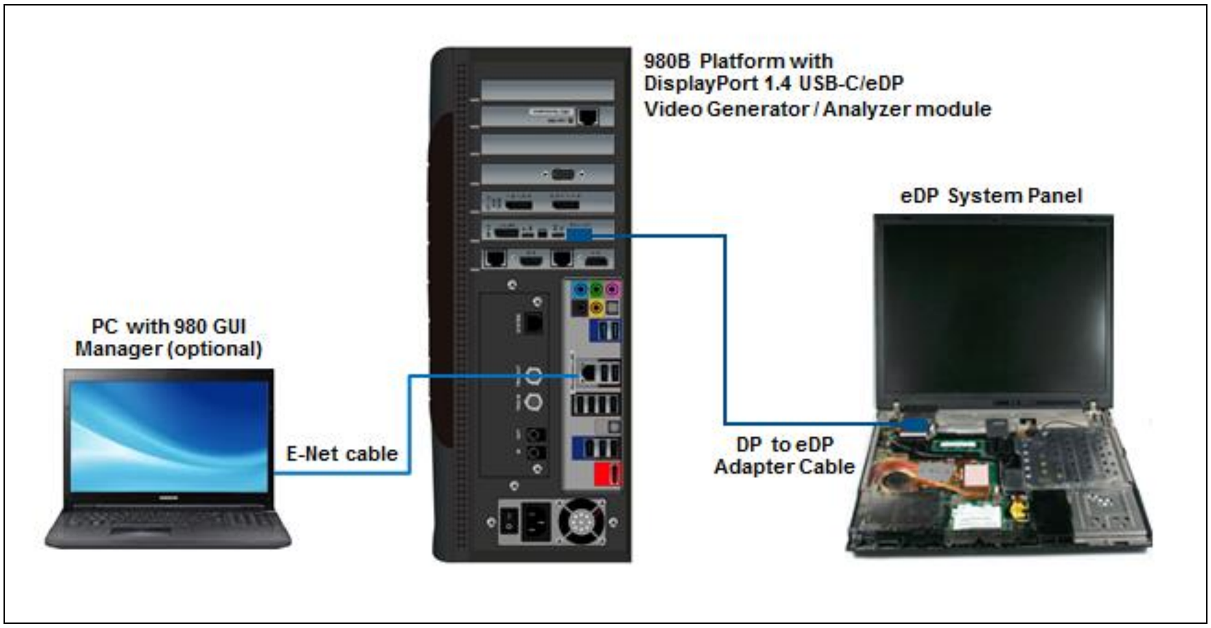
8.1 eDP Testing Connections

This section provides procedures on how to connect your eDP TCON panel or graphics source system to the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module. You will use the Standard DisplayPort connectors for testing eDP (not the USB-C connectors). You will need an eDP to DP adapter cable and or an adapter board to make these connections.

8.1.1 eDP Source Test Connections



8.1.2 eDP Sink Test Connections



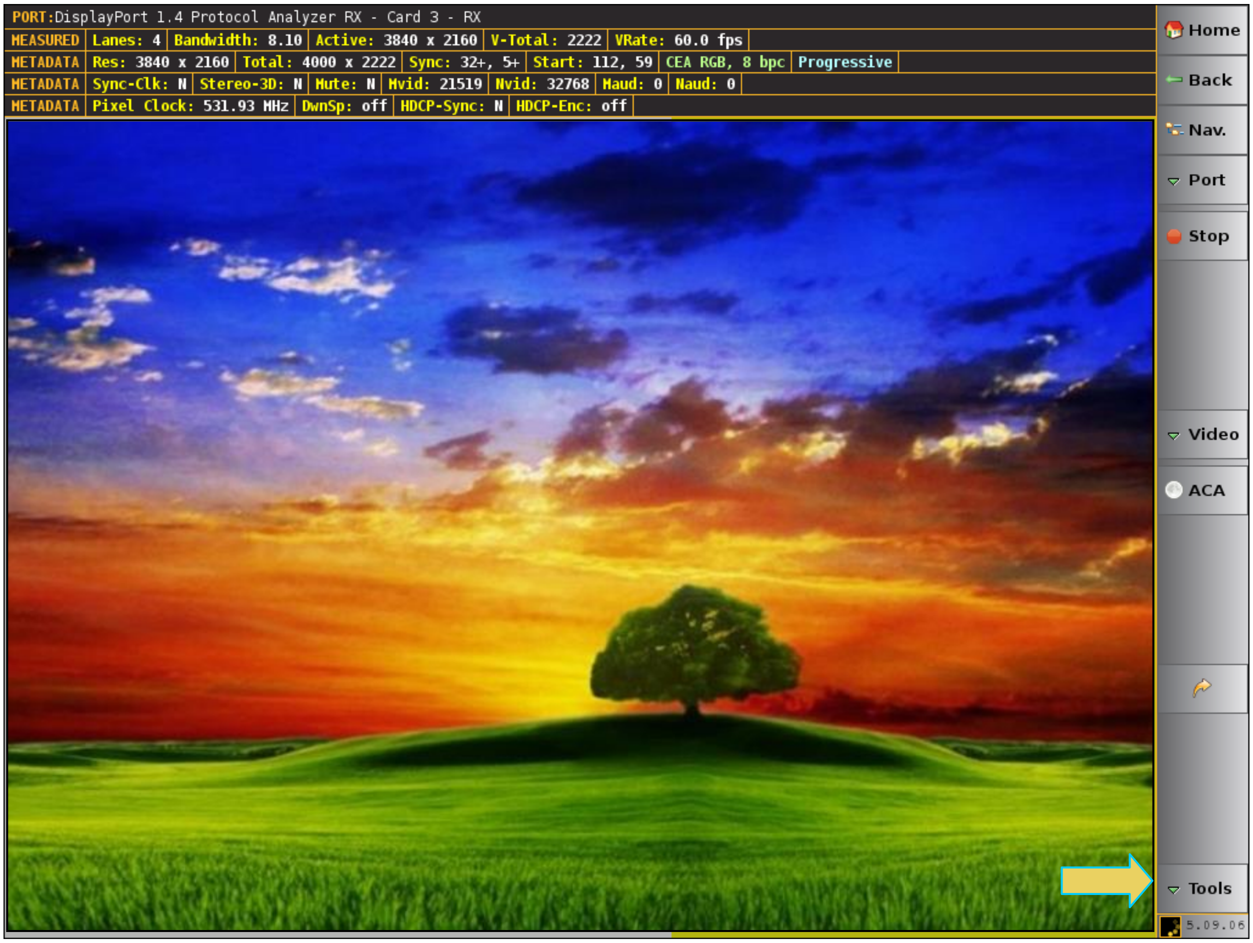
8.2 Fast Link Training

This section provides procedures on eDP fast link training. Once the fast link training has been achieved the Source or Sink test features supported by the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module can be used.

8.2.1 Fast Link Training – Source Tests

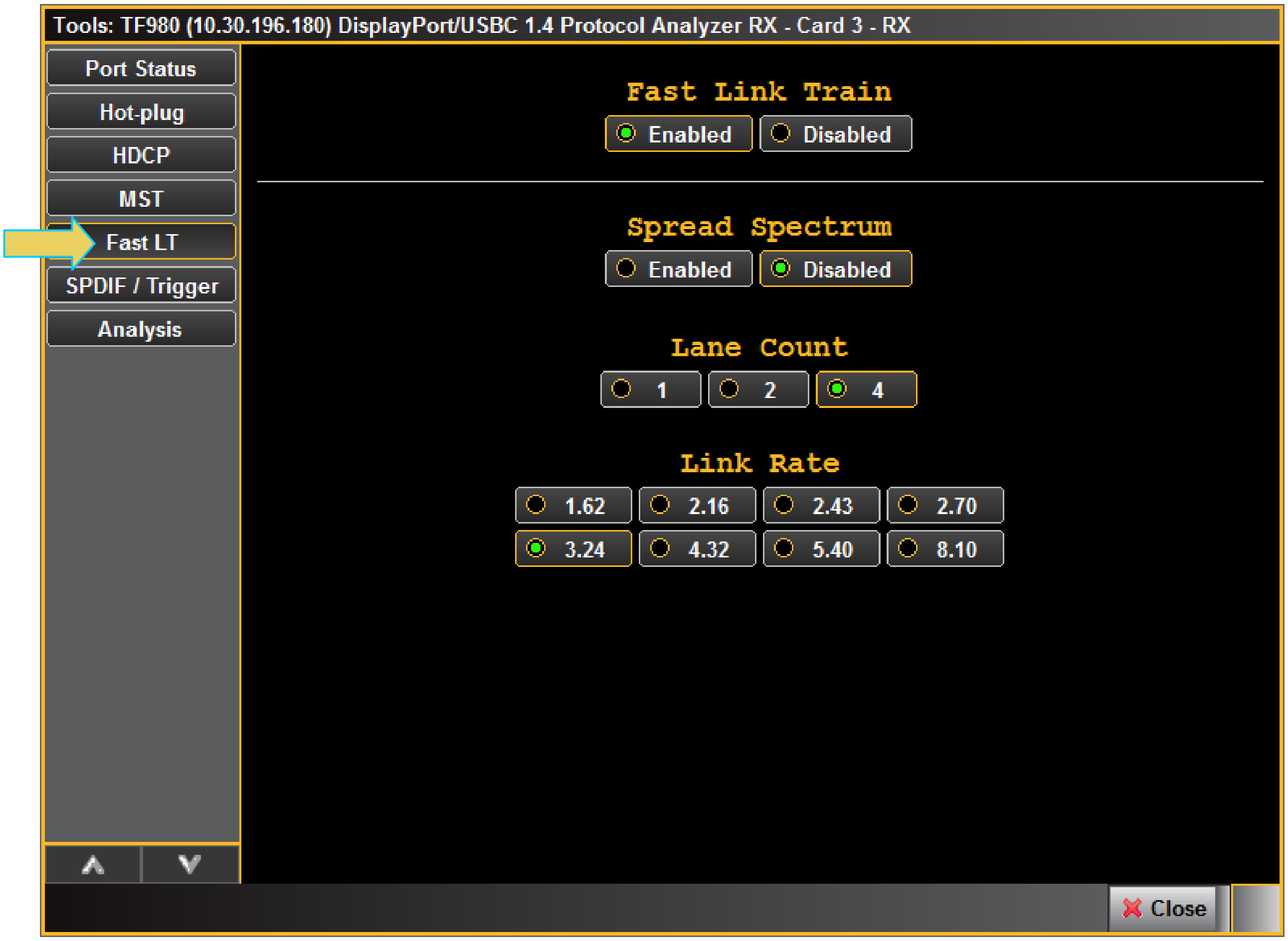
Use the following procedure to test eDP fast link training on an eDP source device.

1. Access the Analyzer Control panel from the **Tools** fly out menu.



```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 3 - RX
MEASURED | Lanes: 4 | Bandwidth: 8.10 | Active: 3840 x 2160 | V-Total: 2222 | VRate: 60.0 fps
METADATA | Res: 3840 x 2160 | Total: 4000 x 2222 | Sync: 32+, 5+ | Start: 112, 59 | CEA RGB, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 21519 | Nvid: 32768 | Maud: 0 | Naud: 0
METADATA | Pixel Clock: 531.93 MHz | DwnSp: off | HDCP-Sync: N | HDCP-Enc: off
```

The Analyzer Control Panel appears as shown below.



Tools: TF980 (10.30.196.180) DisplayPort/USBC 1.4 Protocol Analyzer RX - Card 3 - RX

Fast Link Train

● Enabled ○ Disabled

Spread Spectrum

○ Enabled ● Disabled

Lane Count

○ 1 ○ 2 ● 4

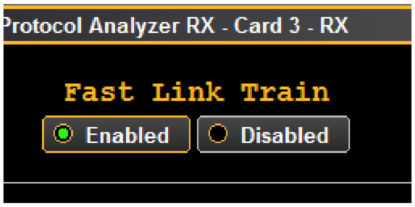
Link Rate

○ 1.62 ○ 2.16 ○ 2.43 ○ 2.70

● 3.24 ○ 4.32 ○ 5.40 ○ 8.10

Access the **Analyzer Control** panel from the **Tools** fly out menu.

2. Select the **Fast LT** button on the left to access the Fast Link Training controls. Refer to the screen above indicated by the arrow.
3. Enable Fast Link Training using the Enabled radio button indicated below:



rotocol Analyzer RX - Card 3 - RX

Fast Link Train

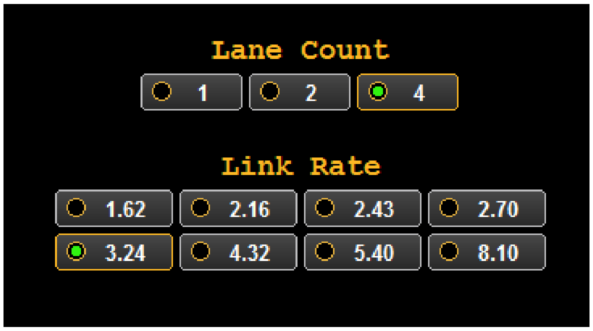
● Enabled ○ Disabled

4. Select to enable or disable **Spread Spectrum** according to your test requirements.

Spread Spectrum

○ Enabled ● Disabled

5. Select to Fast Link Training **Lane Count** and **Link Rate** according to your test requirements.



Lane Count

○ 1 ○ 2 ● 4

Link Rate

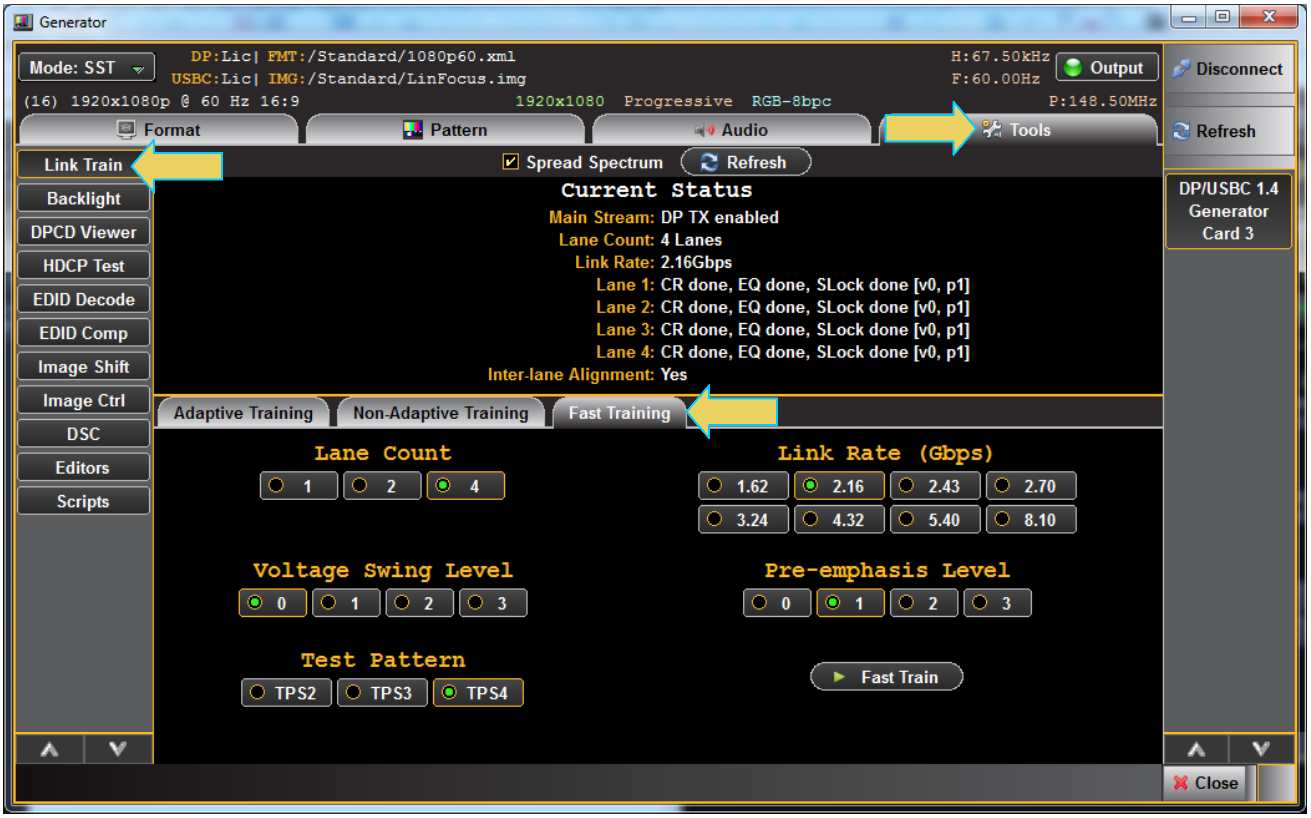
○ 1.62 ○ 2.16 ○ 2.43 ○ 2.70

● 3.24 ○ 4.32 ○ 5.40 ○ 8.10

8.2.2 Fast Link Training – Sink Tests

Use the following procedure to test eDP fast link training on an eDP sink device.

1. Access the Fast Link Training controls from the **Generator** panel and the **Tools** tab.



```
DP:Lic| FMT:/Standard/1080p60.xml                H:67.50kHz
USBC:Lic| IMG:/Standard/LinFocus.img             F:60.00Hz
(16) 1920x1080p @ 60 Hz 16:9    1920x1080  Progressive  RGB-8bpc    P:148.50MHz
```

☑ Spread Spectrum   Refresh

Current Status

Main Stream: DP TX enabled
Lane Count: 4 Lanes
Link Rate: 2.16Gbps
Lane 1: CR done, EQ done, SLock done [v0, p1]
Lane 2: CR done, EQ done, SLock done [v0, p1]
Lane 3: CR done, EQ done, SLock done [v0, p1]
Lane 4: CR done, EQ done, SLock done [v0, p1]
Inter-lane Alignment: Yes

Adaptive Training | Non-Adaptive Training | Fast Training

Lane Count: ○ 1 ○ 2 ● 4

Link Rate (Gbps): ○ 1.62 ● 2.16 ○ 2.43 ○ 2.70 ○ 3.24 ○ 4.32 ○ 5.40 ○ 8.10

Voltage Swing Level: ● 0 ○ 1 ○ 2 ○ 3

Pre-emphasis Level: ○ 0 ● 1 ○ 2 ○ 3

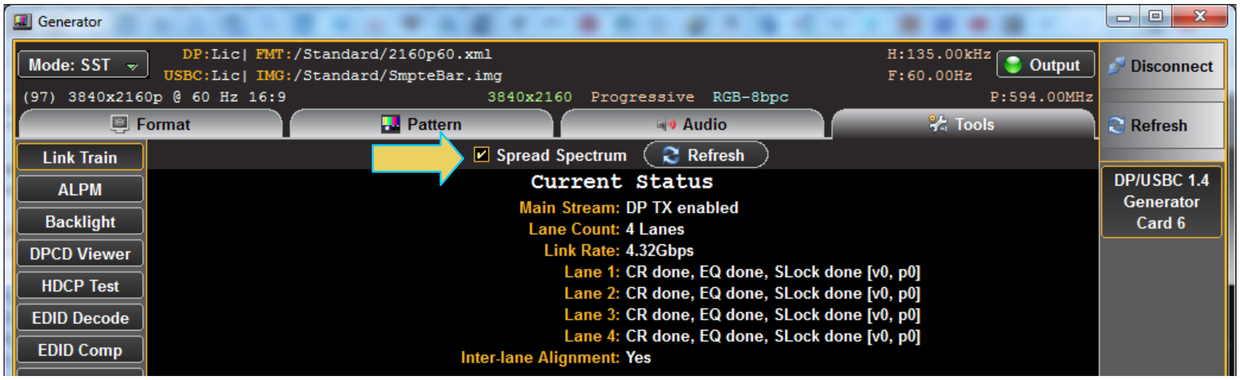
Test Pattern: ○ TPS2 ○ TPS3 ● TPS4

Fast Train

2. Select the Fast Train button on the left indicated by the arrow on the above screen shot.

   The Link Train window shows the current status on the top and the controls on the bottom. There is a third tab on the lower control panel for **Fast Training**.

3. Select the **Spread Spectrum** check box above the **Current Status** section of the window according to your test requirements.



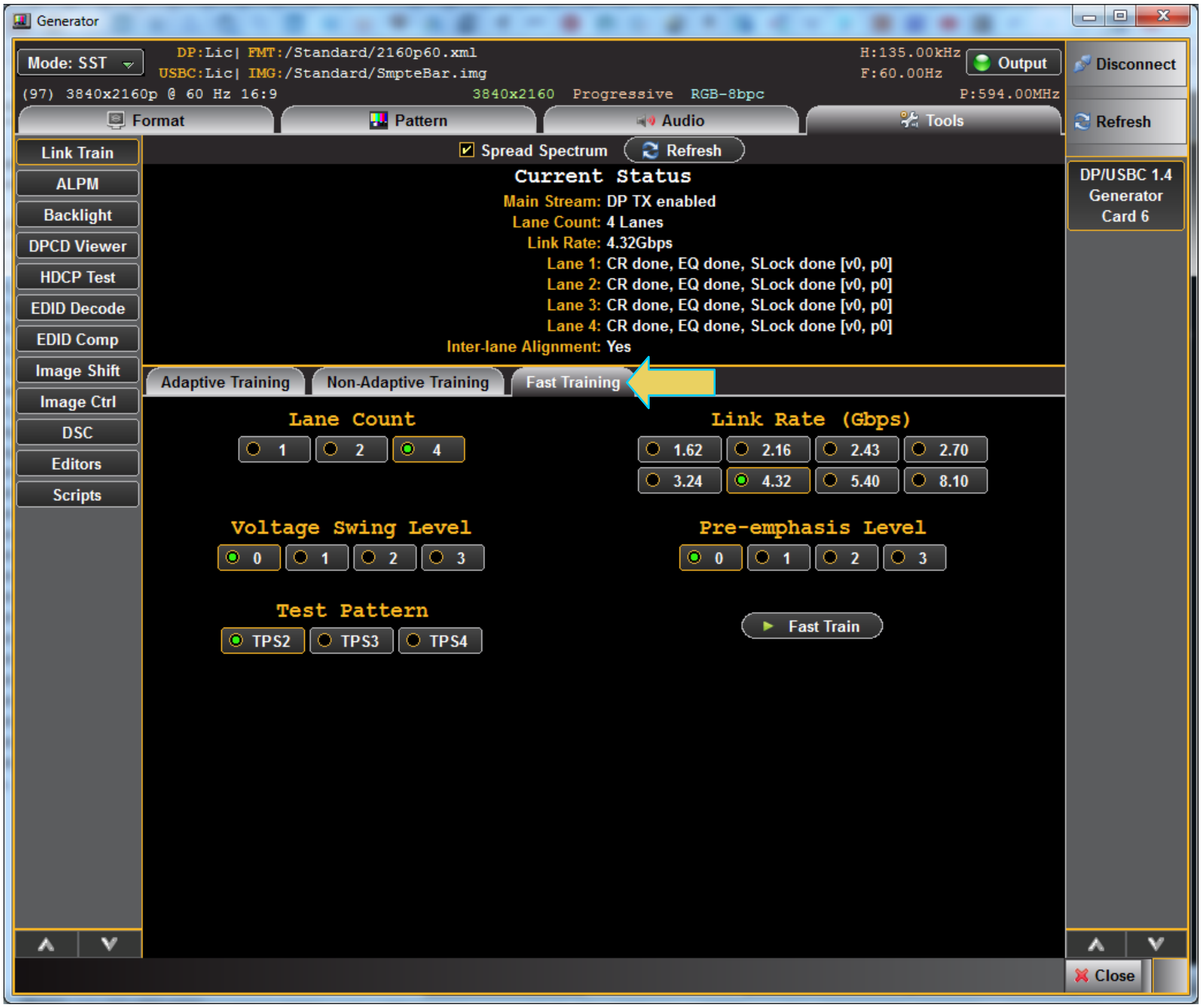
```
DP:Lic| FMT:/Standard/2160p60.xml                    H:135.00kHz
USBC:Lic| IMG:/Standard/SmpteBar.img                 F:60.00Hz
(97) 3840x2160p @ 60 Hz 16:9   3840x2160  Progressive  RGB-8bpc   P:594.00MHz
```

☑ Spread Spectrum

```
Current Status
Main Stream: DP TX enabled
Lane Count: 4 Lanes
Link Rate: 4.32Gbps
Lane 1: CR done, EQ done, SLock done [v0, p0]
Lane 2: CR done, EQ done, SLock done [v0, p0]
Lane 3: CR done, EQ done, SLock done [v0, p0]
Lane 4: CR done, EQ done, SLock done [v0, p0]
Inter-lane Alignment: Yes
```

4. Select the Spread Spectrum check box above the Current Status section of the window according to your test requirements.

5. Select the Fast Link Train tab on the lower panel. See below.



```
DP:Lic| FMT:/Standard/2160p60.xml                    H:135.00kHz
USBC:Lic| IMG:/Standard/SmpteBar.img                 F:60.00Hz
(97) 3840x2160p @ 60 Hz 16:9   3840x2160  Progressive  RGB-8bpc   P:594.00MHz
```

☑ Spread Spectrum

```
Current Status
Main Stream: DP TX enabled
Lane Count: 4 Lanes
Link Rate: 4.32Gbps
Lane 1: CR done, EQ done, SLock done [v0, p0]
Lane 2: CR done, EQ done, SLock done [v0, p0]
Lane 3: CR done, EQ done, SLock done [v0, p0]
Lane 4: CR done, EQ done, SLock done [v0, p0]
Inter-lane Alignment: Yes
```

Fast Training

Lane Count: ○ 1 ○ 2 ● 4

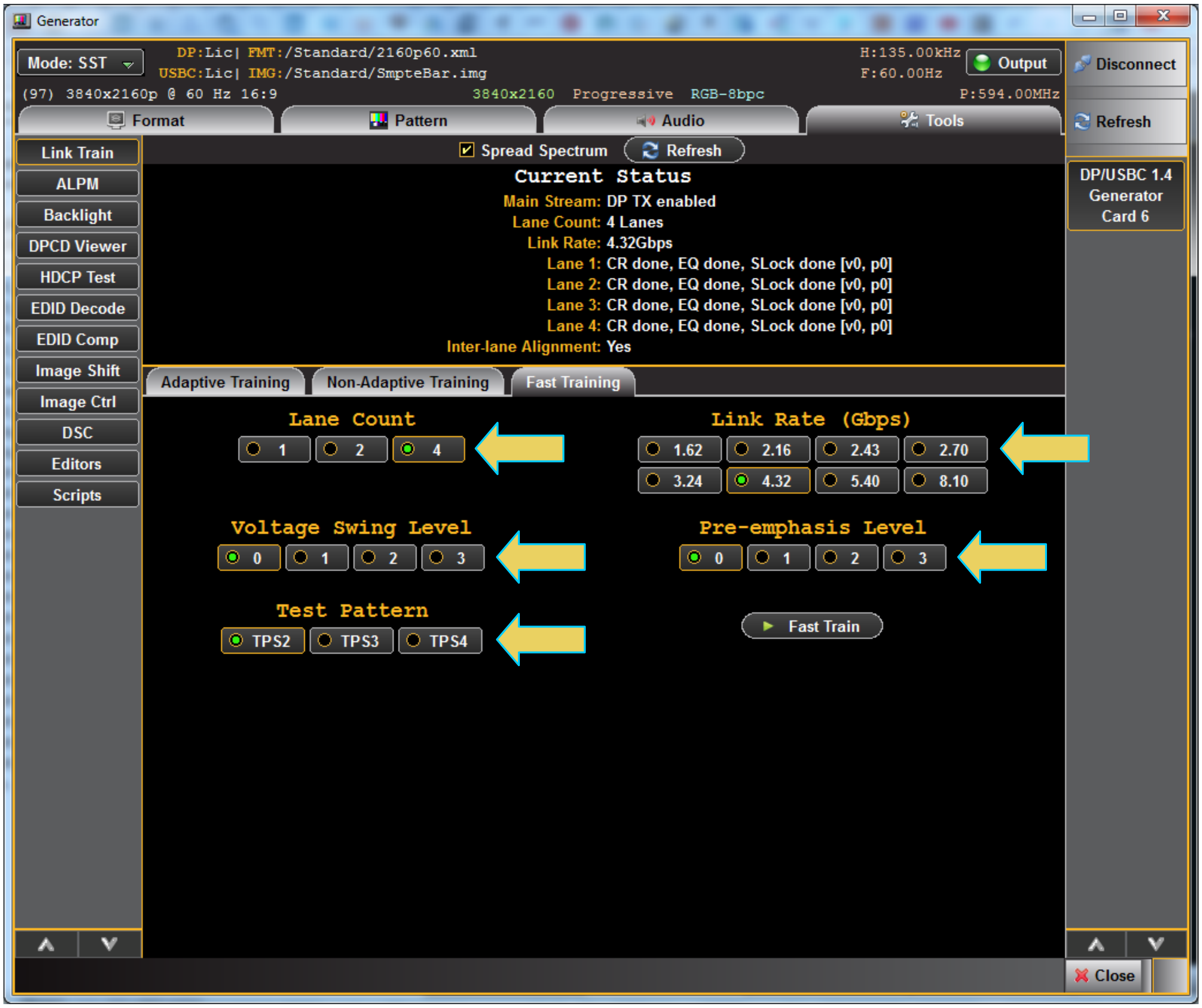
Link Rate (Gbps): ○ 1.62 ○ 2.16 ○ 2.43 ○ 2.70 ○ 3.24 ● 4.32 ○ 5.40 ○ 8.10

Voltage Swing Level: ● 0 ○ 1 ○ 2 ○ 3

Pre-emphasis Level: ● 0 ○ 1 ○ 2 ○ 3

Test Pattern: ● TPS2 ○ TPS3 ○ TPS4

6. Select the Lane Count, Link Rate, Voltage Swing, Pre-Emphasis and the Test Pattern in accordance with your eDP test requirements. See below.



```
DP:Lic| FMT:/Standard/2160p60.xml                H:135.00kHz
USBC:Lic| IMG:/Standard/SmpteBar.img             F:60.00Hz
(97) 3840x2160p @ 60 Hz 16:9    3840x2160  Progressive  RGB-8bpc    P:594.00MHz
```

☑ Spread Spectrum

Current Status

Main Stream: DP TX enabled
Lane Count: 4 Lanes
Link Rate: 4.32Gbps
Lane 1: CR done, EQ done, SLock done [v0, p0]
Lane 2: CR done, EQ done, SLock done [v0, p0]
Lane 3: CR done, EQ done, SLock done [v0, p0]
Lane 4: CR done, EQ done, SLock done [v0, p0]
Inter-lane Alignment: Yes

Lane Count
○ 1 ○ 2 ● 4

Link Rate (Gbps)
○ 1.62 ○ 2.16 ○ 2.43 ○ 2.70
○ 3.24 ● 4.32 ○ 5.40 ○ 8.10

Voltage Swing Level
● 0 ○ 1 ○ 2 ○ 3

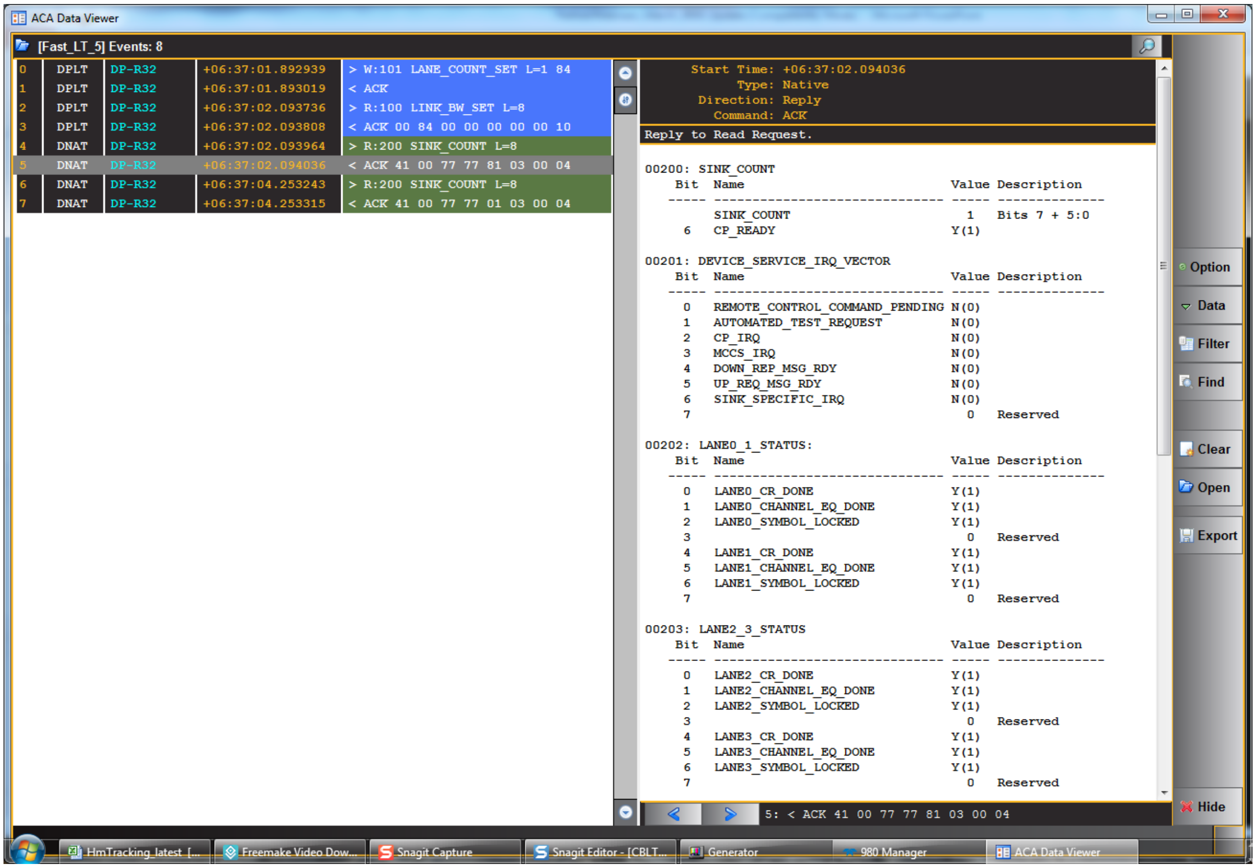
Pre-emphasis Level
● 0 ○ 1 ○ 2 ○ 3

Test Pattern
● TPS2 ○ TPS3 ○ TPS4

7. Click on the Fast Train button to initiate the link training. Then click on the Refresh button.

8.2.3 Fast Link Training – Monitoring the Fast Link Training Transactions on the Aux Channel

Refer to the ACA section Monitoring the DisplayPort auxiliary channels with the ACA utilities for procedures in monitoring the eDP fast link training and ALPM Aux Channel transactions associated with the eDP negotiations. A sample screen shot is shown below.



```
[Fast_LT_5] Events: 8
0  DPLT  DP-R32  +06:37:01.892939  > W:101 LANE_COUNT_SET L=1 84
1  DPLT  DP-R32  +06:37:01.893019  < ACK
2  DPLT  DP-R32  +06:37:02.093736  > R:100 LINK_BW_SET L=8
3  DPLT  DP-R32  +06:37:02.093808  < ACK 00 84 00 00 00 00 00 10
4  DNAT  DP-R32  +06:37:02.093964  > R:200 SINK_COUNT L=8
5  DNAT  DP-R32  +06:37:02.094036  < ACK 41 00 77 77 81 03 00 04
6  DNAT  DP-R32  +06:37:04.253243  > R:200 SINK_COUNT L=8
7  DNAT  DP-R32  +06:37:04.253315  < ACK 41 00 77 77 01 03 00 04
```

```
     Start Time: +06:37:02.094036
           Type: Native
      Direction: Reply
        Command: ACK
Reply to Read Request.

00200: SINK_COUNT
    Bit  Name                          Value Description
   ----- ----------------------------- ----- -------------
         SINK_COUNT                      1   Bits 7 + 5:0
     6   CP_READY                      Y(1)

00201: DEVICE_SERVICE_IRQ_VECTOR
    Bit  Name                          Value Description
   ----- ----------------------------- ----- -------------
     0   REMOTE_CONTROL_COMMAND_PENDING N(0)
     1   AUTOMATED_TEST_REQUEST        N(0)
     2   CP_IRQ                        N(0)
     3   MCCS_IRQ                      N(0)
     4   DOWN_REP_MSG_RDY              N(0)
     5   UP_REQ_MSG_RDY                N(0)
     6   SINK_SPECIFIC_IRQ             N(0)
     7                                   0   Reserved

00202: LANE0_1_STATUS:
    Bit  Name                          Value Description
   ----- ----------------------------- ----- -------------
     0   LANE0_CR_DONE                 Y(1)
     1   LANE0_CHANNEL_EQ_DONE         Y(1)
     2   LANE0_SYMBOL_LOCKED           Y(1)
     3                                   0   Reserved
     4   LANE1_CR_DONE                 Y(1)
     5   LANE1_CHANNEL_EQ_DONE         Y(1)
     6   LANE1_SYMBOL_LOCKED           Y(1)
     7                                   0   Reserved

00203: LANE2_3_STATUS
    Bit  Name                          Value Description
   ----- ----------------------------- ----- -------------
     0   LANE2_CR_DONE                 Y(1)
     1   LANE2_CHANNEL_EQ_DONE         Y(1)
     2   LANE2_SYMBOL_LOCKED           Y(1)
     3                                   0   Reserved
     4   LANE3_CR_DONE                 Y(1)
     5   LANE3_CHANNEL_EQ_DONE         Y(1)
     6   LANE3_SYMBOL_LOCKED           Y(1)
     7                                   0   Reserved

5: < ACK 41 00 77 77 81 03 00 04
```

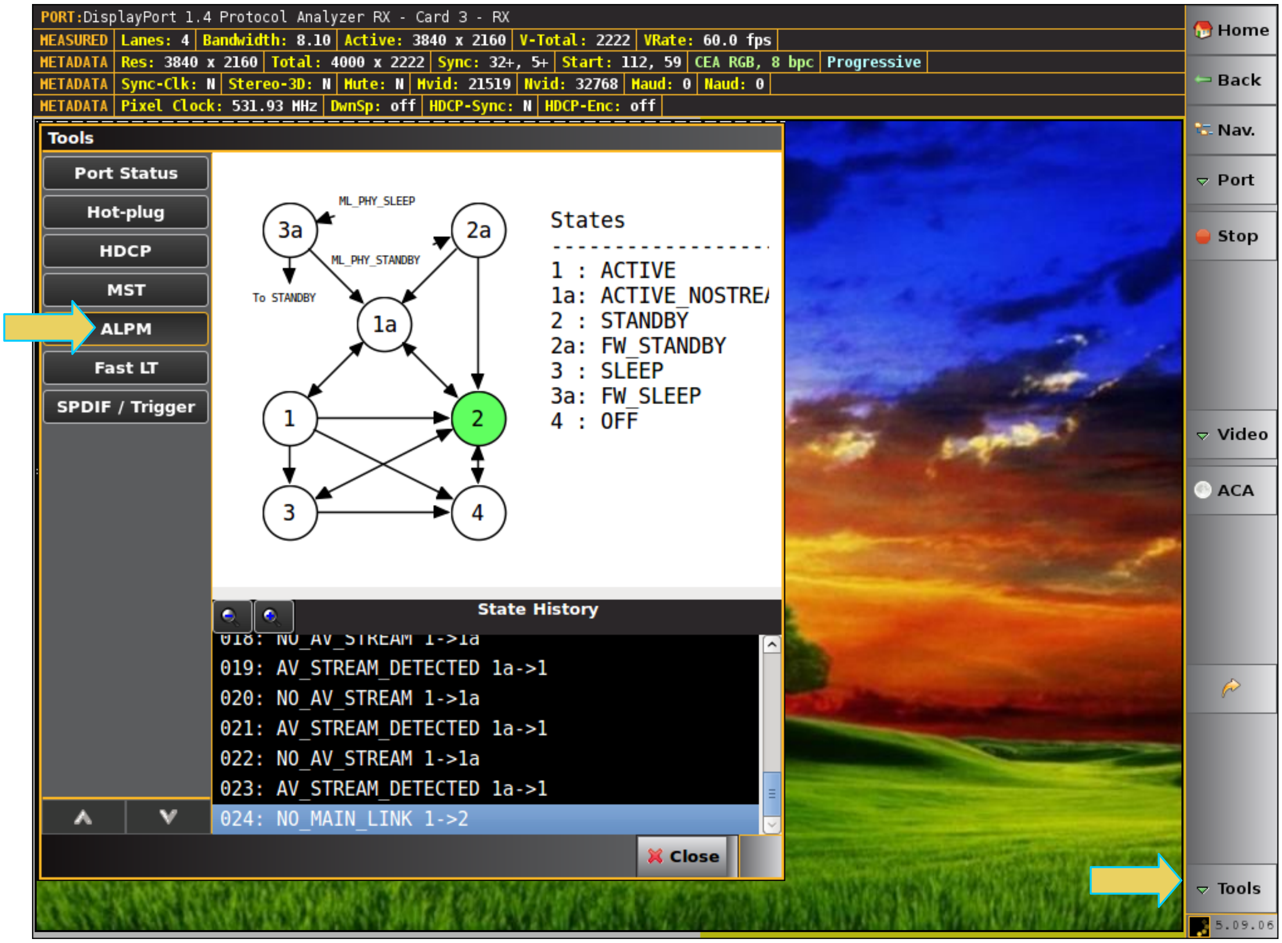
8.3 Advanced Link Power Management (ALPM)

This section provides procedures on testing eDP ALPM on eDP source and sink devices.

8.3.1 ALPM – Source Tests

Use the following procedure to test eDP ALPM on an eDP source device.

1. Access the Analyzer Control panel from the **Tools** fly out menu.



```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 3 - RX
MEASURED | Lanes: 4 | Bandwidth: 8.10 | Active: 3840 x 2160 | V-Total: 2222 | VRate: 60.0 fps
METADATA | Res: 3840 x 2160 | Total: 4000 x 2222 | Sync: 32+, 5+ | Start: 112, 59 | CEA RGB, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 21519 | Nvid: 32768 | Maud: 0 | Naud: 0
METADATA | Pixel Clock: 531.93 MHz | DwnSp: off | HDCP-Sync: N | HDCP-Enc: off
```

```
States
------------------
1 : ACTIVE
1a: ACTIVE_NOSTRE/
2 : STANDBY
2a: FW_STANDBY
3 : SLEEP
3a: FW_SLEEP
4 : OFF
```

State History

```
018: NO_AV_STREAM 1->1a
019: AV_STREAM_DETECTED 1a->1
020: NO_AV_STREAM 1->1a
021: AV_STREAM_DETECTED 1a->1
022: NO_AV_STREAM 1->1a
023: AV_STREAM_DETECTED 1a->1
024: NO_MAIN_LINK 1->2
```

The Analyzer Control Panel appears as shown below.

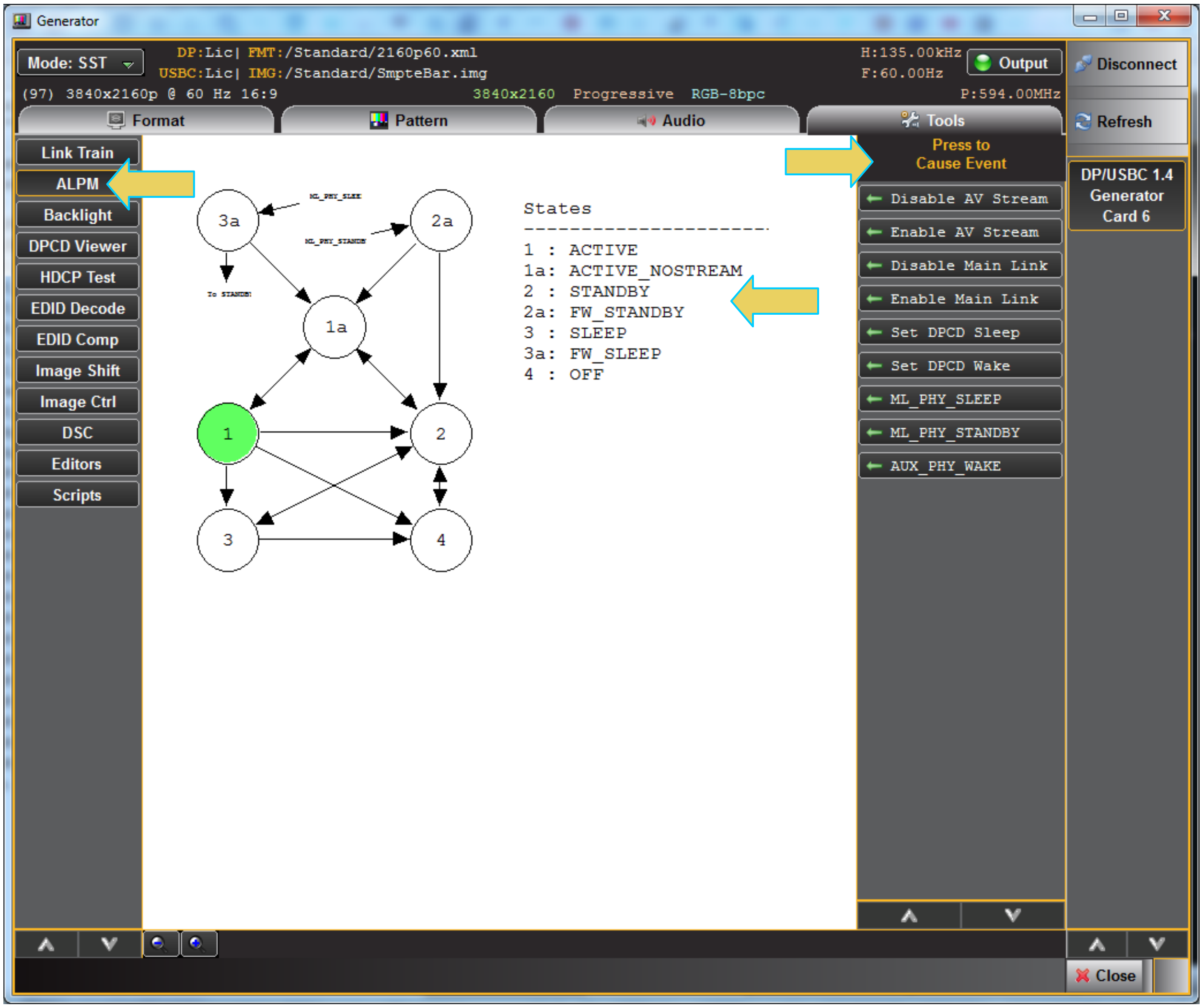
Access the **Analyzer Control** panel from the **Tools** fly out menu.

2. Select the **ALPM** button on the left to access the Fast Link Training controls. Refer to the screen above indicated by the arrow.
3. View the state diagram on the top of the **Tools** panel and the state transactions on the bottom.

8.3.2 ALPM – Sink Tests

Use the following procedure to test eDP ALPM on an eDP sink device.

1. Access the **ALPM** controls from the **Generator** panel and the **Tools** tab.



```
DP:Lic| FMT:/Standard/2160p60.xml          H:135.00kHz
USBC:Lic| IMG:/Standard/SmpteBar.img       F:60.00Hz
(97) 3840x2160p @ 60 Hz 16:9   3840x2160  Progressive  RGB-8bpc   P:594.00MHz
```

```
States
-----------------------
1 : ACTIVE
1a: ACTIVE_NOSTREAM
2 : STANDBY
2a: FW_STANDBY
3 : SLEEP
3a: FW_SLEEP
4 : OFF
```

2. Select the ALPM button on the left indicated by the arrow on the above screen shot.

   The ALPM window shows the current state on the left side of the panel.

3. Select the activation buttons on the right side of the window to cause transitions to the various ALPM states.

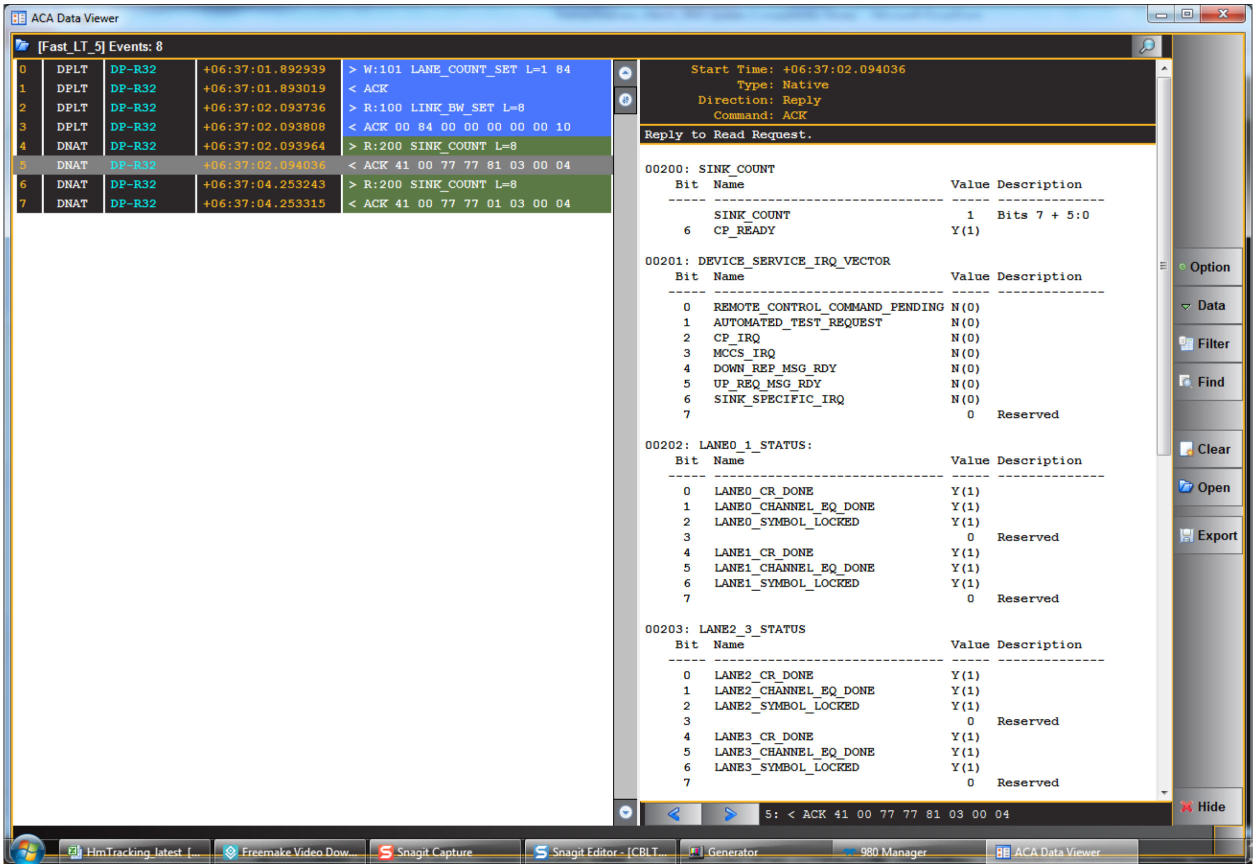
   The following table describes the ALPM **Activation** function buttons.

ALPM State Transition Buttons	
ALPM Activation Buttons	**Function**
Disable AV Stream ← Disable AV Stream	Disables the streaming of audio and video over the main link. The link is trained and the source is sending either an idle pattern or a ML_PHY_LOCK pattern. Causes a transition to the 1a state: Active NoStream.
Enable AV Stream ← Enable AV Stream	Enables the streaming of audio and video over the main link. The link is trained and the source is sending an AV stream. Causes a transition to the 1 state: Active.
Disable Main Link	Disables the Main Link.

ALPM State Transition Buttons	
ALPM Activation Buttons	**Function**
← Disable Main Link	
Enable Main Link ← Enable Main Link	.Enables the Main Link.
Set DPCD Sleep ← Set DPCD Sleep	Puts the ALPM sink in the Sleep state by writing to DPCD registers over the Aux Channel.
Set DPCD Wake ← Set DPCD Wake	Puts the ALPM sink in the Wake state by writing to DPCD registers over the Aux Channel.
ML Phy Sleep ← ML_PHY_SLEEP	Puts the ALPM sink in the Sleep state by sending K-character sequence over the Main Link.
ML Phy Standby ← ML_PHY_STANDBY	Puts the ALPM sink in the Standby state by sending K-character sequence over the Main Link.
Aux Phy Wake ← AUX_PHY_WAKE	Puts the ALPM sink in the Standby state by writing a bit sequence over the Aux Channel.

8.3.3 Fast Link Training – Monitoring the ALPM Transactions on the Aux Channel

Refer to the ACA section Monitoring the DisplayPort auxiliary channels with the ACA utilities for procedures in monitoring the eDP fast link training and ALPM Aux Channel transactions associated with the eDP negotiations. A sample screen shot is shown below.



```
0  DPLT  DP-R32  +06:37:01.892939  > W:101 LANE_COUNT_SET L=1 84
1  DPLT  DP-R32  +06:37:01.893019  < ACK
2  DPLT  DP-R32  +06:37:02.093736  > R:100 LINK_BW_SET L=8
3  DPLT  DP-R32  +06:37:02.093808  < ACK 00 84 00 00 00 00 00 10
4  DNAT  DP-R32  +06:37:02.093964  > R:200 SINK_COUNT L=8
5  DNAT  DP-R32  +06:37:02.094036  < ACK 41 00 77 77 81 03 00 04
6  DNAT  DP-R32  +06:37:04.253243  > R:200 SINK_COUNT L=8
7  DNAT  DP-R32  +06:37:04.253315  < ACK 41 00 77 77 01 03 00 04
```

```
      Start Time: +06:37:02.094036
            Type: Native
       Direction: Reply
         Command: ACK
Reply to Read Request.

00200: SINK_COUNT
    Bit  Name                          Value Description
   ----- ----------------------------- ----- -------------
         SINK_COUNT                      1   Bits 7 + 5:0
     6   CP_READY                      Y(1)

00201: DEVICE_SERVICE_IRQ_VECTOR
    Bit  Name                          Value Description
   ----- ----------------------------- ----- -------------
     0   REMOTE_CONTROL_COMMAND_PENDING N(0)
     1   AUTOMATED_TEST_REQUEST        N(0)
     2   CP_IRQ                        N(0)
     3   MCCS_IRQ                      N(0)
     4   DOWN_REP_MSG_RDY              N(0)
     5   UP_REQ_MSG_RDY                N(0)
     6   SINK_SPECIFIC_IRQ             N(0)
     7                                   0   Reserved

00202: LANE0_1_STATUS:
    Bit  Name                          Value Description
   ----- ----------------------------- ----- -------------
     0   LANE0_CR_DONE                 Y(1)
     1   LANE0_CHANNEL_EQ_DONE         Y(1)
     2   LANE0_SYMBOL_LOCKED           Y(1)
     3                                   0   Reserved
     4   LANE1_CR_DONE                 Y(1)
     5   LANE1_CHANNEL_EQ_DONE         Y(1)
     6   LANE1_SYMBOL_LOCKED           Y(1)
     7                                   0   Reserved

00203: LANE2_3_STATUS
    Bit  Name                          Value Description
   ----- ----------------------------- ----- -------------
     0   LANE2_CR_DONE                 Y(1)
     1   LANE2_CHANNEL_EQ_DONE         Y(1)
     2   LANE2_SYMBOL_LOCKED           Y(1)
     3                                   0   Reserved
     4   LANE3_CR_DONE                 Y(1)
     5   LANE3_CHANNEL_EQ_DONE         Y(1)
     6   LANE3_SYMBOL_LOCKED           Y(1)
     7                                   0   Reserved

5: < ACK 41 00 77 77 81 03 00 04
```

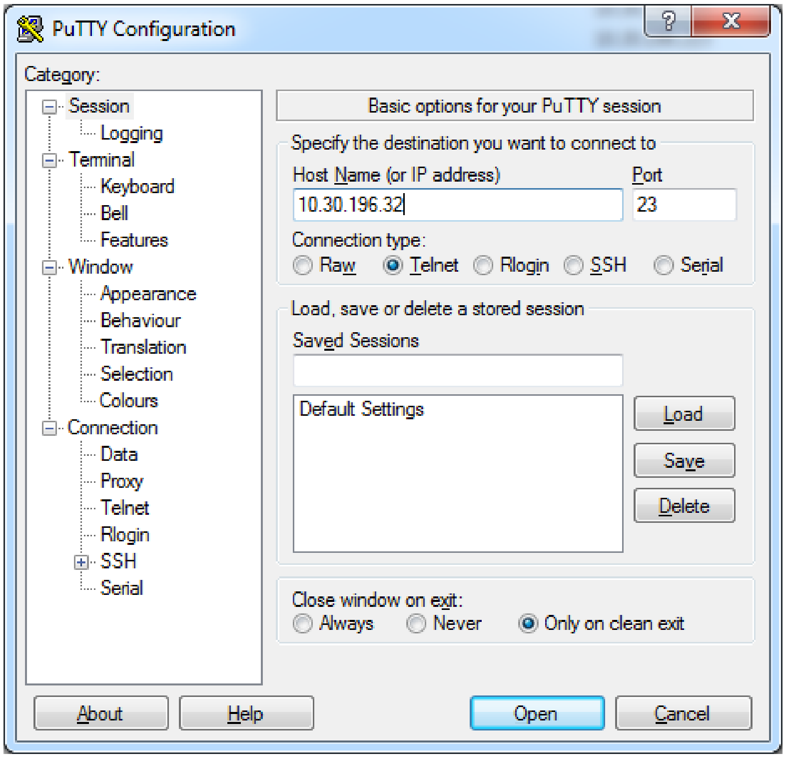
8.4 Alternate Scrambler Seed

Use the following procedure to configure the number of downstream MST nodes.

8.4.1 Alternate Scrambler Seed

The DP 1.4 eDP-capable module supports the alternate scrambler seed. Currently the feature is supported only through the command line. Use the following procedures to activate the alternate scrambler seed for an eDP source.

1. Access the command line interface through the 980 GUI console or a terminal program such as PUTTY as shown below.



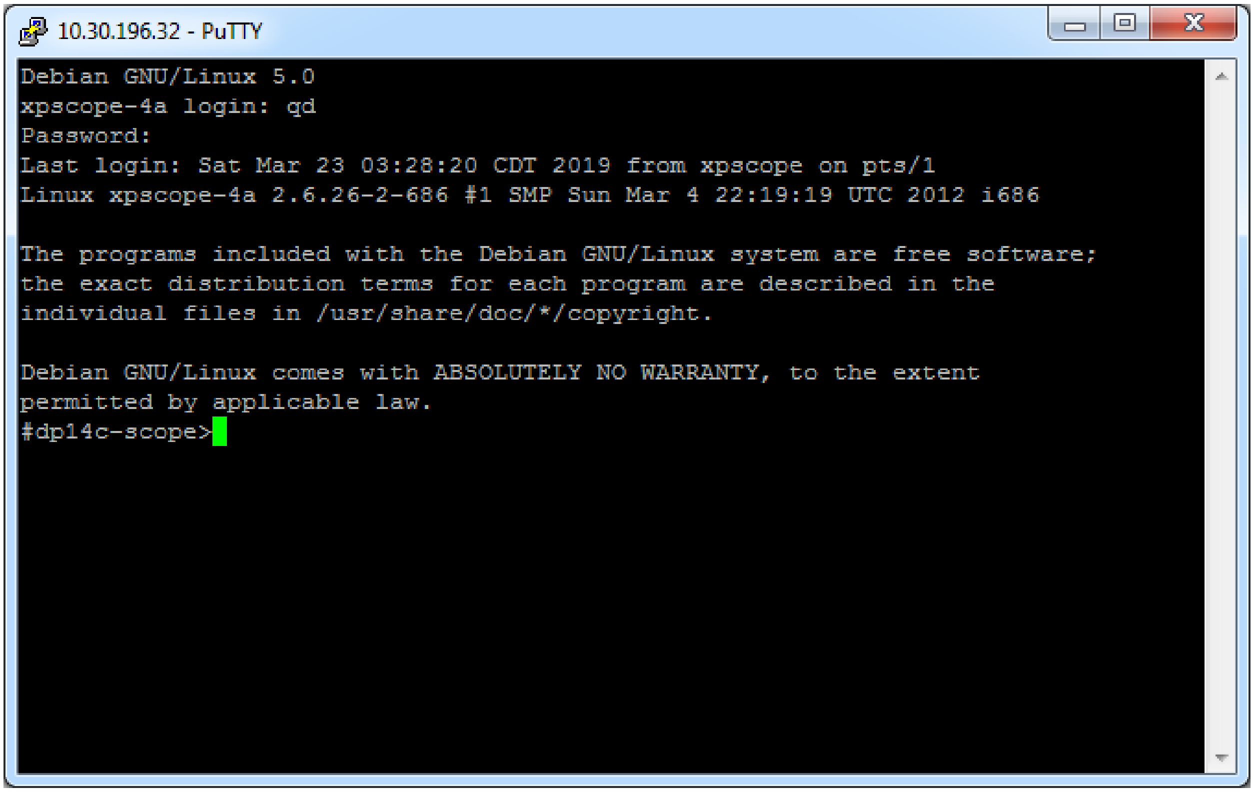
Host Name (or IP address): 10.30.196.32

Port: 23

Connection type: ○ Raw ● Telnet ○ Rlogin ○ SSH ○ Serial

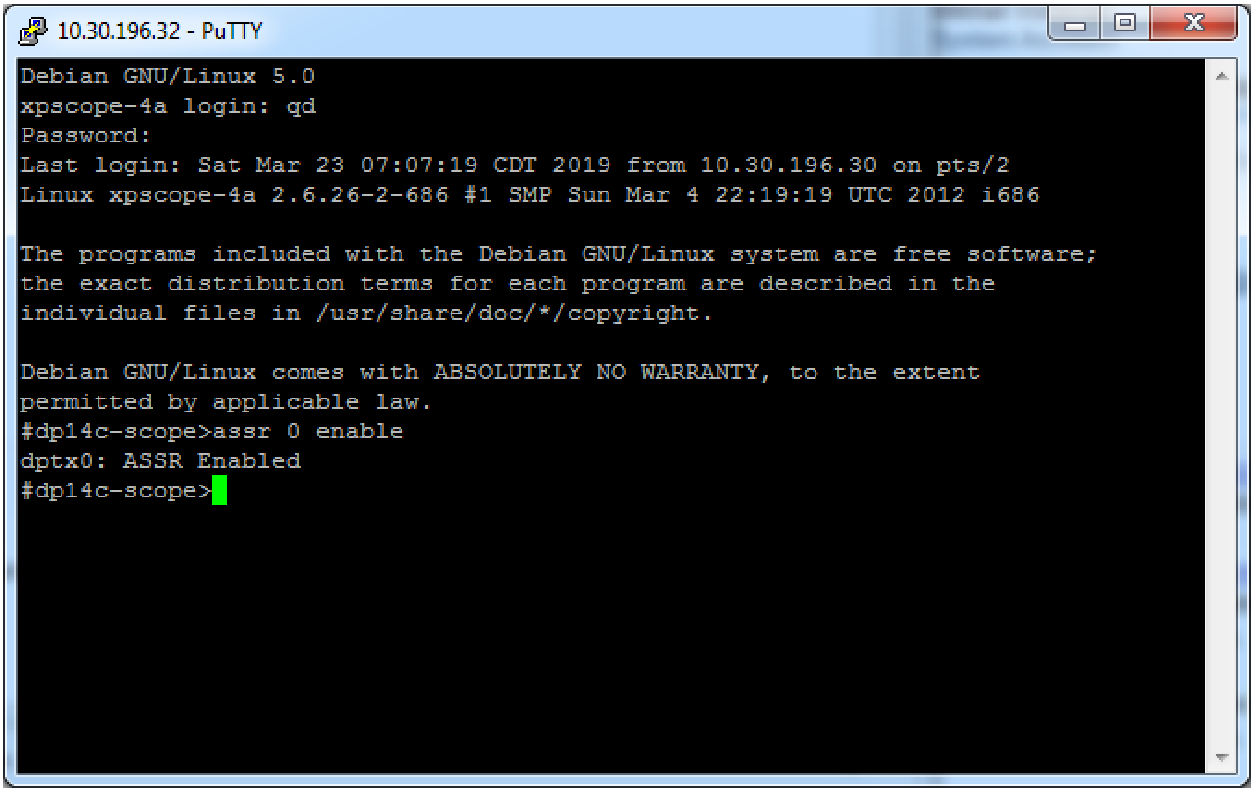
Close window on exit: ○ Always ○ Never ● Only on clean exit

2. Enter qd for the login.
3. Enter qd for the password. The following screen appears.



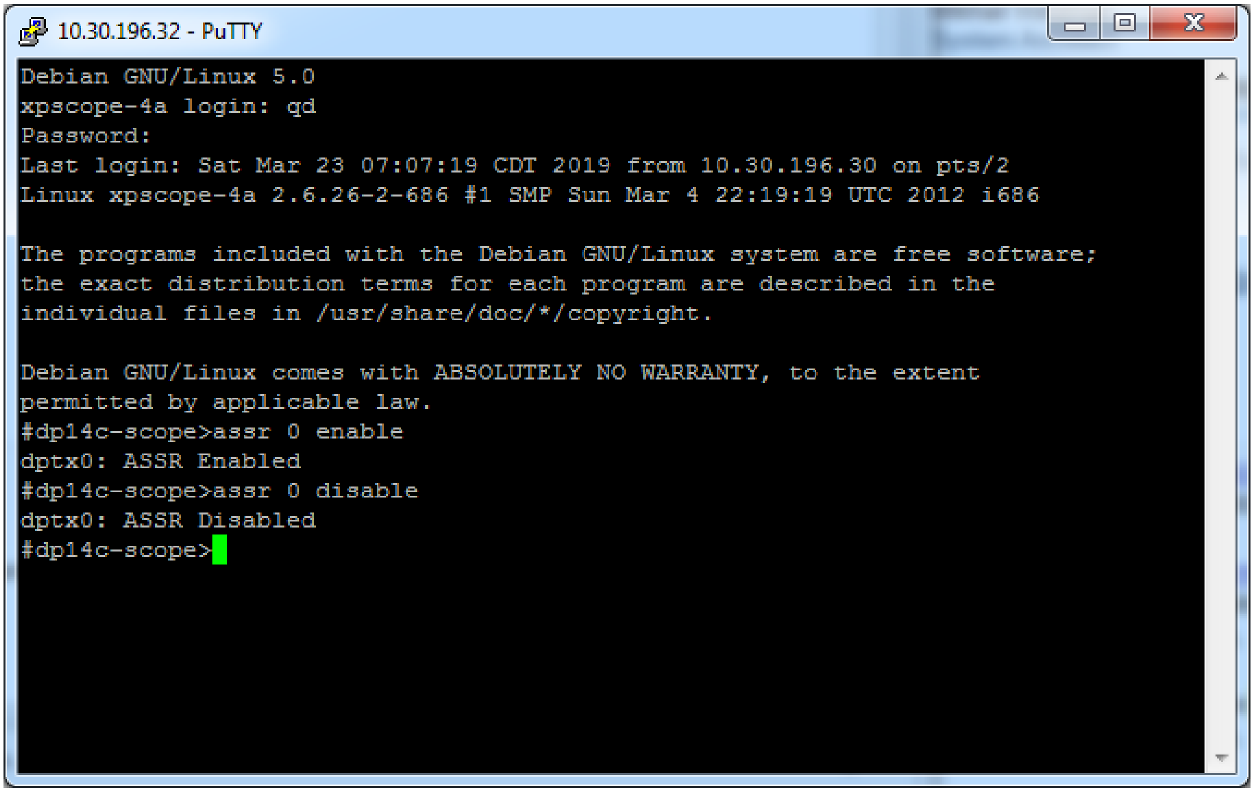
```
Debian GNU/Linux 5.0
xpscope-4a login: qd
Password:
Last login: Sat Mar 23 03:28:20 CDT 2019 from xpscope on pts/1
Linux xpscope-4a 2.6.26-2-686 #1 SMP Sun Mar 4 22:19:19 UTC 2012 i686

The programs included with the Debian GNU/Linux system are free software;
the exact distribution terms for each program are described in the
individual files in /usr/share/doc/*/copyright.

Debian GNU/Linux comes with ABSOLUTELY NO WARRANTY, to the extent
permitted by applicable law.
#dp14c-scope>
```

4. To enable alternate scrambler:



```
Debian GNU/Linux 5.0
xpscope-4a login: qd
Password:
Last login: Sat Mar 23 07:07:19 CDT 2019 from 10.30.196.30 on pts/2
Linux xpscope-4a 2.6.26-2-686 #1 SMP Sun Mar 4 22:19:19 UTC 2012 i686

The programs included with the Debian GNU/Linux system are free software;
the exact distribution terms for each program are described in the
individual files in /usr/share/doc/*/copyright.

Debian GNU/Linux comes with ABSOLUTELY NO WARRANTY, to the extent
permitted by applicable law.
#dp14c-scope>assr 0 enable
dptx0: ASSR Enabled
#dp14c-scope>
```

5. To disable alternate scrambler:



```
Debian GNU/Linux 5.0
xpscope-4a login: qd
Password:
Last login: Sat Mar 23 07:07:19 CDT 2019 from 10.30.196.30 on pts/2
Linux xpscope-4a 2.6.26-2-686 #1 SMP Sun Mar 4 22:19:19 UTC 2012 i686

The programs included with the Debian GNU/Linux system are free software;
the exact distribution terms for each program are described in the
individual files in /usr/share/doc/*/copyright.

Debian GNU/Linux comes with ABSOLUTELY NO WARRANTY, to the extent
permitted by applicable law.
#dp14c-scope>assr 0 enable
dptx0: ASSR Enabled
#dp14c-scope>assr 0 disable
dptx0: ASSR Disabled
#dp14c-scope>
```

8.5 Backlight Control

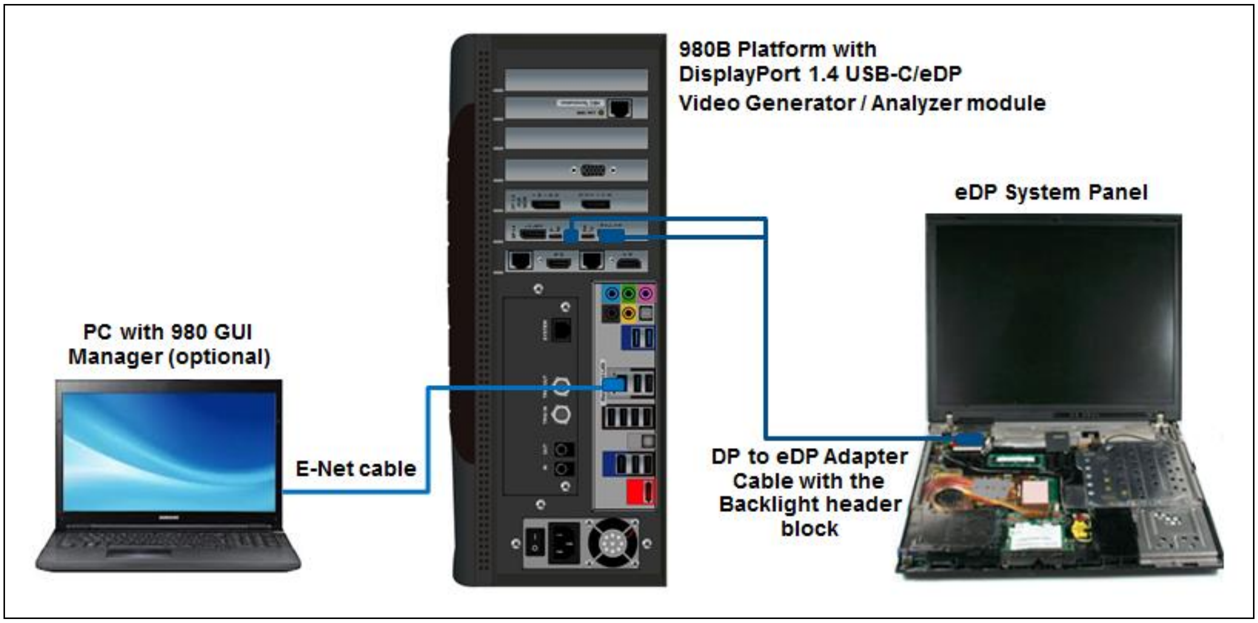
This section describes backlight control and provides procedures for using the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module to control the backlight of an eDP TCON panel subsystem.

There are two methods of controlling the backlight: 1) Aux control messages, 2) control backlight thought direct connection leads.

8.5.1 Backlight Control Test Connections

This subsection provides procedures on how to connect the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module to your eDP display panel for backlight control. You will use the Standard DisplayPort connector and the eDP header pin block and a special Teledyne LeCroy provided cable assembly.

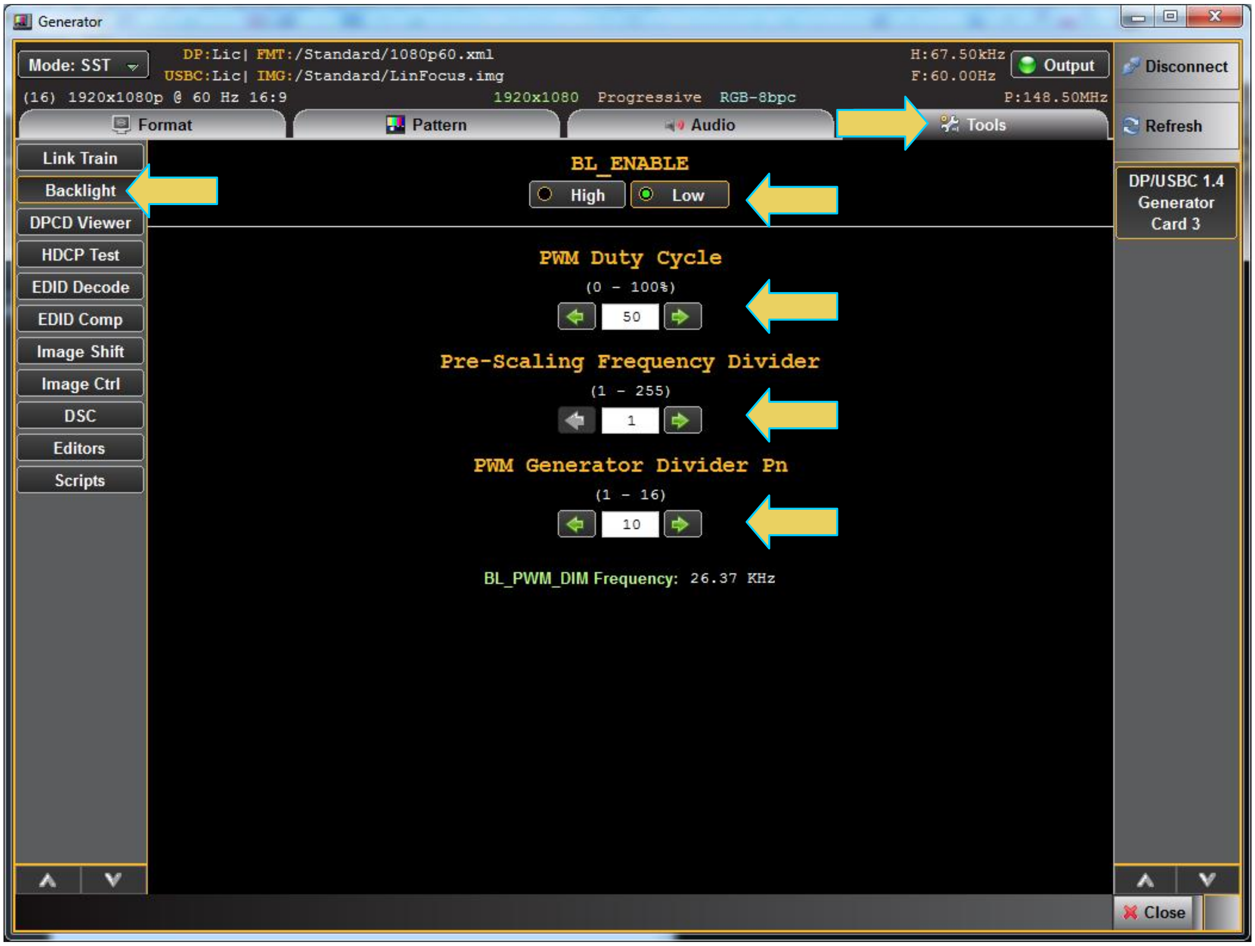
1. Connect the provided cable from the eDP System Panel using the eDP connector.
2. Connect the other end with the standard DP connector and the eDP header block the provided cable to the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module. Refer to the diagram below.



8.5.2 Backlight Control – Sink Tests

Use the following procedure to test eDP backlight on an eDP sink device.

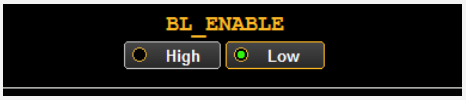
1. Access the **Backlight** controls from the **Generator** panel and the **Tools** tab. Refer to the screen below.

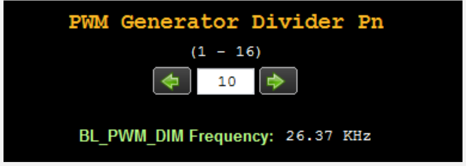


DP:Lic| FMT:/Standard/1080p60.xml
USBC:Lic| IMG:/Standard/LinFocus.img
(16) 1920x1080p @ 60 Hz 16:9 1920x1080 Progressive RGB-8bpc
H:67.50kHz F:60.00Hz P:148.50MHz

BL_ENABLE: ○ High ● Low
PWM Duty Cycle: 50
Pre-Scaling Frequency Divider: 1
PWM Generator Divider Pn: 10
BL_PWM_DIM Frequency: 26.37 KHz

The following table describes the Tx Backlight Controls.

ALPM State Transition Buttons	
Backlight Enable  	Enables the Backlight control feature.
PWM Duty Cycle  	The Duty Cycle control can be modified in percentages from 0 to 100%. The percentage of the Duty Cycle controls the percentage of the voltage high period.
Pre-Scaling Freq Divider  	The Pre-Scaling Frequency Divider is used to pre-scale the backlight PWM Cycle frequency.
PWM Generator Divider Pn	The PWM Generator Divider is used to create backlight dimming PWM signal.

ALPM State Transition Buttons	
 PWM Generator Divider Pn (1 - 16) 10 BL_PWM_DIM Frequency: 26.37 KHz	

9 Pattern List Editor

Use the following procedures to create a custom list of test patterns. The **Pattern List Editor** can be used either on the embedded 980 GUI Manager or the external 980 GUI Manager. The examples in this procedure use the external 980 GUI Manager.

9.1 Creating a custom list of test patterns

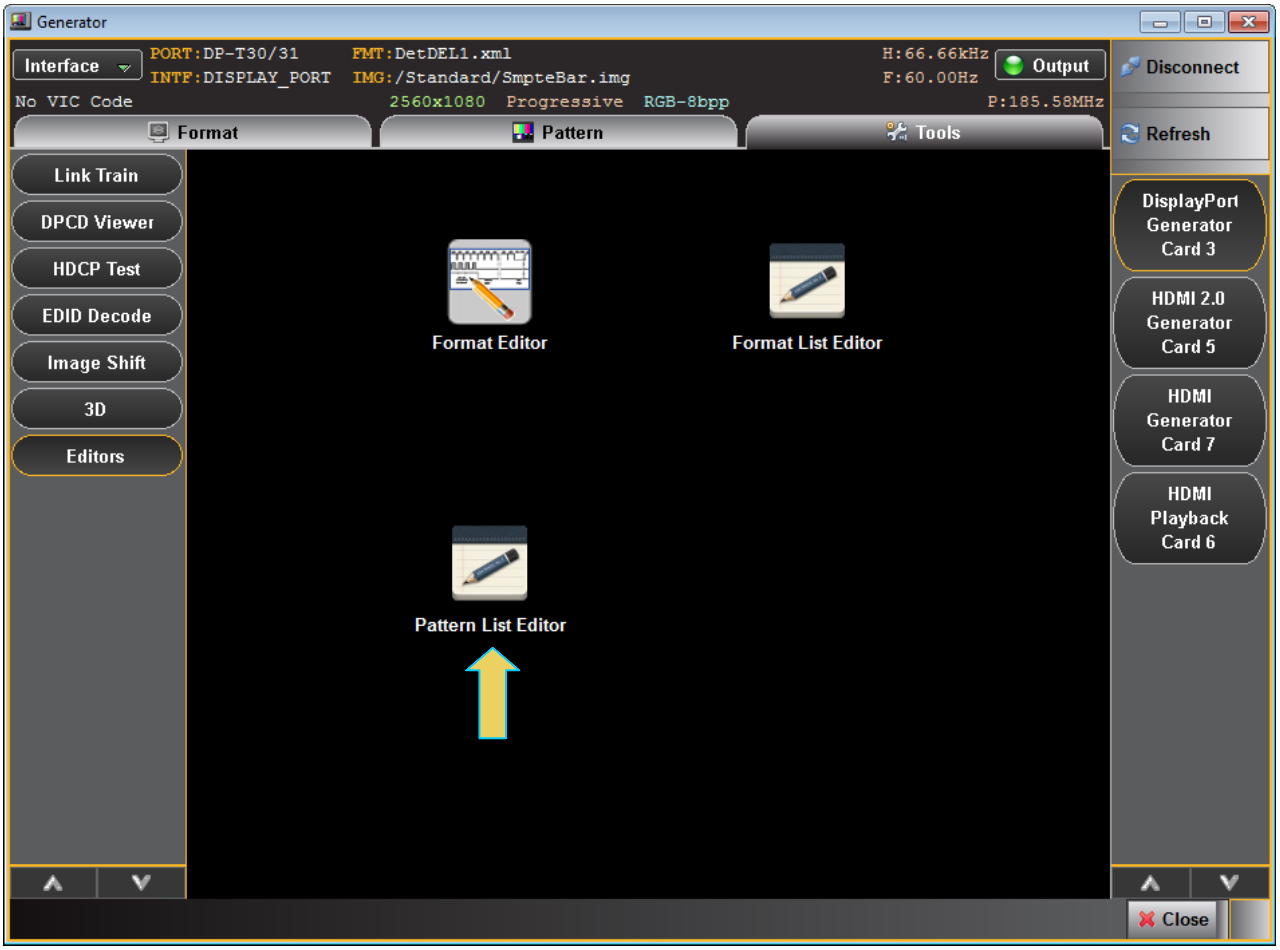
This subsection describes how you can create a custom pattern list.

To create a custom list of test patterns:

1. From the Editors Page of the Apps panel, select **Pattern List Editor** from the **View** menu as shown below.

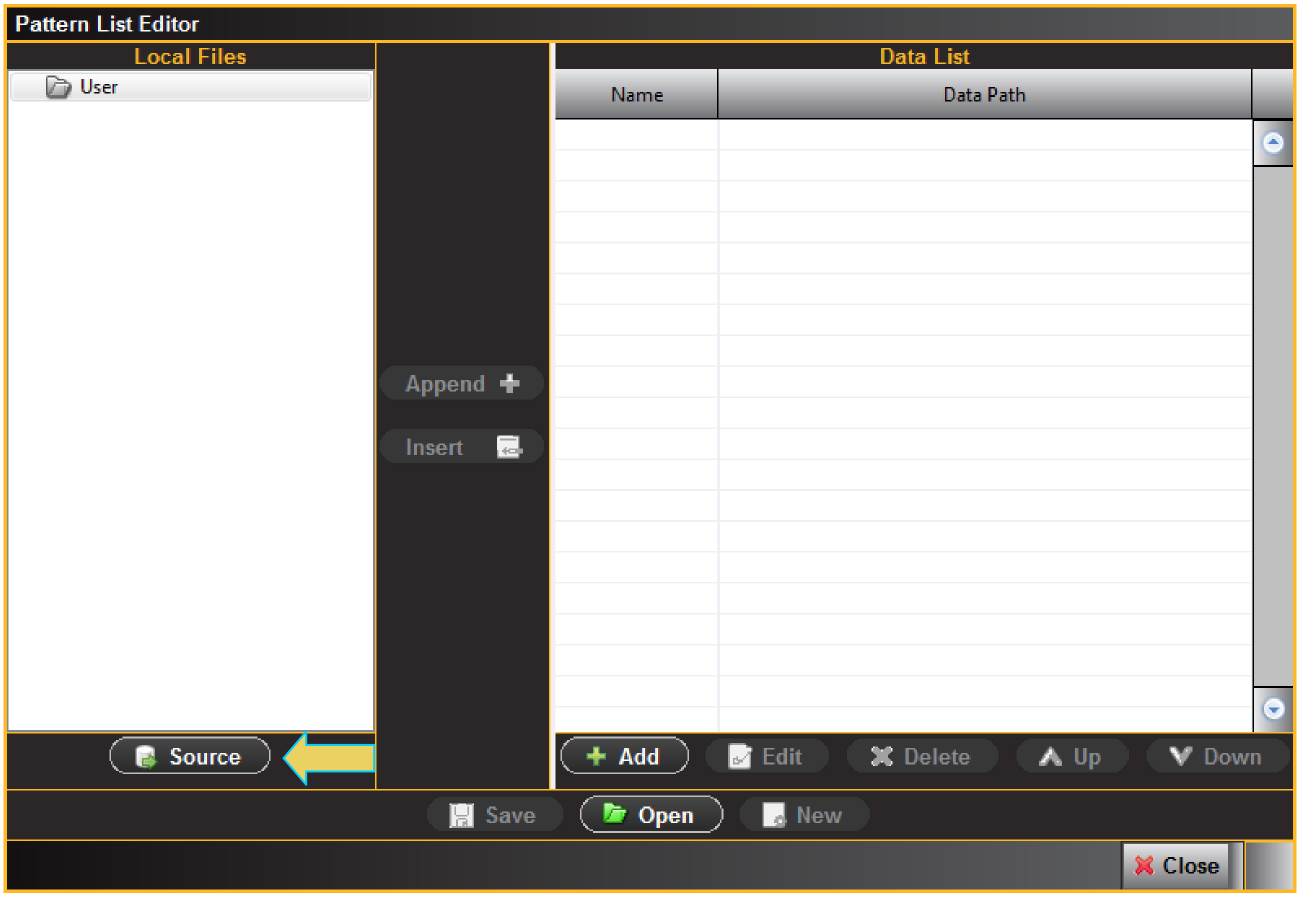
Alternatively, if you are using the embedded 980 GUI Manager you can access the **Pattern List Editor** from the **Generator Tools tab**. Be sure to select the correct Transmitter (Generator) port on the right side:

The list of editors appears as shown in the screen below.



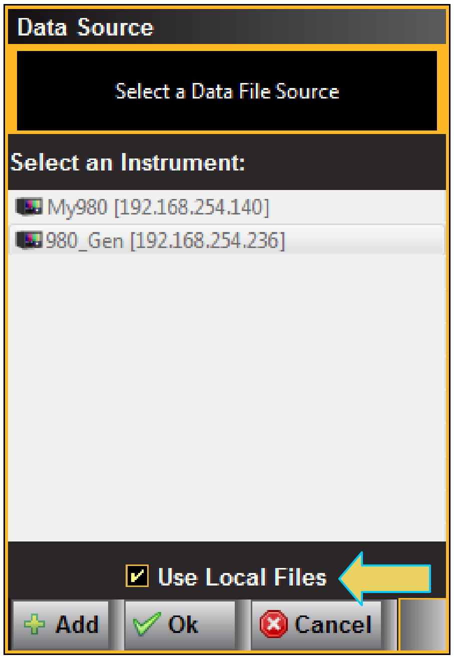
1. Select the Pattern List Editor icon.

The **Pattern List Editor** appears as shown below:



2. Click on the **Source** button on the lower left under Local Files (indicated in the diagram above). The Data **Source** dialog box will appear enabling you to select between using files on your PC or using files on the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module to create your custom list. This dialog box also enables you to select the particular 980 (if there is more than one on the network). (You can also add a new 980 through this dialog box.)

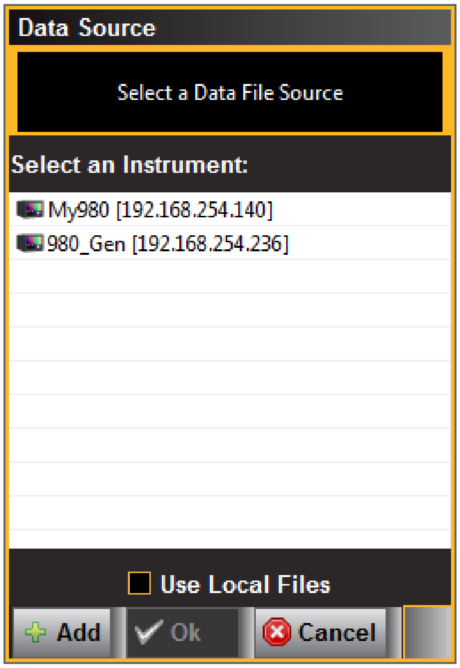
   Note: “Local Files” when using the external 980 GUI Manager means that you are using the files stored locally on your host PC. If you deselect Local Files on the dialog box below you are viewing files on the 980 file system.



☑ Use Local Files

3. Select the instrument that you want to use as the source of your test patterns. (If there are multiple 980s on the network you will have to choose which one.) Note that if you are using the **Pattern List Editor** on the external 980 GUI Manager, the custom Pattern List is stored on the host PC not the 980 instrument itself.

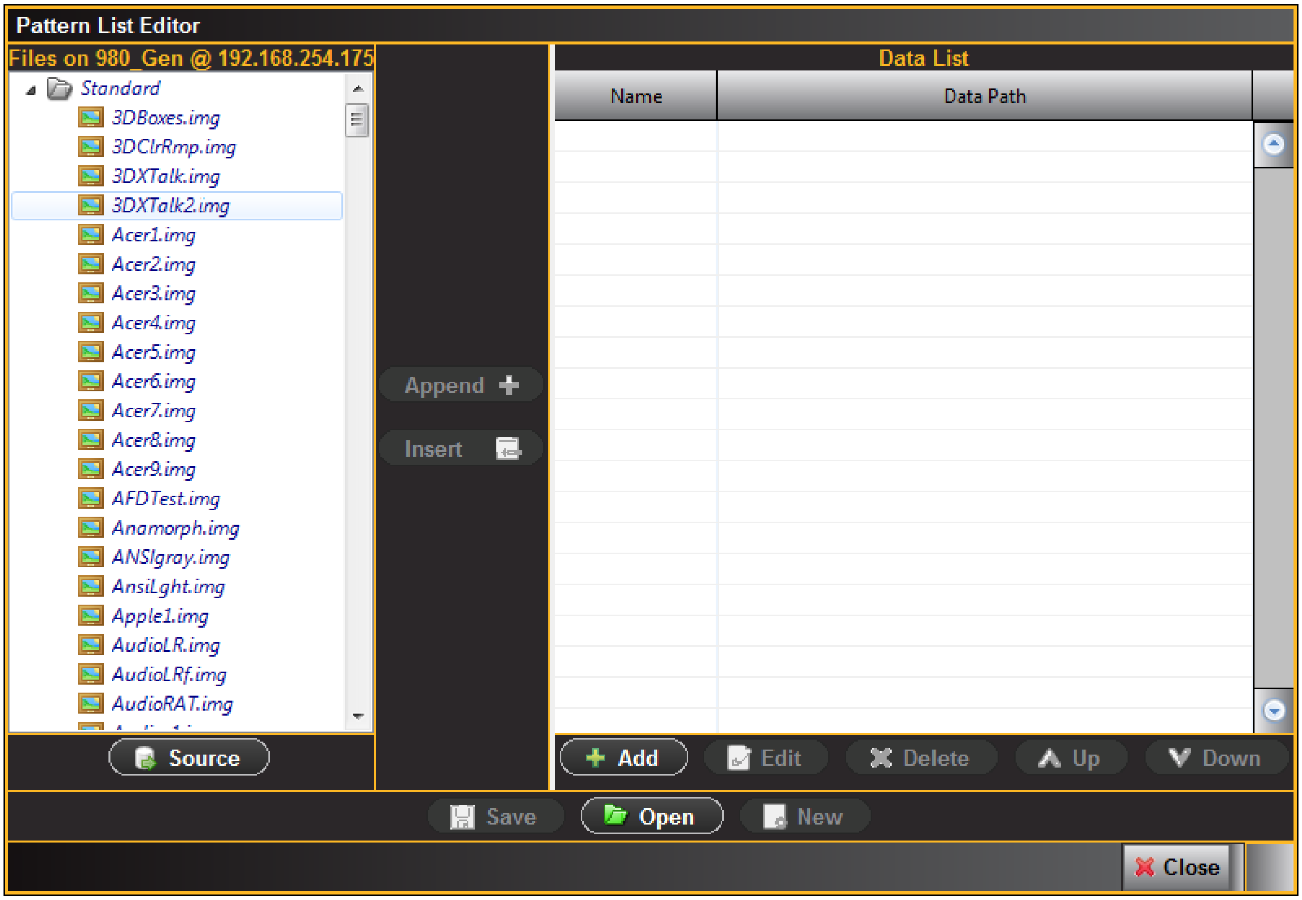
   Note that you will have to deselect **Use Local Files** in order to select a 980. If you do not de-select **Use Local Files**, then you will be using test patterns on your host PC to create your list.

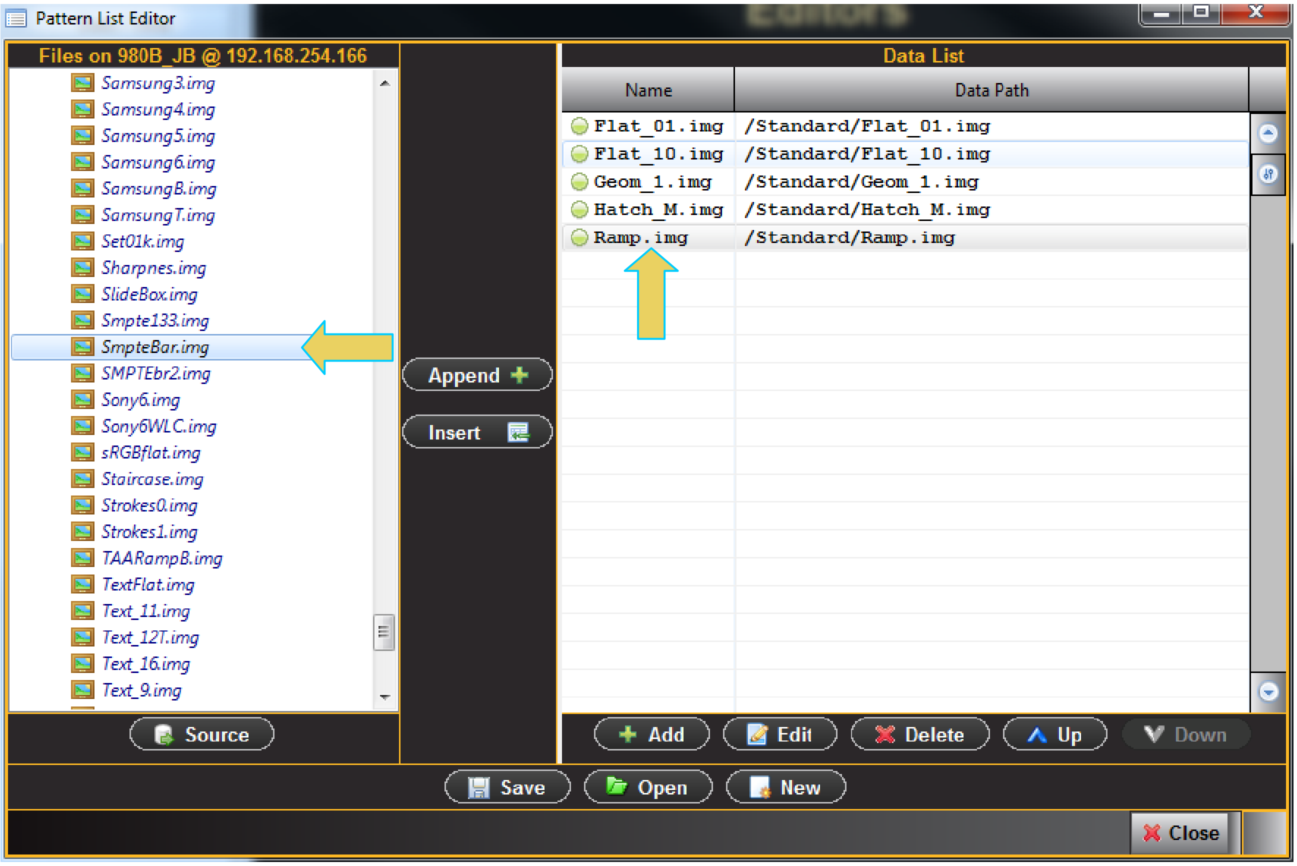


☐ Use Local Files

4. Click **OK** to continue.

   The left side window of the **Pattern List Editor** will display the files on the 980 DP Video Generator module in the Standard directory. The panel on the right (**Data List**) is a list of test patterns in your custom list.


Pattern List Editor
Files on 980_Gen @ 192.168.254.175
Standard
3DBoxes.img
3DClrRmp.img
3DXTalk.img
3DXTalk2.img
Acer1.img
Acer2.img
Acer3.img
Acer4.img
Acer5.img
Acer6.img
Acer7.img
Acer8.img
Acer9.img
AFDTest.img
Anamorph.img
ANSIgray.img
AnsiLght.img
Apple1.img
AudioLR.img
AudioLRf.img
AudioRAT.img
Source
Append
Insert
Data List
Name
Data Path
Add
Edit
Delete
Up
Down
Save
Open
New
Close



Samsung3.img
Samsung4.img
Samsung5.img
Samsung6.img
SamsungB.img
SamsungT.img
Set01k.img
Sharpnes.img
SlideBox.img
Smpte133.img
SmpteBar.img
SMPTEbr2.img
Sony6.img
Sony6WLC.img
sRGBflat.img
Staircase.img
Strokes0.img
Strokes1.img
TAARampB.img
TextFlat.img
Text_11.img
Text_12T.img
Text_16.img
Text_9.img

Name	Data Path
Flat_01.img	/Standard/Flat_01.img
Flat_10.img	/Standard/Flat_10.img
Geom_1.img	/Standard/Geom_1.img
Hatch_M.img	/Standard/Hatch_M.img
Ramp.img	/Standard/Ramp.img

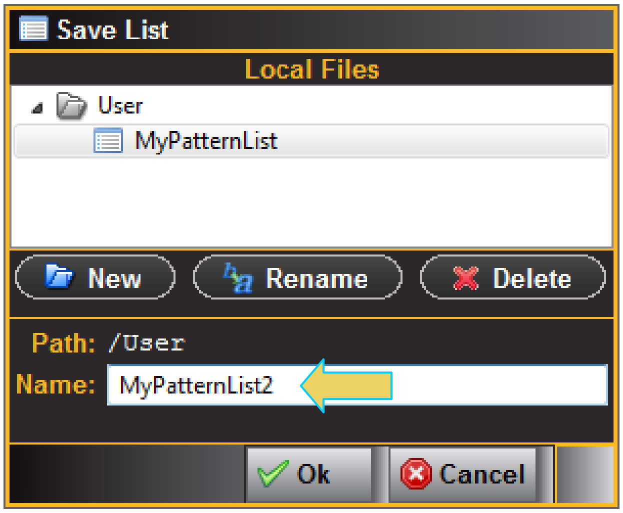
There are three buttons in the middle between the two windows that enable you to configure the test patterns in your Pattern List. These are defined as follows:

Append – Add a new test pattern to the end of your list.

Insert – Insert a new test pattern into your accumulating list above the test pattern that is highlighted in the Data List on the right.

Delete – Delete or remove a test pattern from your list.

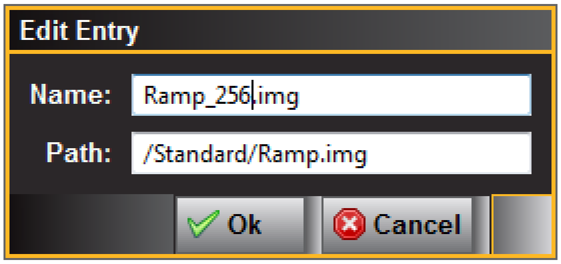
5. Click on the **Save** activation button when you are done configuring your custom list. You will be asked to enter a name for your new Pattern List. Use the **Name** field provided (below).



Path: /User

Name: MyPatternList2

6. Click on the pattern name if you wish to rename it.



Name: Ramp_256.img

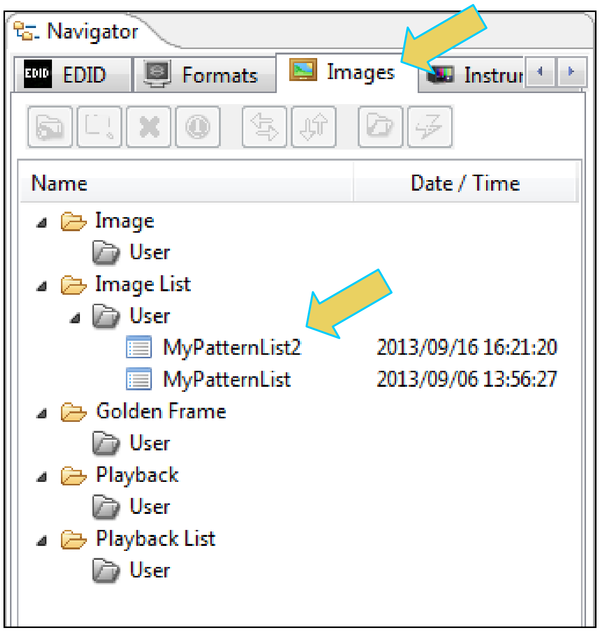
Path: /Standard/Ramp.img

9.2 Applying a custom Pattern List

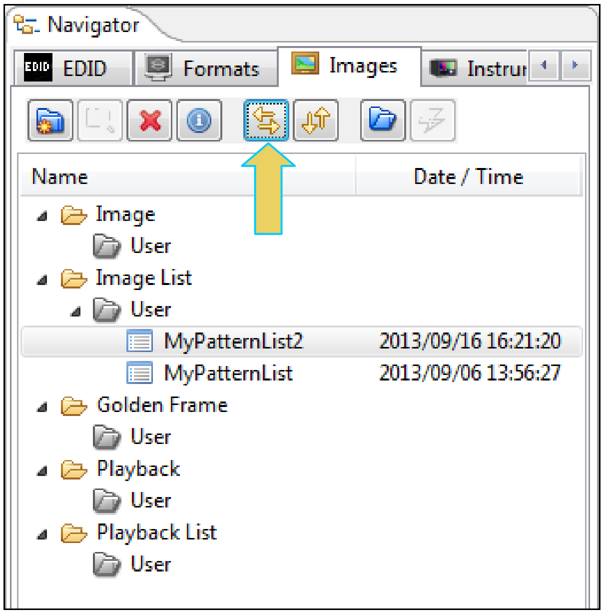
This subsection describes how you can apply a custom pattern list that you have created. Often you will have created the pattern list on your host PC but you may wish to apply it on the 980 instrument itself. In order to do this you will have to transfer the pattern list from your host PC to the 980/980B prior to using it. The procedure below describes these steps.

To apply an existing Pattern List:

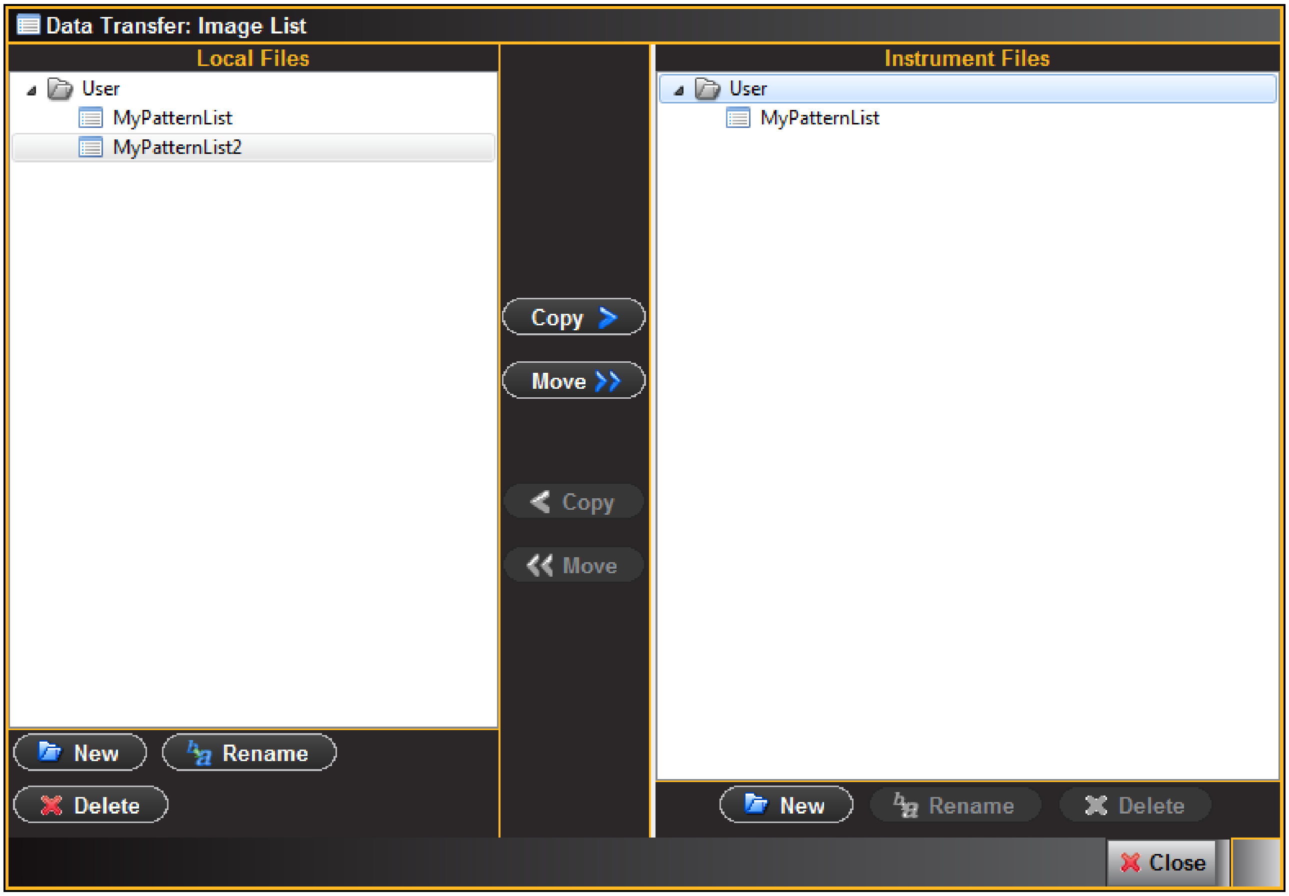
1. Navigate to the Navigate/Images tab.



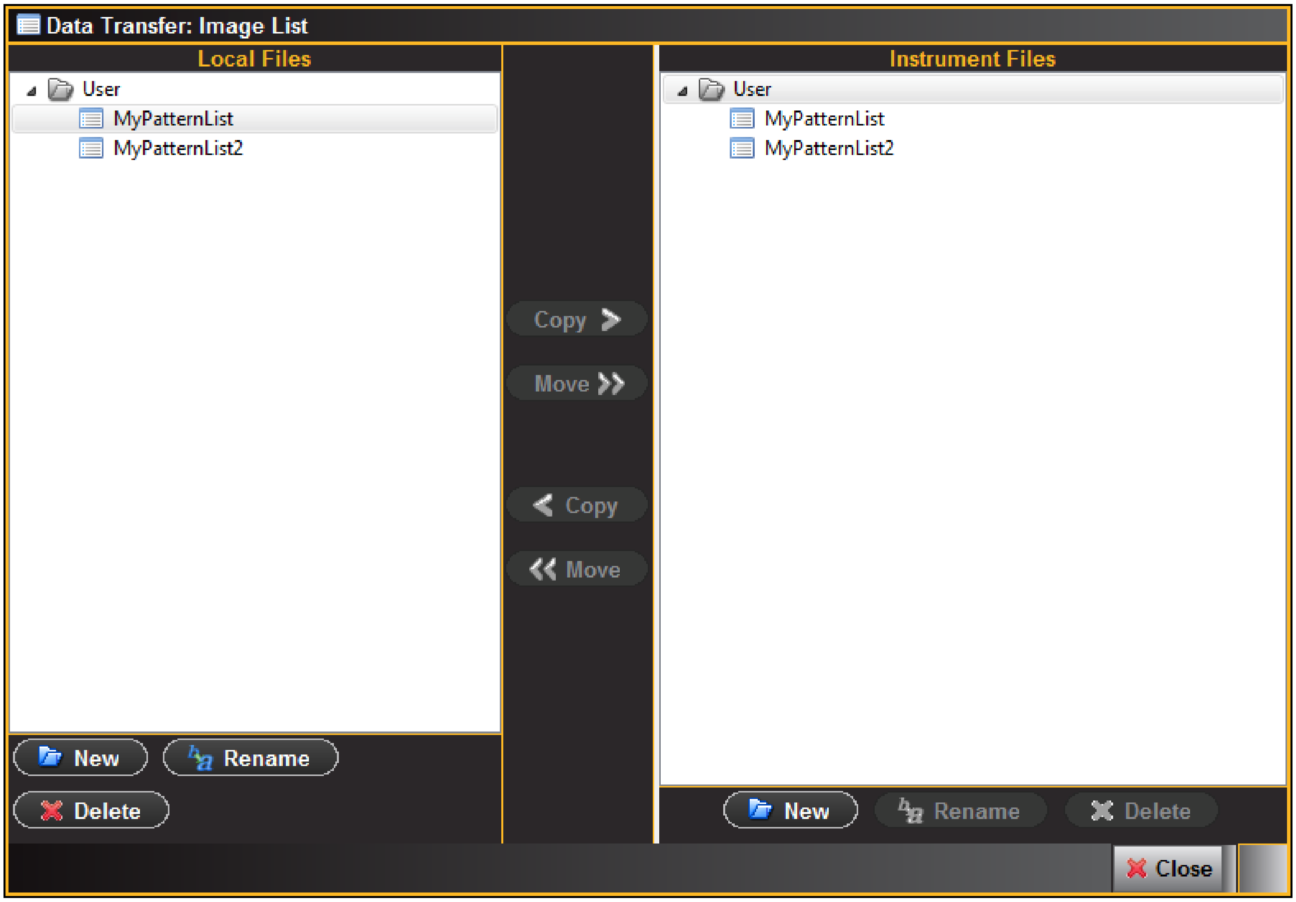
2. Transfer the Pattern List from your Host PC to the 980/980B by invoking the transfer icon indicated below.



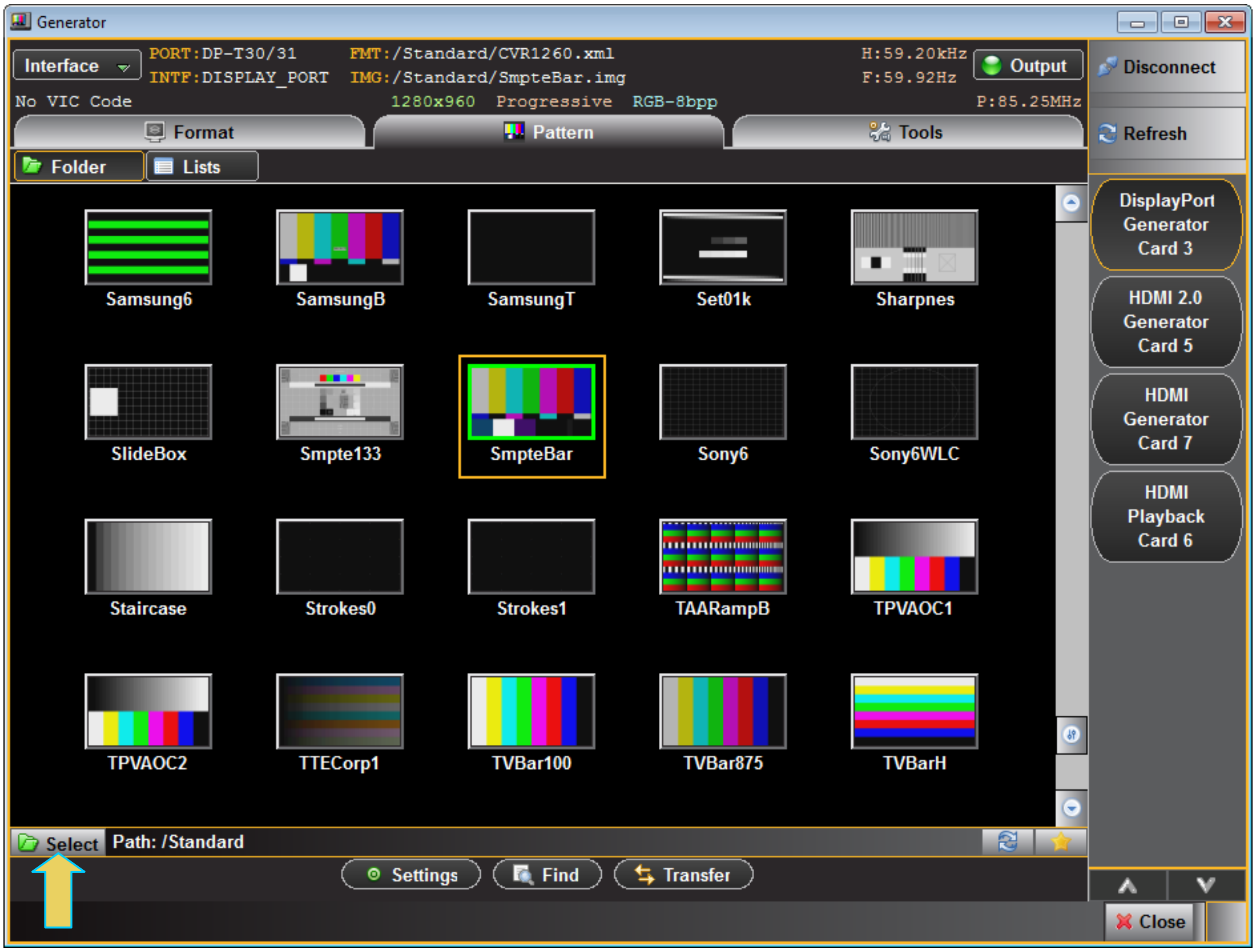
The File Transfer panel appears as shown below:



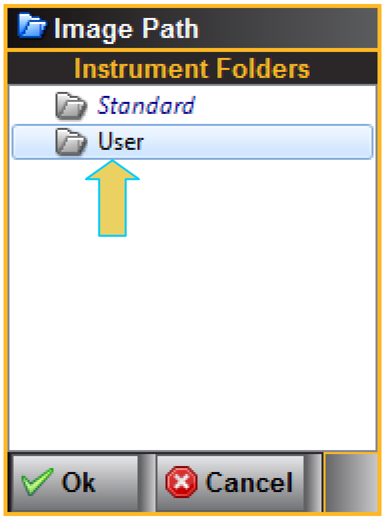
3. Transfer the Pattern list from the Local Files on the left side to the Instrument files using the Copy or Move button. Note that you will have to highlight a directory on the Instrument Files panel in order to enable the Copy or Move button. In this case since you are using the external 980 GUI Manager, the “Local Files” are the files stored on the Host PC. The following screen shows the result:


Data Transfer: Image List
Local Files
User
MyPatternList
MyPatternList2
Copy
Move
Copy
Move
Instrument Files
User
MyPatternList
MyPatternList2
New
Rename
Delete
New
Rename
Delete
Close

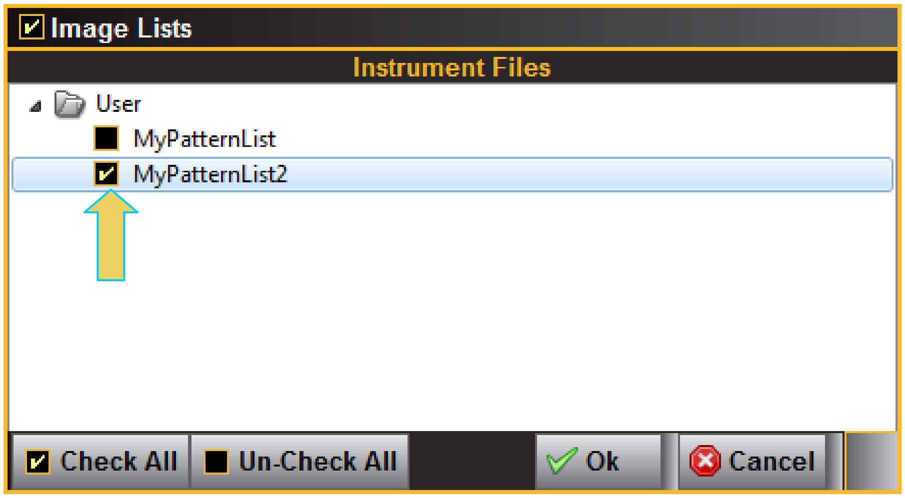
4. Navigate to the **Pattern** Tab on the Generator panel and select your list using the Pattern List icon on the bottom status panel as shown below.



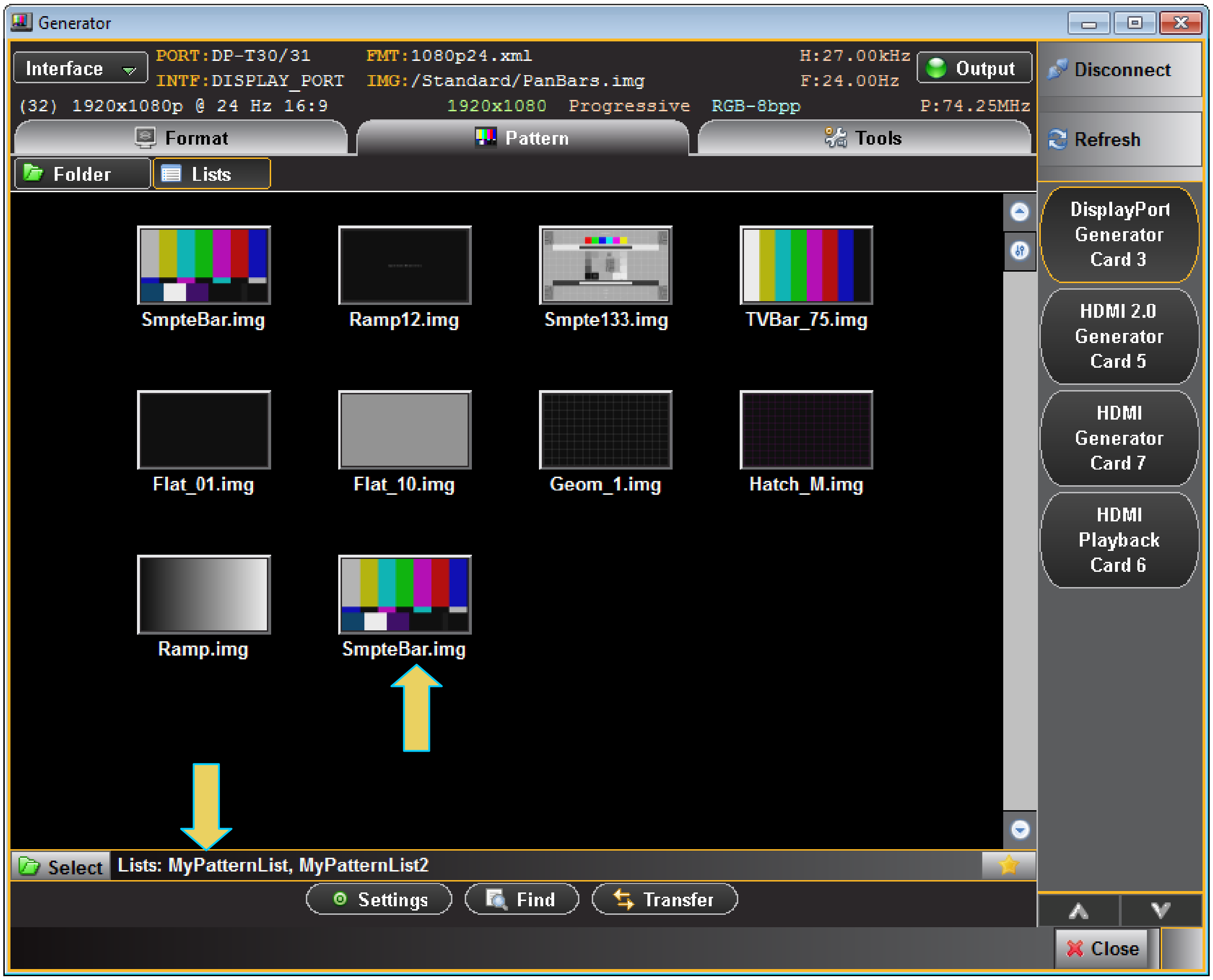
The Pattern Lists dialog box will appear as shown below.



5. Select the Pattern Lists icon and then the desired Pattern List as shown below:


☑ Image Lists
Instrument Files
User
☐ MyPatternList
☑ MyPatternList2
☑ Check All
☐ Un-Check All
Ok
Cancel

The result is that there will be a restricted list of test patterns available and display in the **Pattern** tab window (below). The Path icon on the bottom status panel will display that new list.



PORT:DP-T30/31 FMT:1080p24.xml H:27.00kHz
INTF:DISPLAY_PORT IMG:/Standard/PanBars.img F:24.00Hz
(32) 1920x1080p @ 24 Hz 16:9 1920x1080 Progressive RGB-8bpp P:74.25MHz

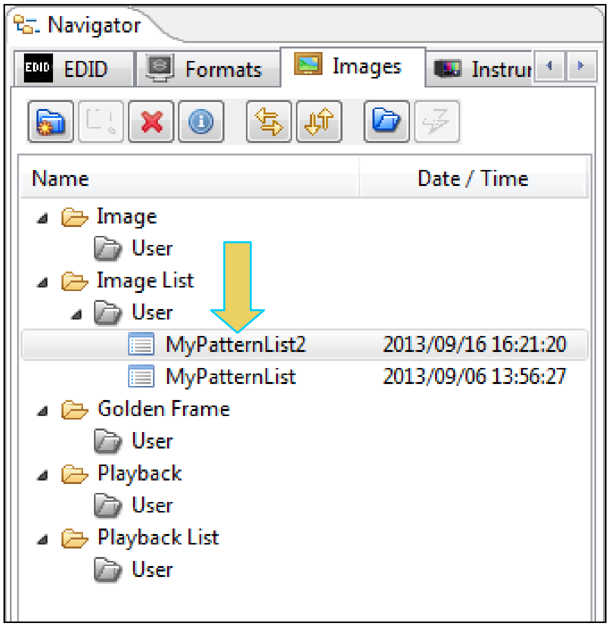
Lists: MyPatternList, MyPatternList2

9.3 Viewing a custom Pattern List

This subsection describes how you can view a custom pattern list that you have created.

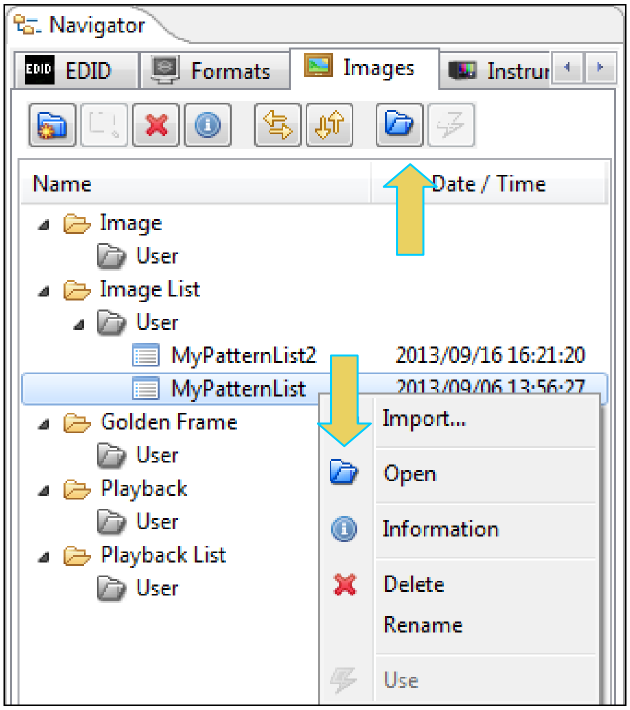
To view an existing Pattern List:

1. View the new Image List through the **Navigator** panel. Select the Pattern List folder.

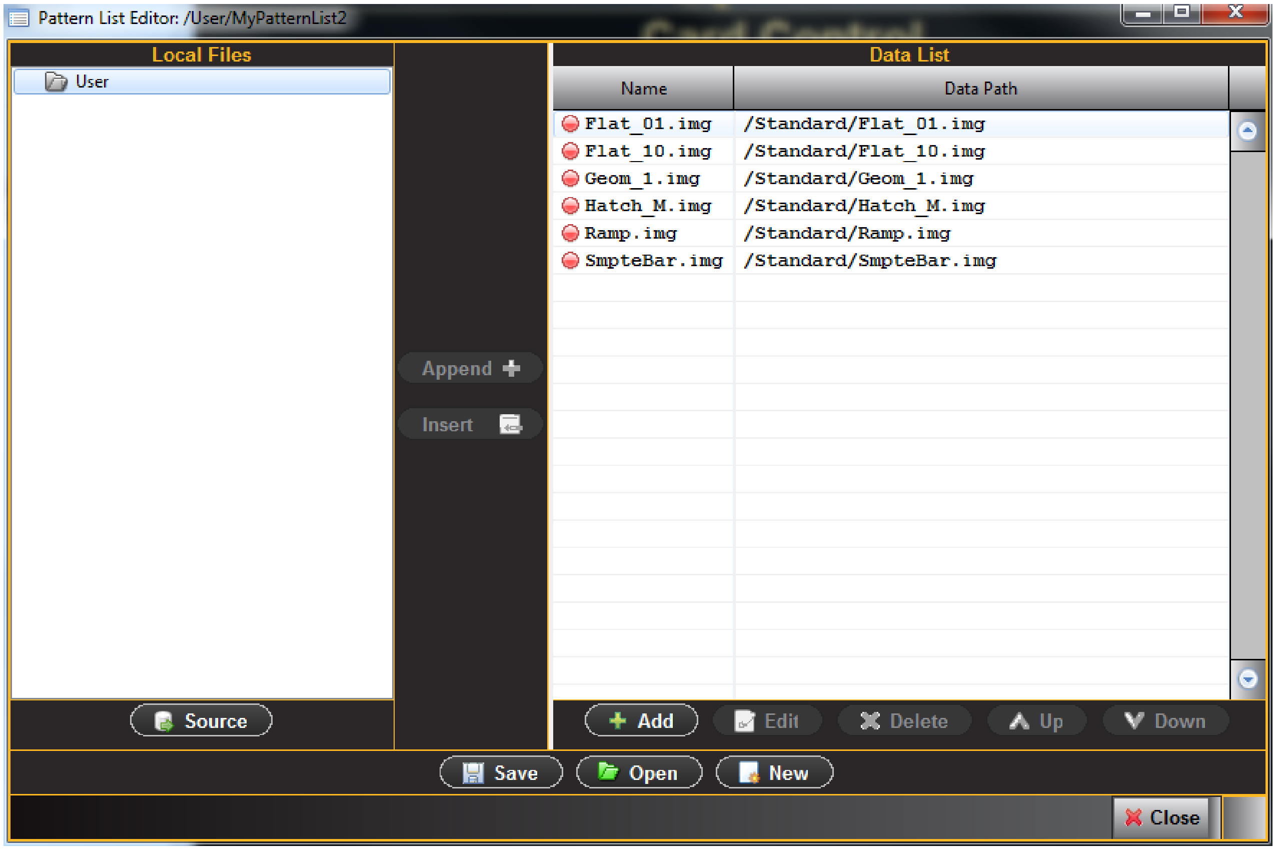


2. The new Pattern List will appear under User in the Local Files panel as shown above.

3. Right click on the desired pattern list or select the Open icon to open up the viewing window. Refer to the screen example below:



The Pattern List will appear in the panel as shown below:



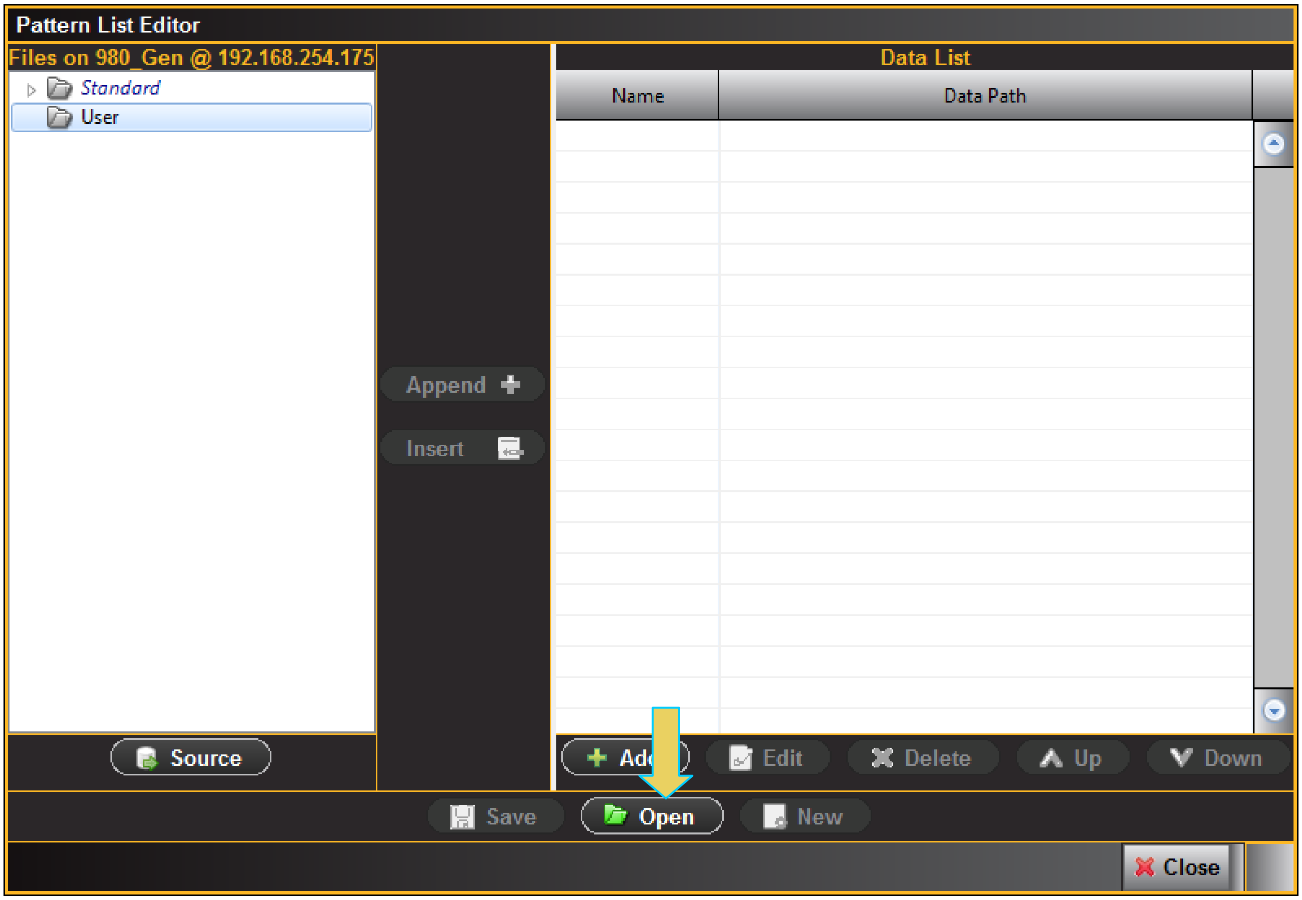
Name	Data Path
Flat_01.img	/Standard/Flat_01.img
Flat_10.img	/Standard/Flat_10.img
Geom_1.img	/Standard/Geom_1.img
Hatch_M.img	/Standard/Hatch_M.img
Ramp.img	/Standard/Ramp.img
SmpteBar.img	/Standard/SmpteBar.img

9.4 Opening a custom Patten List from the Pattern List Editor

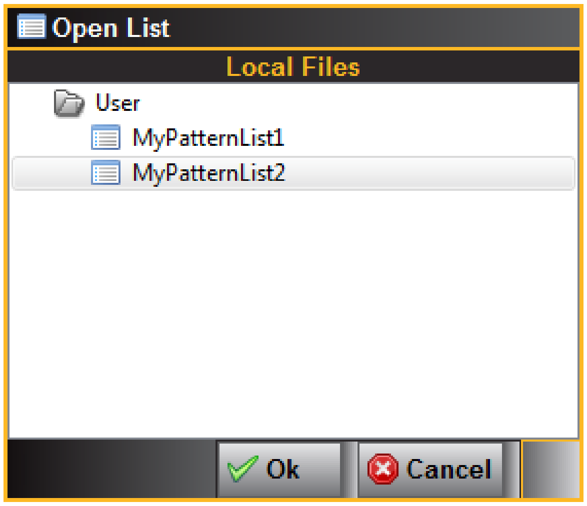
This subsection describes how you can open a custom pattern list that you have created in the Pattern List Editor.

To open an existing Pattern List:

1. Click on the **Open** activation button on the lower panel of the **Pattern List Editor** window.

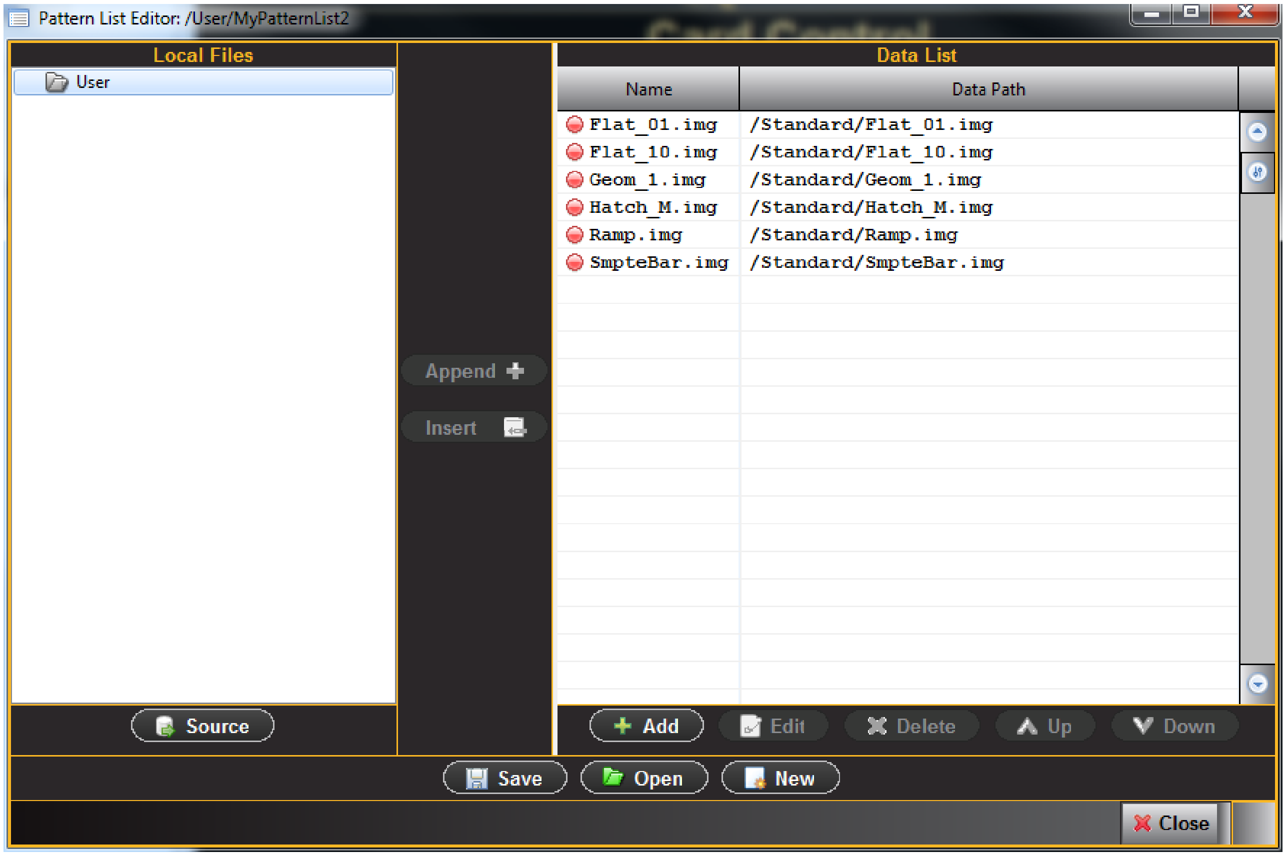


The **Open List** dialog box appears enabling you to select a Pattern List (below).



2. Select the list you wish to open (only one list is shown in the **Open List** dialog box example above). The Pattern List will appear in the Pattern List Editor window as shown below.

   You can now edit the list as desired using the same techniques that you used to create the list.



Name	Data Path
Flat_01.img	/Standard/Flat_01.img
Flat_10.img	/Standard/Flat_10.img
Geom_1.img	/Standard/Geom_1.img
Hatch_M.img	/Standard/Hatch_M.img
Ramp.img	/Standard/Ramp.img
SmpteBar.img	/Standard/SmpteBar.img

10 Format List Editor

Use the following procedures to create a custom format list. The **Format List Editor** can be used either on the embedded 980 GUI Manager or the external 980 GUI Manager. The examples in this procedure use the external 980 GUI Manager

10.1 Opening a custom Format List

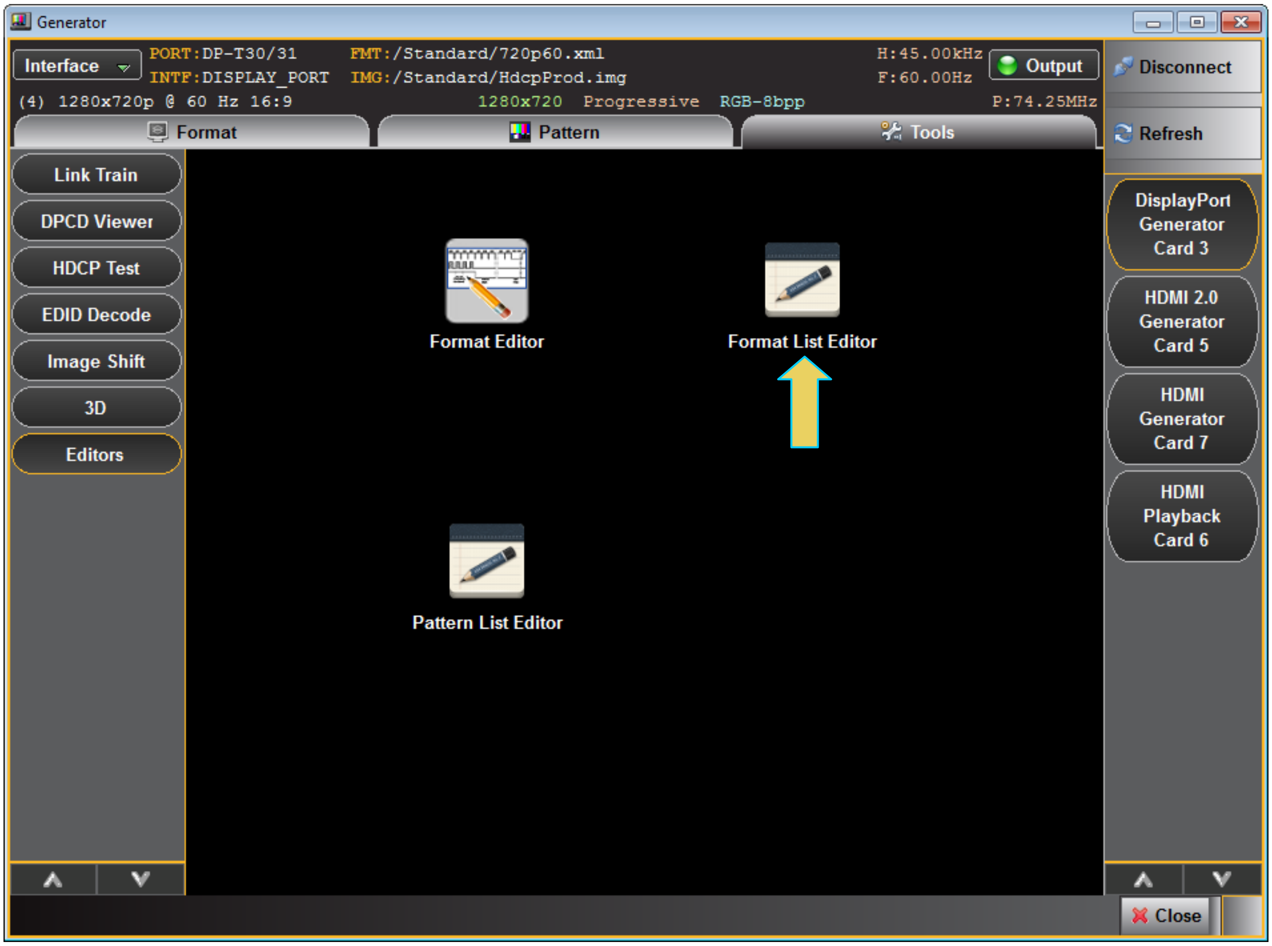
This subsection describes how you can create a custom format list.

To create a custom list of test patterns:

1. From the Editors Page of the Apps panel, select **Format List Editor** from the **View** menu as shown below.

Alternatively, if you are using the embedded 980 GUI Manager you can access the **Format List Editor** from the **Generator Tools tab**. Be sure to select the correct Transmitter on the right side.

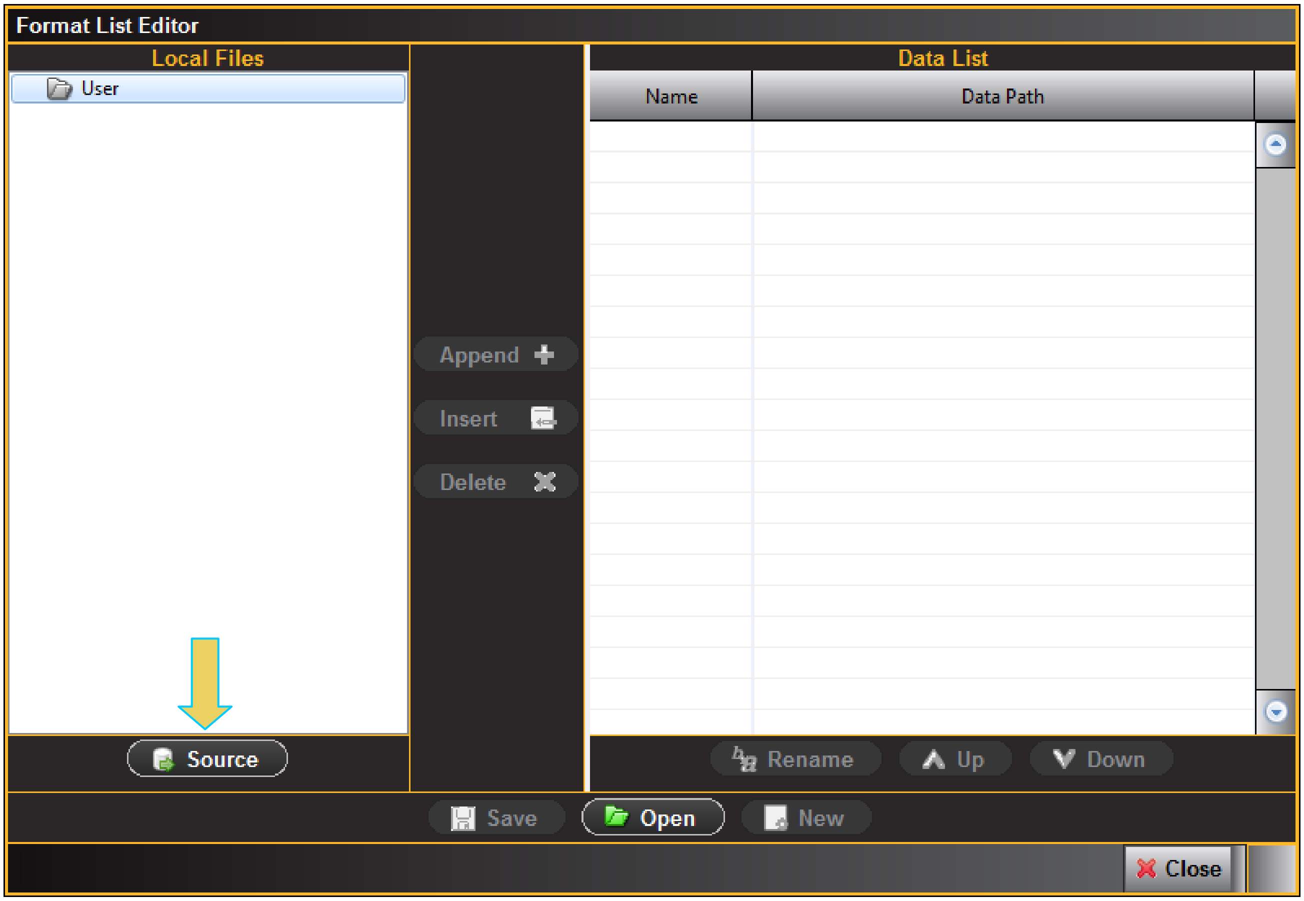
The list of editors appears as shown in the screen below.



PORT:DP-T30/31 FMT:/Standard/720p60.xml H:45.00kHz
INTF:DISPLAY_PORT IMG:/Standard/HdcpProd.img F:60.00Hz
(4) 1280x720p @ 60 Hz 16:9 1280x720 Progressive RGB-8bpp P:74.25MHz

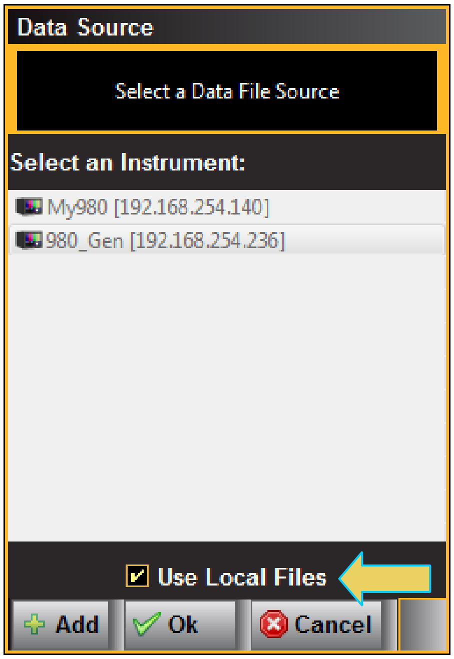
1. Select the Format Editor icon.

The **Format List Editor** appears as shown below:



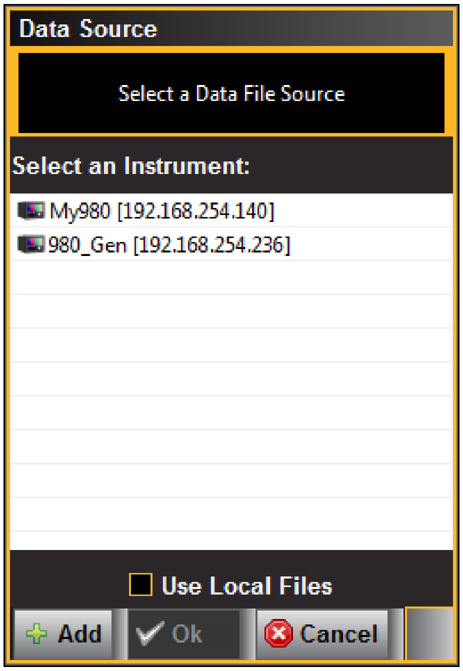
2. Click on the **Source** button on the lower left under Local Files (indicated in the diagram above). The Data **Source** dialog box will appear enabling you to select between using files on your PC or using files on the 980 DP Video Generator module to create your custom list. This dialog box also enables you to select the particular 980B (if there are more than one on the network). (You can also add a new 980 through this dialog box.)

Note: "Local Files" when using the external 980 GUI Manager means that you are using the files stored locally on your host PC. If you deselect Local Files on the dialog box below you are viewing files on the 980B file system.



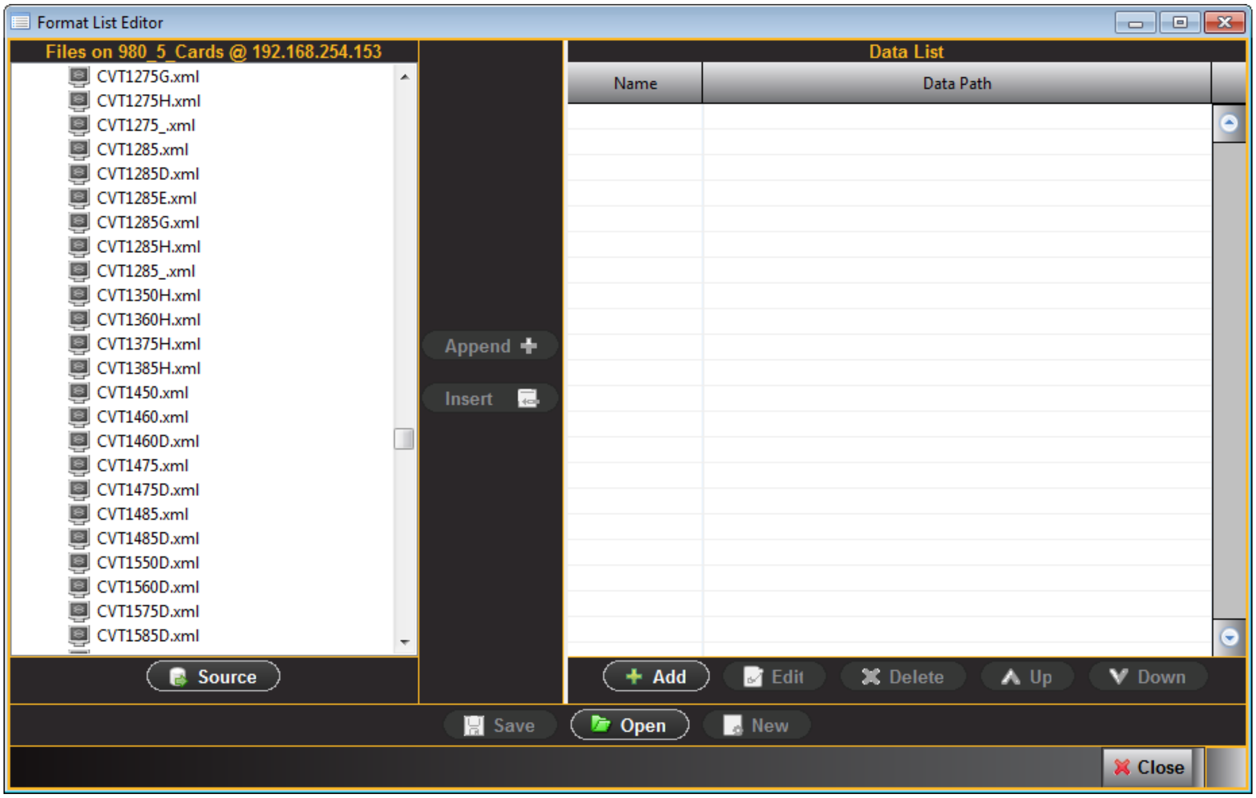
3. Select the instrument that you want to use as the source of your formats. (If there are multiple 980s on the network you will have to choose which one.) Note that if you are using the **Format List Editor** on the external 980 GUI Manager, the custom Format List is stored on the host PC not the 980 instrument itself.

   Note that you will have to deselect **Use Local Files** in order to select a 980B. If you do not de-select **Use Local Files**, then you will be using formats on your host PC to create your list.



4. Click **OK** to continue.

   The left side window of the **Format List Editor** will display the files on the 980 DP Video Generator module in the Standard directory. The panel on the right (**Data List**) is a list of formats in your custom list.



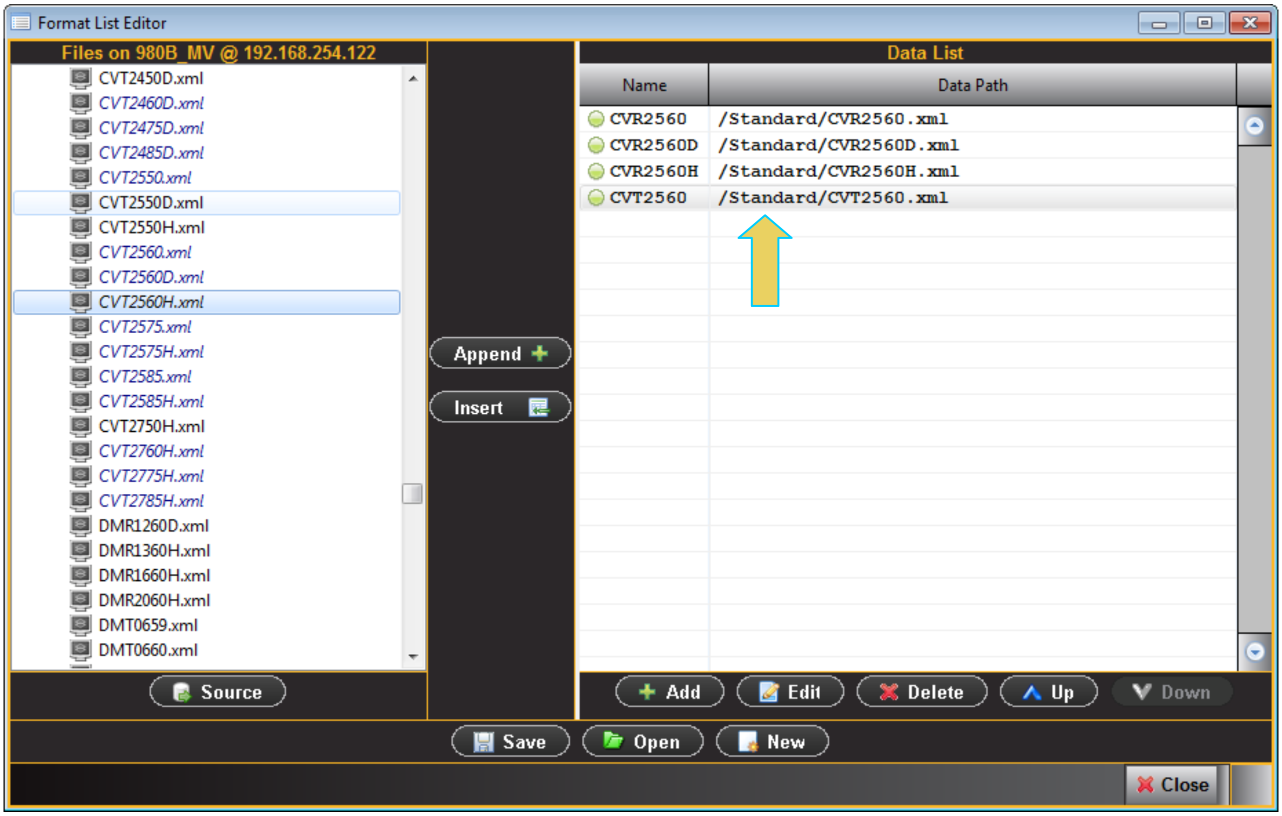
5. Select formats from the left side panel (Files on 980) and Append or Insert them to your Format List. They will accumulate on the Data List panel on the right side of the Format List Editor window.

   There are three buttons in the middle between the two panels that enable you to configure the formats in your Format List. These are defined as follows:

   Append – Add a new format to the end of your list.

   Insert – Insert a new format into your accumulating list above the test pattern that is highlighted in the Data List on the right.

   Delete – Delete or remove a format from your list.

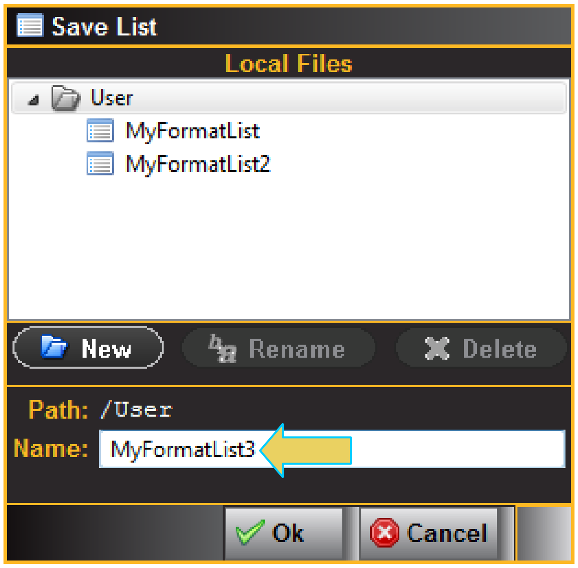


CVT2450D.xml
CVT2460D.xml
CVT2475D.xml
CVT2485D.xml
CVT2550.xml
CVT2550D.xml
CVT2550H.xml
CVT2560.xml
CVT2560D.xml
CVT2560H.xml
CVT2575.xml
CVT2575H.xml
CVT2585.xml
CVT2585H.xml
CVT2750H.xml
CVT2760H.xml
CVT2775H.xml
CVT2785H.xml
DMR1260D.xml
DMR1360H.xml
DMR1660H.xml
DMR2060H.xml
DMT0659.xml
DMT0660.xml

Name	Data Path
CVR2560	/Standard/CVR2560.xml
CVR2560D	/Standard/CVR2560D.xml
CVR2560H	/Standard/CVR2560H.xml
CVT2560	/Standard/CVT2560.xml

Note: The formats listed in blue are formats that are in the EDID of the connected display.

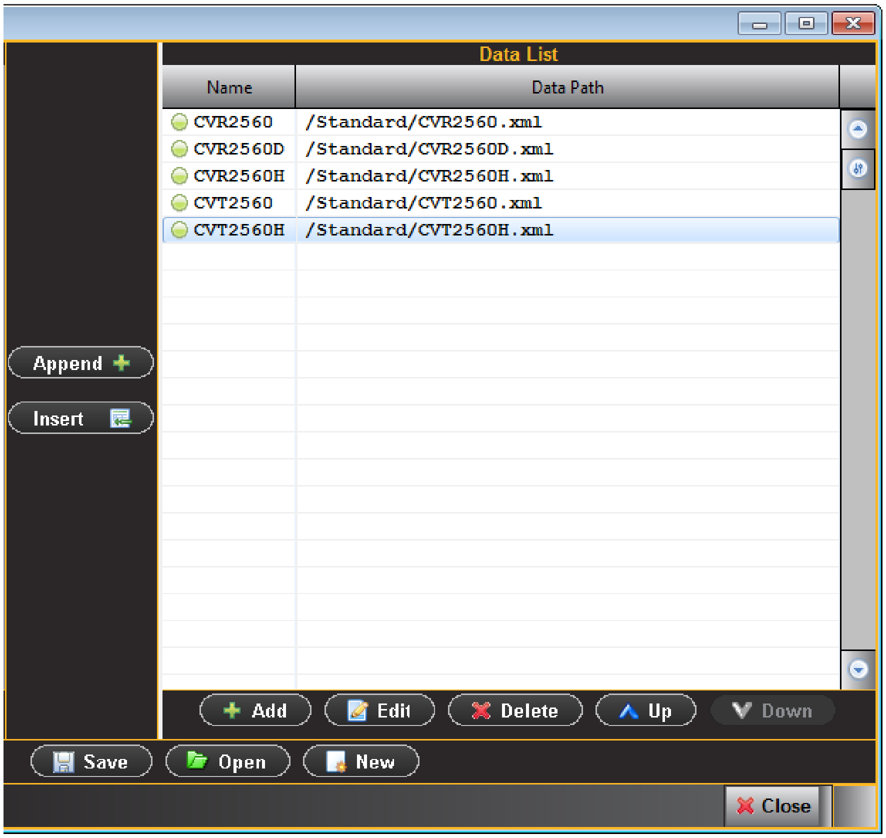
6. Click on the **Save** activation button when you are done configuring your custom list. You will be asked to enter a name for your new Format List. Use the **Name** field provided (below).



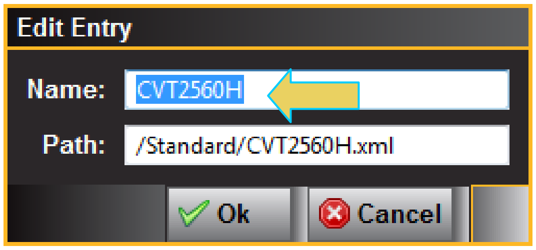
User
MyFormatList
MyFormatList2

Path: /User
Name: MyFormatList3

7. Click on any format if you wish to rename it for convenience.



Name	Data Path
CVR2560	/Standard/CVR2560.xml
CVR2560D	/Standard/CVR2560D.xml
CVR2560H	/Standard/CVR2560H.xml
CVT2560	/Standard/CVT2560.xml
CVT2560H	/Standard/CVT2560H.xml



Name: CVT2560H

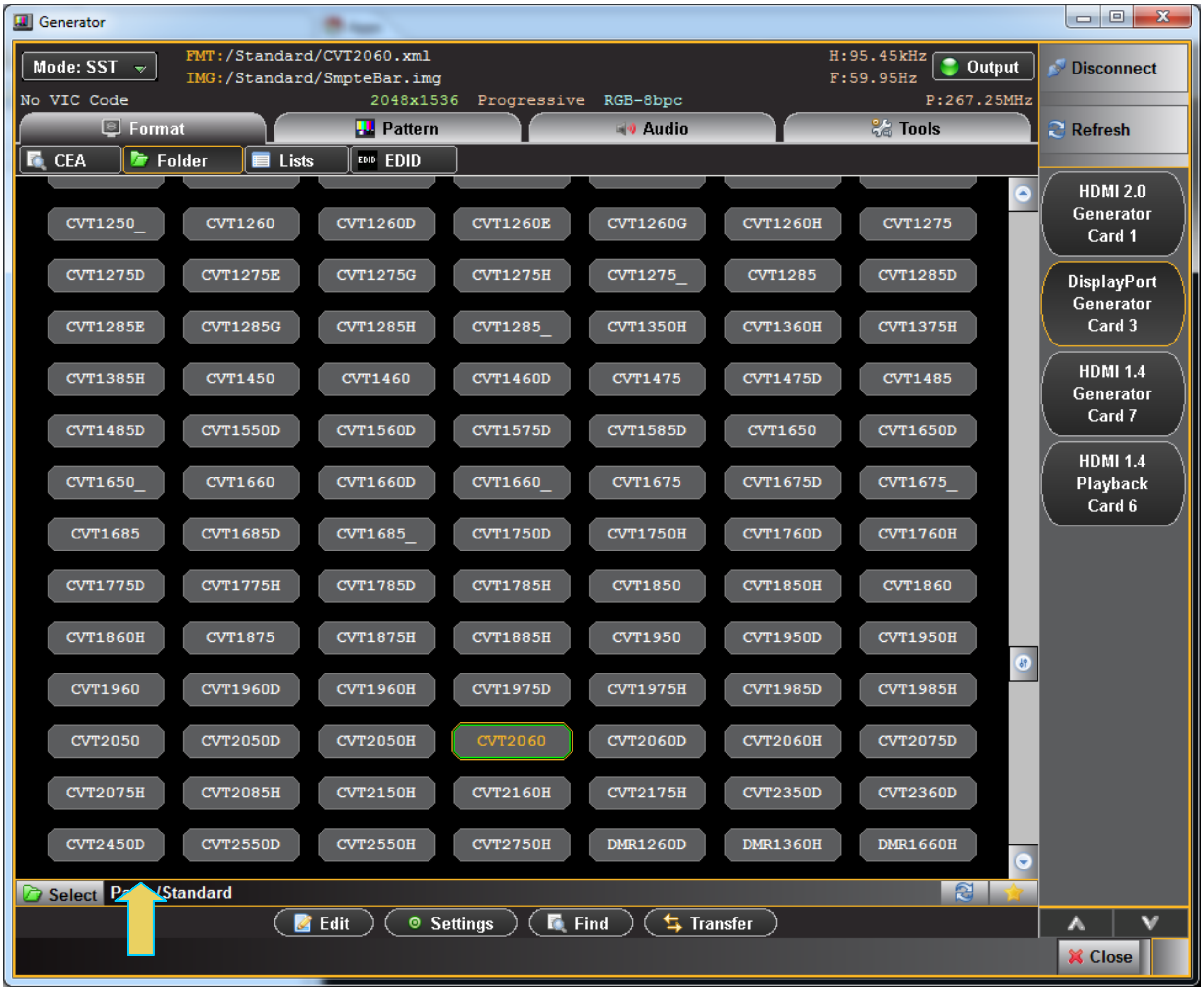
Path: /Standard/CVT2560H.xml

10.2 Applying a custom Format List

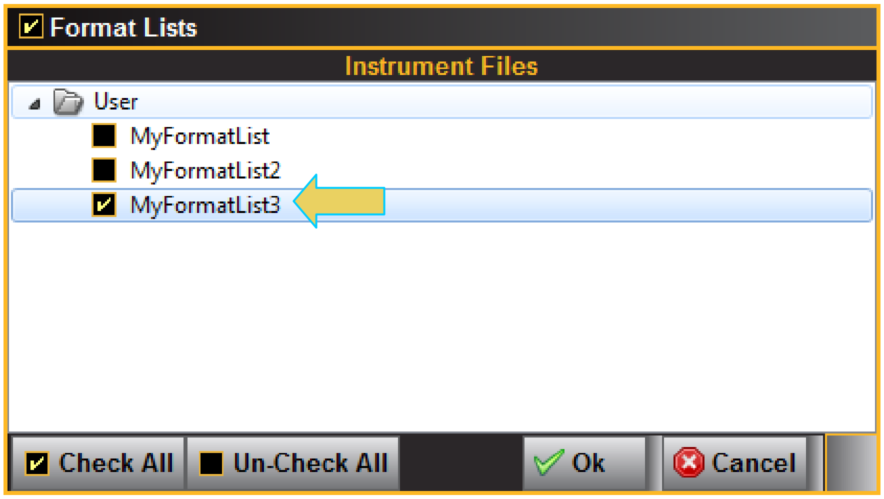
This subsection describes how you can apply a custom format list that you have created.

To apply an existing Format List:

1. Navigate to the **Formats** Tab and select your list using the Format List icon on the bottom status panel as shown below.

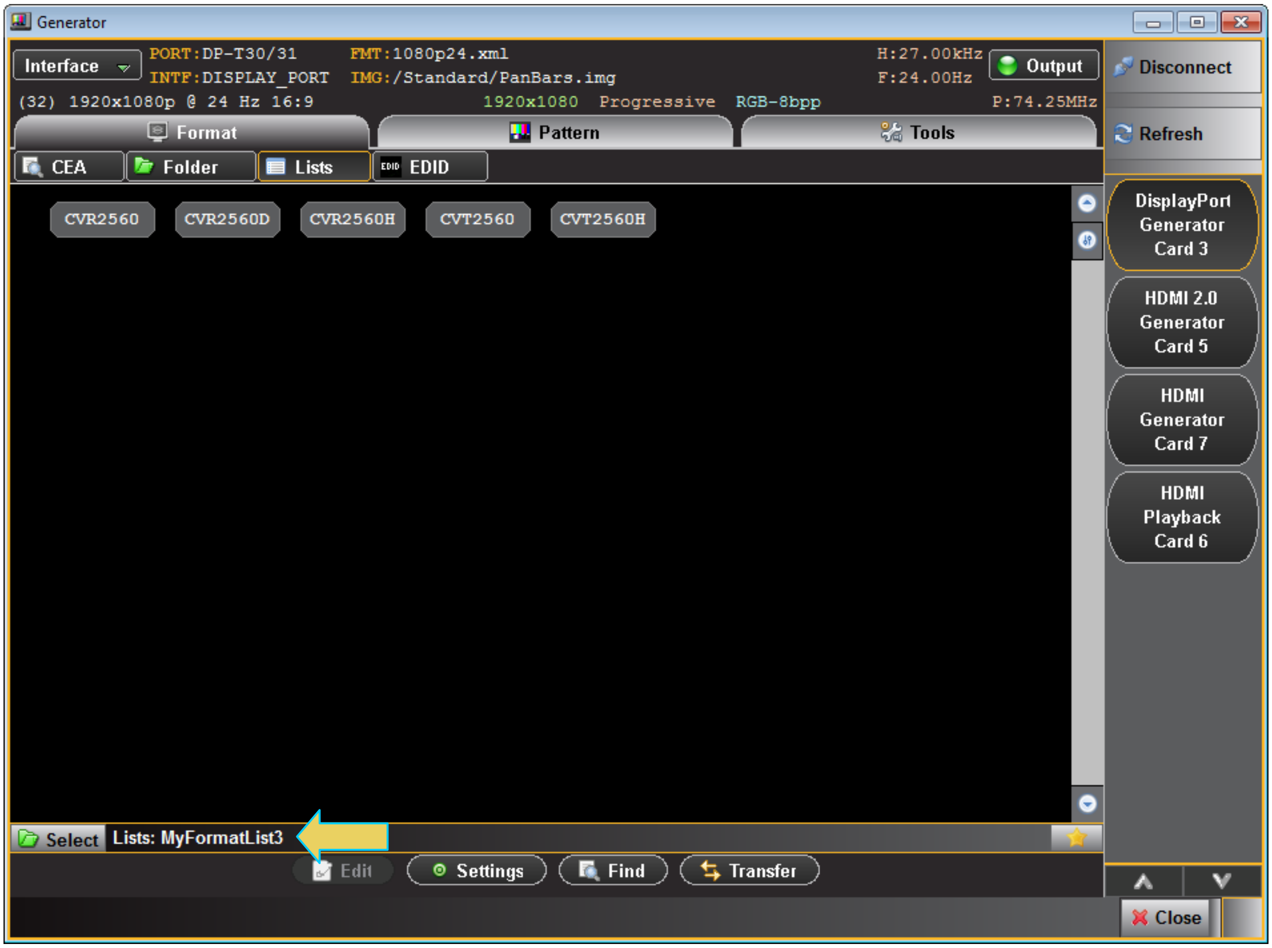


The Format Lists dialog box will appear as shown below.



2. Select the desired format list.

The result is that there will be a restricted list of formats available and display in the **Format** tab window (below). The Path icon on the bottom status panel will display that new list.



PORT:DP-T30/31 FMT:1080p24.xml H:27.00kHz
INTF:DISPLAY_PORT IMG:/Standard/PanBars.img F:24.00Hz
(32) 1920x1080p @ 24 Hz 16:9 1920x1080 Progressive RGB-8bpp P:74.25MHz

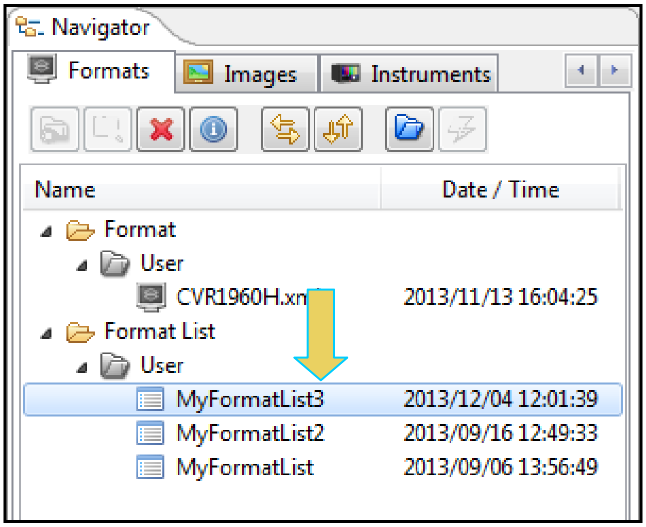
Lists: MyFormatList3

10.3 Viewing a custom Format List

This subsection describes how you can view a custom format list that you have created.

To view an existing Format List:

1. View the new Format List through the **Navigator** panel. Select the Format List folder.



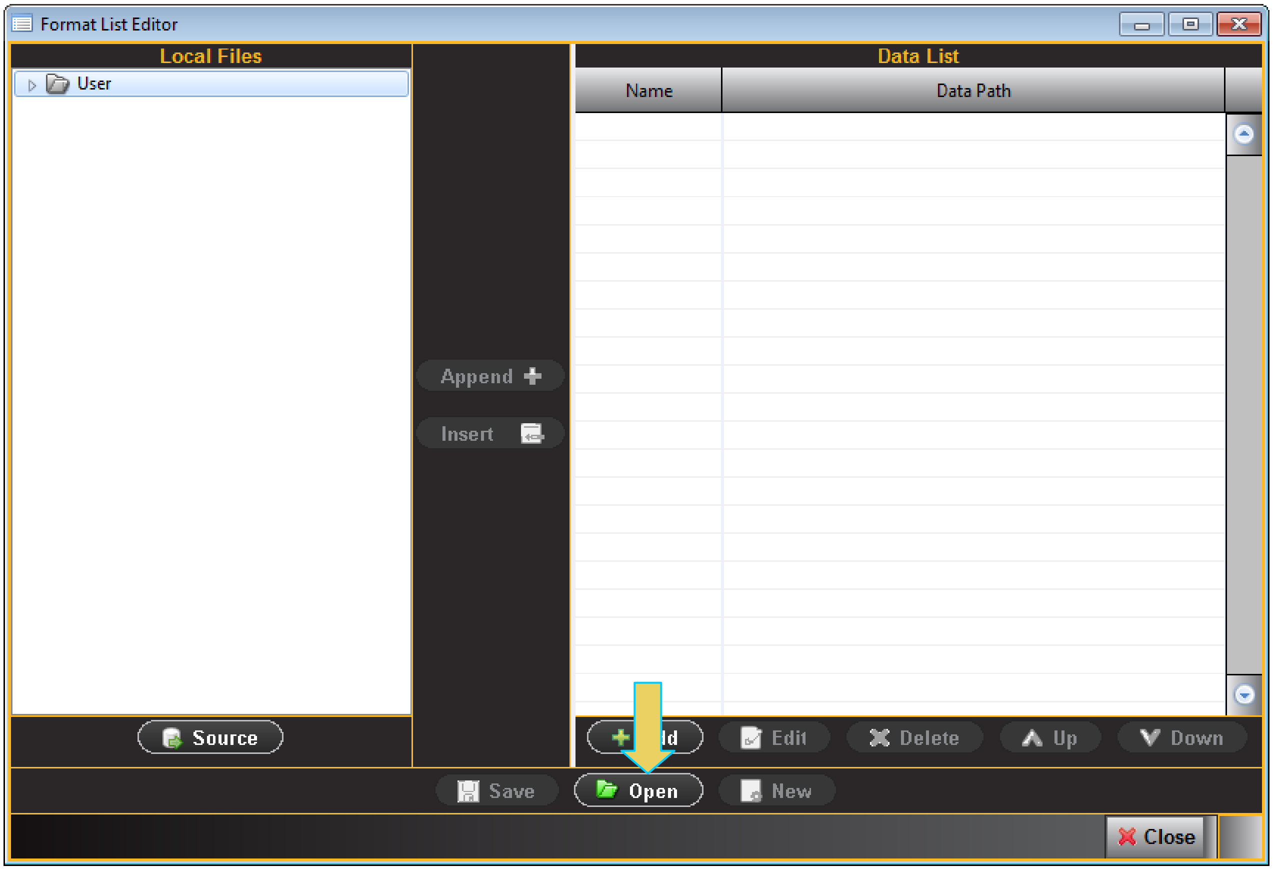
2. The new Format List will appear under User in the Local Files panel as indicated above.

10.4 Opening a custom Format List

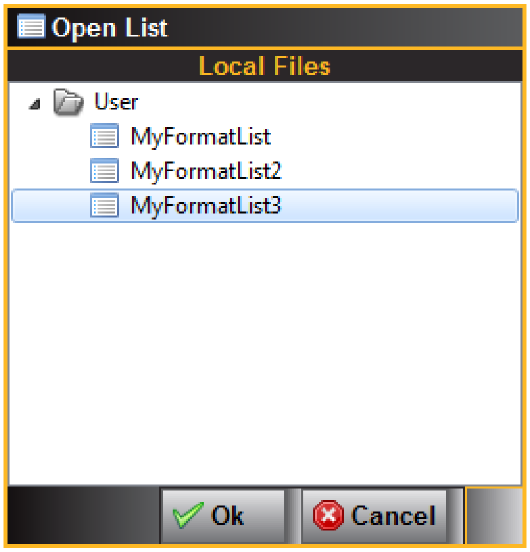
This subsection describes how you can open a custom format list that you have created.

To open an existing Format List for editing:

1. Click on the **Open** activation button on the lower panel of the **Format List Editor** window.

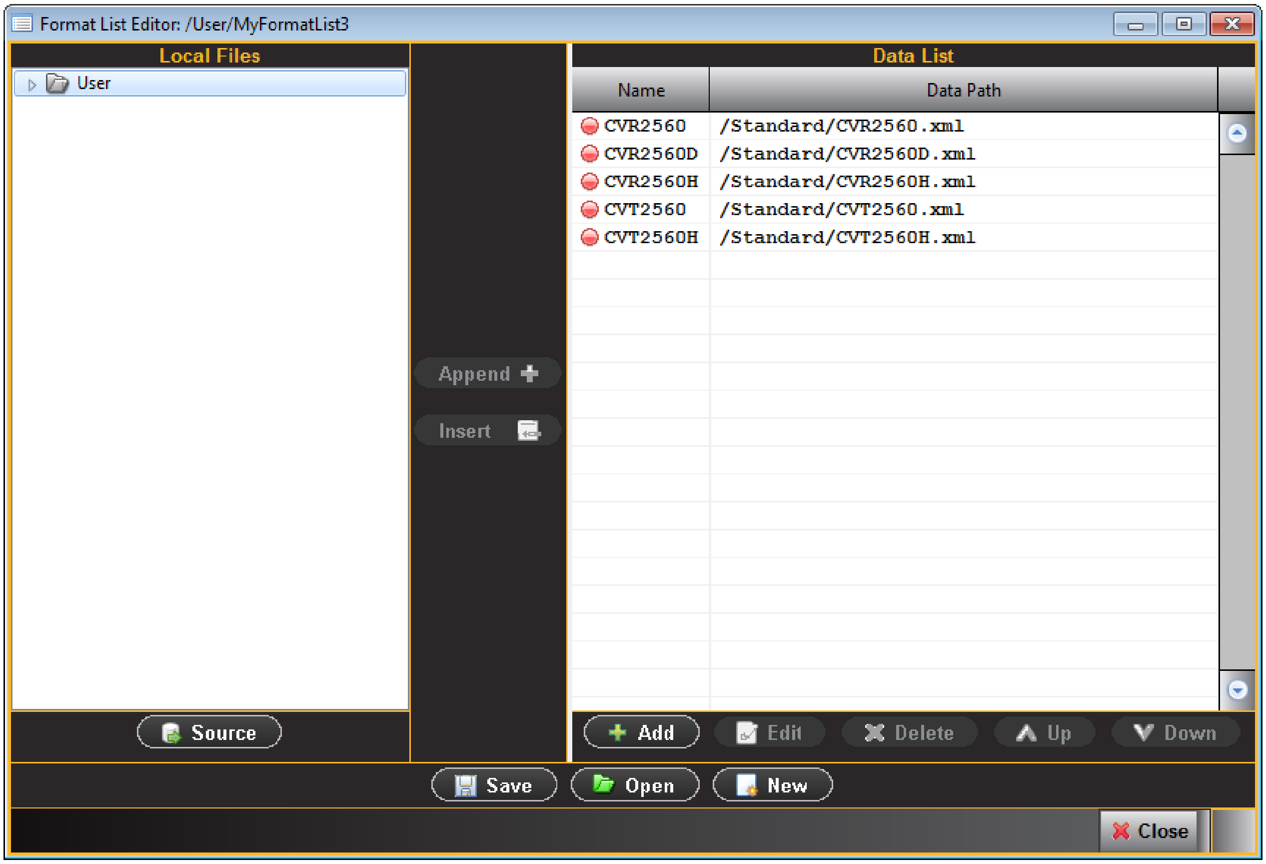


The **Open List** dialog box appears enabling you to select a Format List (below).



2. Select the list you wish to open (only one list is shown in the **Open List** dialog box example above). The Format List will appear in the **Format List Editor** window as shown below.

   You can now edit the list as desired.



Name	Data Path
CVR2560	/Standard/CVR2560.xml
CVR2560D	/Standard/CVR2560D.xml
CVR2560H	/Standard/CVR2560H.xml
CVT2560	/Standard/CVT2560.xml
CVT2560H	/Standard/CVT2560H.xml

11 Format Editor

The **Format Editor** provides a graphical user interface for modifying existing formats, creating custom formats and viewing format parameters. The **Format Editor** can be run on the embedded 980 GUI Manager or on the external 980 GUI Manager.

11.1 Accessing the Format Editor

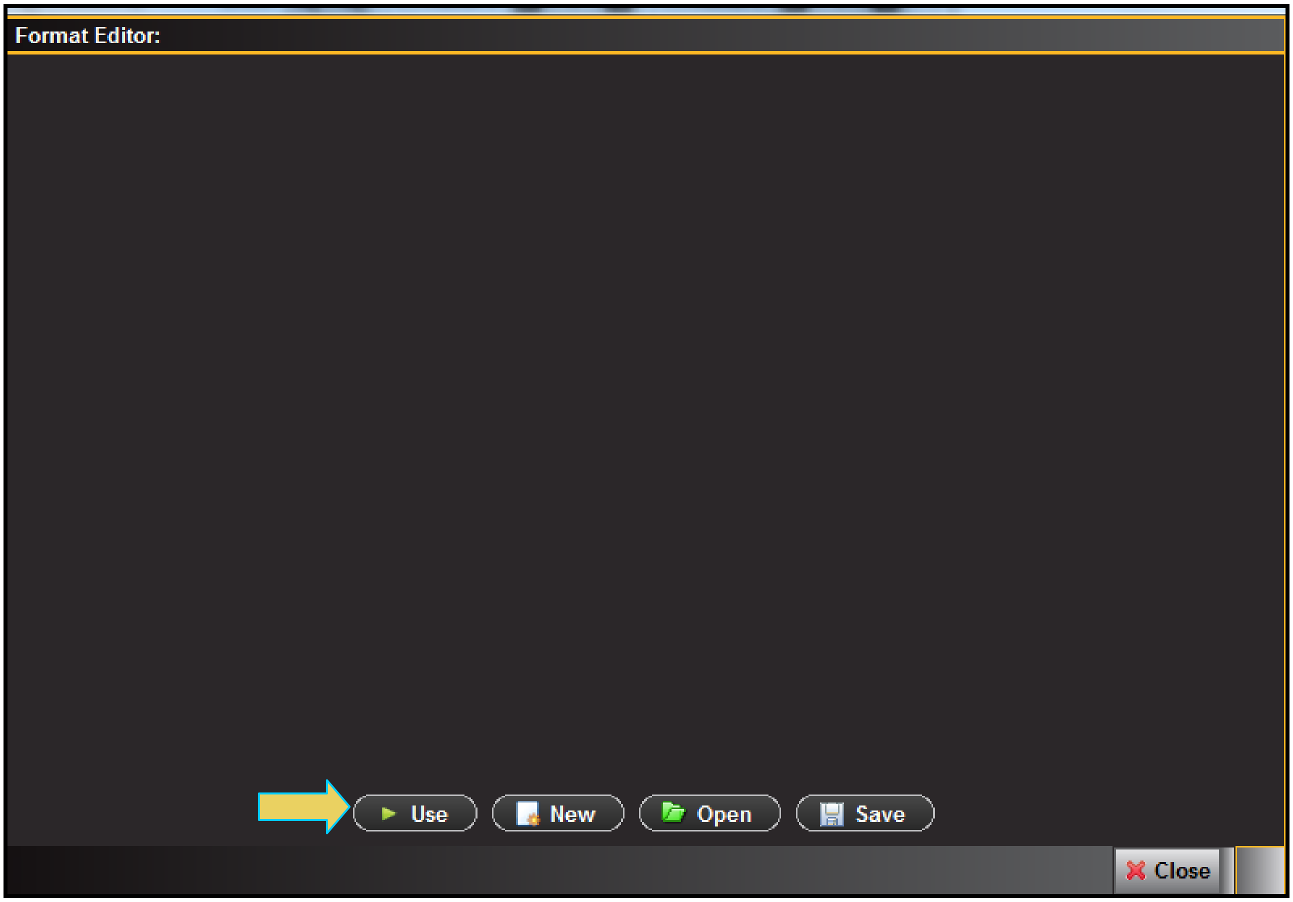
Use the following procedures to access the Format Editor.

To access the Format Editor:

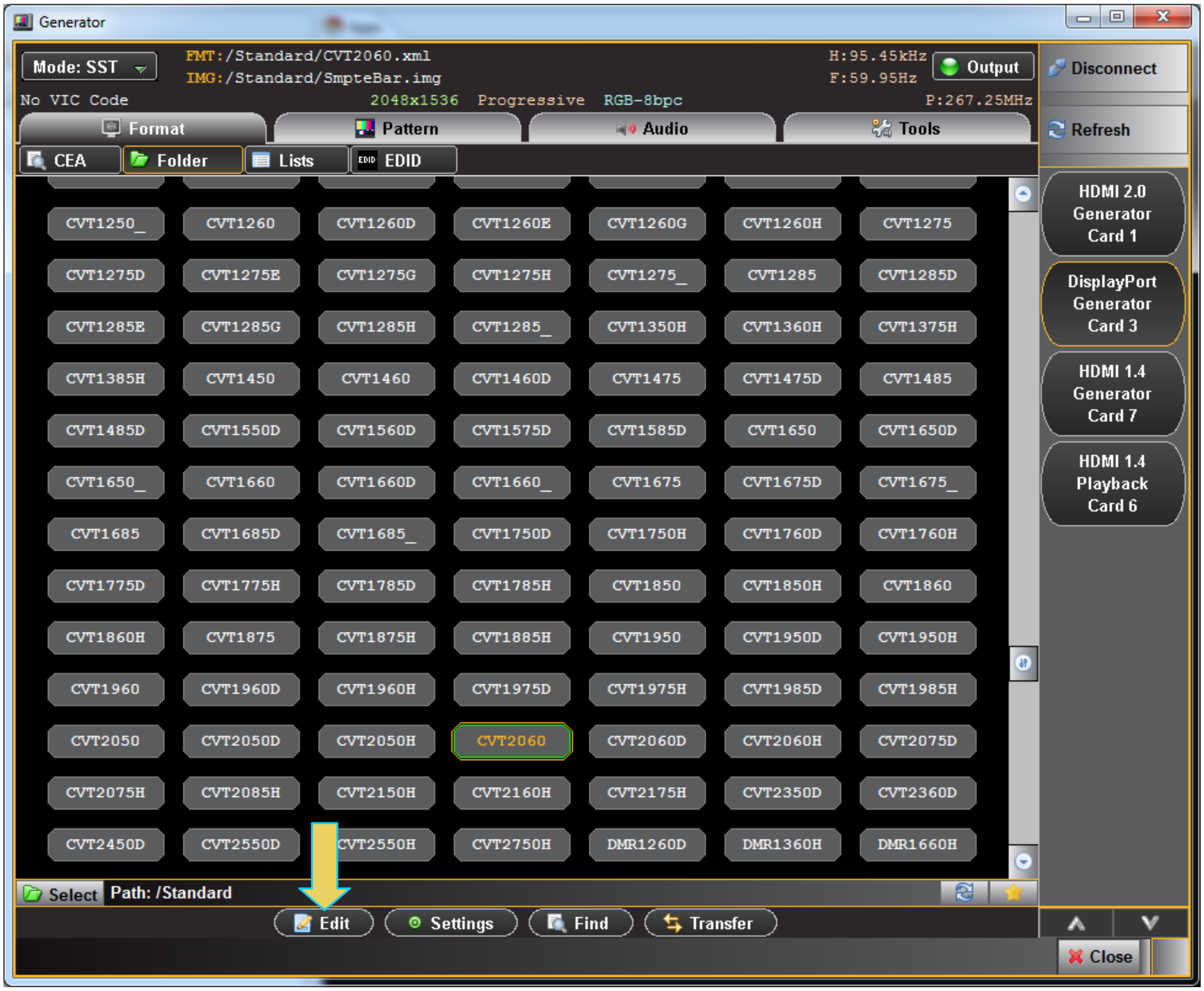
1 Access the **Format Editor** through the **Editors Page** of the **Apps** panel as shown below.

(Optionally) access the **Format Editor** through the **Format** tab using the **Edit** button on the bottom of the window (indicated below).

When you first open the **Format Editor**, the window will be blank as shown below. There are a set of activation buttons on the bottom of the screen that enable you to load, save and create formats.



Please note that you can also invoke the **Format Editor** from the Generator panel's Format tab as shown below.



FMT:/Standard/CVT2060.xml
IMG:/Standard/SmpteBar.img
No VIC Code
2048x1536 Progressive RGB-8bpc
H:95.45kHz
F:59.95Hz
P:267.25MHz
Path: /Standard

In this case the Format Editor is provisioned with the format timing settings of the format that had been selected in the Format tab window. This is shown below.

Format Editor: /qd/genfs/library/hpformats_DP_03/DMT1260G.xml

🟥 Calculated

Pixel Rate 108.000001 MHz 9.259259 ns

	Horizontal		Vertical	
Rate	63.981043 KHz		60.019740 Hz	
	Tune 1.000000 Base 63.981043 KHz			
Active	1280 Pixels	11.851852 us	1024 Lines	16.004741 ms
Blank	408 Pixels	3.777778 us	42 Lines	0.656444 ms
Total	1688 Pixels	15.629630 us	1066 Lines	16.661185 ms
Pulse Delay	48 Pixels	0.444444 us	1 Lines	0.015630 ms
Pulse Width	112 Pixels	1.037037 us	3 Lines	0.046889 ms

Serration width Adjustment 0 Pixels

H to V Pulse Delay 0 Pixels

Horizontal Broad Pulse Delay 0 Pixels

Eq. Before 0 Lines

Eq. After 0 Lines

Entry Units
● Machine
○ Time

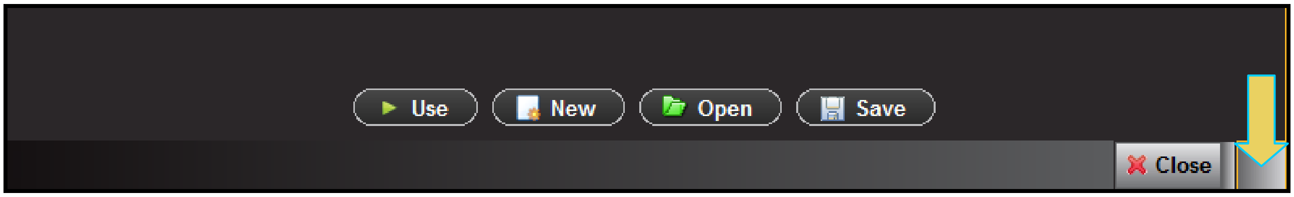
Scan Type
● Progressive
○ Interlace

☐ Back Porch

☐ Clock Pulse
☐ PreEmphasis
☐ DC Balance
☐ Flat Front Porch
☐ TriLevel
☐ Repeat Field

10.1 Format Editor - Basic Window Configuration and Operation

You can resize the window using the square area on the lower right side (indicated below).



10.1.1 Format Editor – Lower Activation Buttons

The following table describes the **Format Editor** menu buttons.

Button	Description
Use	Activates the custom format you create.
New Format	Opens up the New Format at the Timing tab. Enables you to create new formats. This is equivalent to selecting the **New Format** from the **File** menu.
Open	Enables you to browse to and open an xml format file on your PC. This is equivalent to clicking on the **Open** activation button.
Save	Enables you to save an xml format file on your PC. This is equivalent to clicking on the **Save** activation

Button	Description
	button.

10.1.2 Format Editor – Top Level Tabs

When you select the New activation button a populated window will appear as shown below.

Format Editor: <Not Saved>

Pixel Rate 25.200000 MHz 39.682540 ns

	Horizontal				Vertical			
Rt	31.500000	KHz			60.000000	Hz		
	Tune 1.000000	Base 31.500000 KHz						
Act	640	Pixels	25.396825	us	480	Lines	15.238095	ms
Bln	160	Pixels	6.349206	us	45	Lines	1.428571	ms
Tot	800	Pixels	31.746032	us	525	Lines	16.666667	ms
PD	16	Pixels	0.634921	us	10	Lines	0.317460	ms
PW	96	Pixels	3.809524	us	2	Lines	0.063492	ms

Serration width Adjustment 0 Pixels

H to V Pulse Delay 0 Pixels

Horizontal Broad Pulse Delay 0 Pixels

Eq. Before 0 Lines

Eq. After 0 Lines

Entry Units

● Machine

○ Time

Scan Type

● Progressive

○ Interlace

☐ Back Porch

☐ Clock Pulse

☐ PreEmphasis

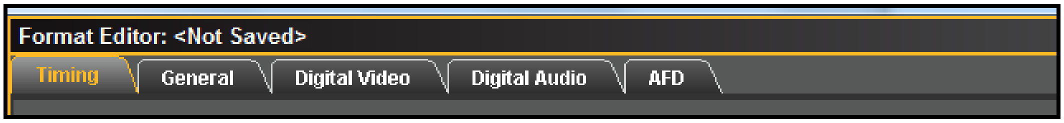
☐ DC Balance

☐ Flat Front Porch

☐ TriLevel

☐ Repeat Field

There are a series of tabs on the top as shown below.



Format Editor: <Not Saved>

The following table describes the top level tabs in the Format Editor.

Tab	Description / Function
Timing	Selecting the Timing tab opens up an application screen that enables you to define the timing parameters for a custom format or modify the timing parameters of an existing format.

Tab	Description / Function
General	Selecting the General tab opens up an application screen that enables you to define the sync, level, pixel depth, gamma and pedestal parameters for a custom format or modify these parameters of an existing format.
Digital Video	Selecting the Digital Video tab opens up an application screen that enables you to define the digital video parameters for a custom format or modify these parameters of an existing format.
Digital Audio	Selecting the Digital Audio tab opens up an application screen that enables you to define the digital audio parameters for a custom format or modify these parameters of an existing format.
AFD	Selecting the AFD tab opens up an application screen that enables you to define the AFD parameters for a custom format or modify these parameters of an existing format.

10.2 Format Editor – New Format

This subsection defines the tabs and status panels available with Format Editor shown below.

Important Note: Many of the settings and parameters in the Format Editor screens apply only to HDMI or analog and do not apply to DisplayPort.

Pixel Rate 25.200000 MHz 39.682540 ns

	Horizontal		Vertical	
Rt	31.500000 KHz		60.000000 Hz	
	Tune 1.000000	Base 31.500000 KHz		
Act	640 Pixels	25.396825 us	480 Lines	15.238095 ms
Bln	160 Pixels	6.349206 us	45 Lines	1.428571 ms
Tot	800 Pixels	31.746032 us	525 Lines	16.666667 ms
PD	16 Pixels	0.634921 us	10 Lines	0.317460 ms
PW	96 Pixels	3.809524 us	2 Lines	0.063492 ms

Serration width Adjustment 0 Pixels

H to V Pulse Delay 0 Pixels

Horizontal Broad Pulse Delay 0 Pixels

Eq. Before 0 Lines

Eq. After 0 Lines

Entry Units

- ● Machine
- ○ Time

Scan Type

- ● Progressive
- ○ Interlace

- ☐ Back Porch
- ☐ Clock Pulse
- ☐ PreEmphasis
- ☐ DC Balance
- ☐ Flat Front Porch
- ☐ TriLevel
- ☐ Repeat Field

10.2.1 New Format - Timing Tab

The **Timing** window of the **Format Editor** is shown below. This window is activated by pressing the **Timing** tab.

Pixel Rate 25.200000 MHz 39.682540 ns

	Horizontal				Vertical			
Rt	31.500000	KHz			60.000000	Hz		
	Tune 1.000000	Base 31.500000 KHz						
Act	640	Pixels	25.396825	us	480	Lines	15.238095	ms
Bln	160	Pixels	6.349206	us	45	Lines	1.428571	ms
Tot	800	Pixels	31.746032	us	525	Lines	16.666667	ms
PD	16	Pixels	0.634921	us	10	Lines	0.317460	ms
PW	96	Pixels	3.809524	us	2	Lines	0.063492	ms

Serration width Adjustment 0 Pixels

H to V Pulse Delay 0 Pixels

Horizontal Broad Pulse Delay 0 Pixels

Eq. Before 0 Lines

Eq. After 0 Lines

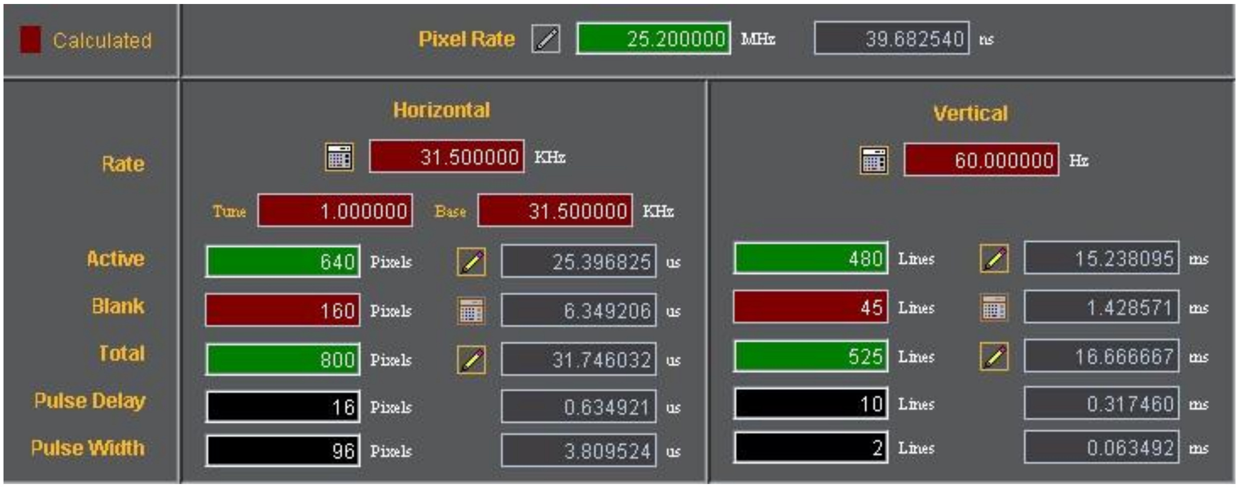
Entry Units
● Machine
○ Time

Scan Type
● Progressive
○ Interlace

☐ Back Porch

☐ Clock Pulse
☐ PreEmphasis
☐ DC Balance
☐ Flat Front Porch
☐ TriLevel
☐ Repeat Field

The main panel of the **Timing** tab is shown below.



🟥 Calculated

Pixel Rate 25.200000 MHz 39.682540 ns

	Horizontal				Vertical			
Rate	31.500000	KHz			60.000000	Hz		
	Tune 1.000000	Base 31.500000 KHz						
Active	640	Pixels	25.396825	us	480	Lines	15.238095	ms
Blank	160	Pixels	6.349206	us	45	Lines	1.428571	ms
Total	800	Pixels	31.746032	us	525	Lines	16.666667	ms
Pulse Delay	16	Pixels	0.634921	us	10	Lines	0.317460	ms
Pulse Width	96	Pixels	3.809524	us	2	Lines	0.063492	ms

The table that follows describes each of the fields in the main panel of the **Timing** tab.

Tab	**Field**	**Description / Function**
Pixel Rate		Sets the pixel rate in pixels (Machine) or microseconds (Time) of the format.
Horizontal	Rate	The horizontal line rate of the format. The HRAT is the fundamental frequency in the 882. Parameter: HRAT.
	Tune	The tunning value of the base frame rate (base/tune) for NTSC color broadcast compatibility. The tuning value is base/1.001
	Base	The base frame rate.
	Active	The number of active pixels (machine) or microseconds (Time) of the horizontal video. Parameter: HRES.
	Blank	The number of active pixels (Machine) or microseconds (Time) of the horizontal video. This parameter is calculated.
	Total	The total number of active pixels (Machine) or microseconds (Time) of the horizontal video. The total is the sum of the Active and Blanking. Parameter: HTOT.
	Pulse Delay	The number of pixels (Machine) or microseconds (Time) in the blanking preceding the horizontal sync pulse. Parameter: HSPD.
	Pulse Width	The number of pixels (Machine) or microseconds (Time) of the horizontal sync pulse. Parameter: HSPW.
Vertical	**Rate**	The vertical frame rate of the format. Parameter: VRAT.
	Active	The number of active lines (machine) or milliseconds (Time) of the vertical video. Parameter: VRES.
	Blank	The number of active lines (Machine) or milliseconds (Time) of the vertical video. This parameter is calculated.
	Total	The total number of active lines (Machine) or milliseconds (Time) of the vertical video. The total is the sum of the Active and Blanking. Parameter: VTOT.
	Pulse Delay	The number of lines (Machine) or milliseconds (Time) in the blanking preceding the vertical sync pulse. Parameter: VSPD.
	Pulse Width	The number of lines (Machine) or milliseconds (Time) of the vertical sync pulse. Parameter: VSPW.
🖩 (green calculator)		Indicates that the value in the field is calculated by the Format Editor.
🖩 (red calculator)		Indicates that the value in the field is calculated by the Format Editor, and that the new value has replaced the value previously in the field.
✏		Indicates that the values in this field are settable in the current configuration.
🟥 Red Field		Indicates that the fields are in the read only mode. These fields will show a change in value when the value in a field affecting these fields is modified.

Tab	Field	Description / Function
Green Field		Indicates that the fields are in the read/write mode. When you make a change and hit the enter key new values will be calculated.
Black Field		Indicates that the fields can be modified directly and are calculated when other related fields are modified.
Grey Field		Indicates that the fields are disabled because the Entry Units are selected such that the fields are not used. However these fields will show a change when the value in a field affecting these fields is modified.

10.2.2 New Format - Timing Tab (Right Side Panel)

The right side panel of the **Timing** tab in the Format Editor is shown below. The table that follows describes each of the fields in the panel.


Entry Units
- ● Machine
- ○ Time

Scan Type
- ● Progressive
- ○ Interlace

- ☐ Back Porch
- ☐ Clock Pulse
- ☐ PreEmphasis
- ☐ DC Balance
- ☐ Flat Front Porch
- ☐ TriLevel
- ☐ Repeat Field

The table that follows describes each of the fields in the main panel of the **Timing** tab.

Tab	Field	Description / Function
Pixel Rate	Machine	Activates the fields in the timing tab window such that the timing parameter values are expressed and settable in terms of pixels and lines.
	Time	Activates the fields in the timing tab window such that the timing parameter values are expressed and settable in terms of time increments such as milliseconds and microseconds.
Scan Type	Progressive	Sets the format scan type to Progressive. Parameter: SCAN = 2

Tab	Field	Description / Function
	Interlace	Sets the format scan type to Interlaced. Parameter: SCAN = 1
Check boxes	Back Porch	Toggles the Pulse Delay field so that the value is provided for the back porch rather than the front porch.
	Clock Pulse	Enables and disables the pixel clock pulse output on generators that have a pixel clock output available. The pixel clock output appears on the special sync BNC connector.
	Pre-Emphasis Not applicable to DP	Enables and disables adding pre-emphasis to the Open LVDI digital outputs on generators that support LVDI outputs.
	DC Balance	Not used.
	Flat Front Porch Not applicable to DP	Determines if composite sync will have all equalization pulses removed in the vertical sync front porch (delay) period as required by certain military HOBO and Maverik video formats.
	Tri-Level Sync	Enables or disables Tri-Level sync.
	Repeat Field	Determines if identical video information is output for each field of an interlaced (SCAN = 2) format.

10.2.3 New Format - General Tab

The **Format Editor General** tab is shown below. The table that follows describes each of the fields in the tab.

Format Editor: <Not Saved>

Horizontal Vertical
Unit Size 11.200000 8.400000 ● inches ○ mm
Pixel Depth Default

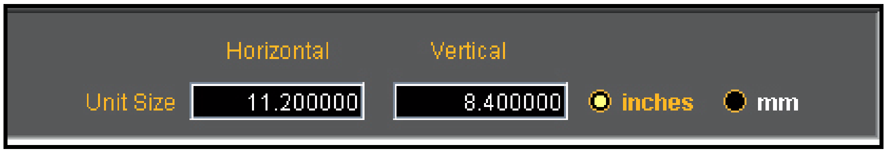
Color Encoding: Digital Component RGB
Sync Type: DSS
ACS Type: American ORed
DCS Type: American ORed
DSS Type: American Separate
SubCarrier: None

Video Swing: 0.700000 V white-blank
Sync Swing: 0.300000 V blank-sync
Gamma ☐ 2.200000
Pedestal ☐ 7.500000 IRE
Cal. Mode: Interpolate
Color Order: R-G-B

Analog Sync Gate: R OFF, G ON, B OFF
Digital Sync Gate: H ON, V ON, C ON
Digital Sync Polarity: H −, V −, C −
Video Gate: R ON, G ON, B ON

10.2.4 New Format - General Tab (Top Left Panel)

The top left panel of the General tab in the Format Editor is shown below.



Horizontal Vertical
Unit Size 11.200000 8.400000 ● inches ○ mm

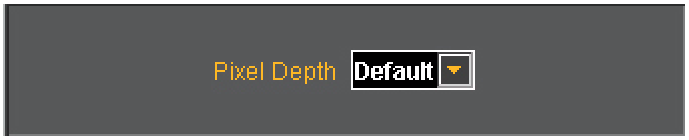
The table that follows describes each of the fields in the top left panel of the General tab.

Field / Entity	Type	Description / Function
Horizontal	Entry field	The horizontal aperture of the display under test.
Vertical	Entry field	The vertical aperture of the display under test.
Unit Size	**Radio Buttons:**	

Field / Entity	Type	Description / Function
	inches	Selects the unit size of the Horizontal and Vertical Size entities to be expressed in inches.
	mm	Selects the unit size of the Horizontal and Vertical Size entities to be expressed in millimeters.

10.2.5 New Format - General Tab (Top Right Panel)

The top right panel of the **General** tab in the **Format Editor** is shown below.



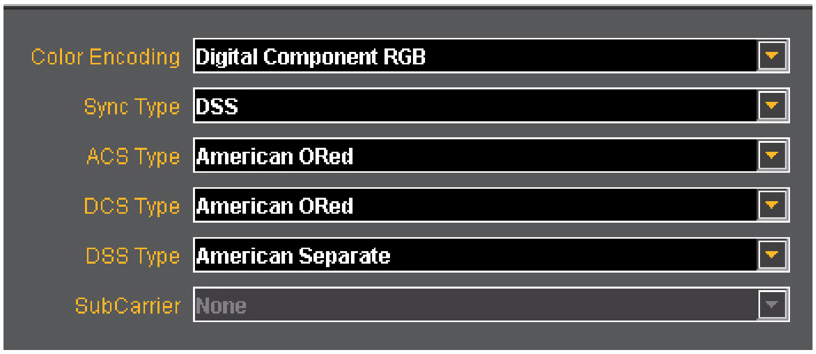
Pixel Depth Default

The table that follows describes each of the fields in the top right panel of the **General** tab.

Field / Entity	Type	Description / Function
Pixel Depth	Pull-down menu	Establishes the number of data bits that represent each active pixel in video memory (frame buffer). Parameter: PELD. There are three settings: • Default - uses the generator default • 8 - 8 bits-per-pixel (256 colors) • 24 - 24 bits-per-pixel (16,777,216 colors)

10.2.6 New Format – General Tab (Center Panel)

The center panel of the **General** tab in the **Format Editor** is shown below.



Color Encoding Digital Component RGB
Sync Type DSS
ACS Type American ORed
DCS Type American ORed
DSS Type American Separate
SubCarrier None

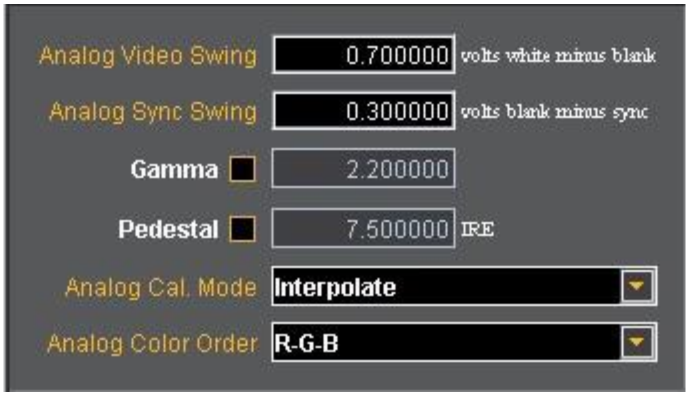
The table below describes the pull-down menus in the center panel of the **General** tab.

Field / Entity	Description / Function
Color Encoding	Sets the colorimetry of the format. The parameter is AVST or DVST. The following are the selections: • Digital Component RGB • Digital Component YCbCr SDTV (ITU-R BT.601-5) • Digital Component YCbCr HDTV Legacy (SMPTE 240M) • Digital Component YCbCr HDTV Modern (ITU-R BT.709-5)

Field / Entity	**Description / Function**
	• Digital BT.601 xvYCC • Digital BT.709 xvYCC **Note**: Several options are not shown and are not applicable to HDMI.
Sync Type **Not used for HDMI**	Sets the sync type of the format. The following are the selections: • (0) None • (1) DSS - Digital Separate Sync • (2) DCS - Digital Composite Sync • (3) ACS - Analog Composite Sync • (4) ACS, DSS - Analog Composite Sync, Digital Separate Sync • (5) ACS, DCS - Analog Composite Sync, Digital Composite Sync • (6) ACS, DCS, DSS - Analog Composite Sync, Digital Composite Sync and Digital Separate Sync • (7) DPMS OFF • (8) DPMS Suspend • (9) DPMS Standby • (10) DPMS ON **Note**: Several options are not shown and are not applicable to HDMI.
ACS Type (Not used)	Not used for DP
DCS Type (Not used)	Not used for DP
SubCarrier (Not used)	Not used for DP

10.2.7 New Format - General Tab (Right Panel)

The right panel of the General tab in the Format Editor is shown below.



Analog Video Swing 0.700000 volts white minus blank

Analog Sync Swing 0.300000 volts blank minus sync

Gamma ☐ 2.200000

Pedestal ☐ 7.500000 IRE

Analog Cal. Mode Interpolate

Analog Color Order R-G-B

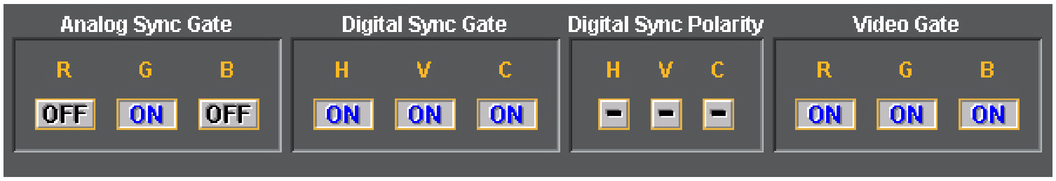
The table below describes the entities and fields of the right-side panel of the **General** tab.

Field / Entity	**Entity Type**	**Description / Function**
Analog Video Swing **Not used for HDMI**	Entry field	Sets the analog video swing.
Analog Sync Swing	Entry field	Sets the analog sync swing.

Field / Entity	Entity Type	Description / Function
Not used for HDMI		
Gamma **Not used for HDMI**	Check box	Enables or disables Gamma. Used with the entry field below.
	Entry field	Enables you to set the Gamma once the Gamma check box above is enabled (checked). The allowable ranges of values is 0.1 to 10.0.
Pedestal **Not used for HDMI**	Check box	Enables or disables the Pedestal. Used with the entry field below. Pedestal is only supported on NTSC format types.
	Entry field	Enables you to set the Pedestal once the Pedestal check box above is enabled (checked). The allowable ranges of values is 0 IRE to 100 IRE.
Analog Cal. Mode **Not used for HDMI**	Pull-down select	Sets the analog calibration mode. Determines how the generator tests and calibrates its analog video outputs. The following are the selections: • Interpolate • Measure Interpolate • Measure Set Absolute • Test Levels
Analog Color Order **Not used for HDMI**	Pull-down select	Sets the mapping of the analog video colors to the video output connections. Parameter: AVCO. The following are the selections: • RGB - R to R, G to G, B to B (default) • RBG - R to R, B to G, G to B • GRB - G to R, R to G, B to B • GBR - G to R, B to G, G to B • BRG - B to R, R to G, G to B • BGR - B to R, G to G, R to B

10.2.8 New Format - General Tab (Bottom Panel)

The bottom panel of the **General** tab in the **Format Editor** is shown below.



The table below describes the gating functions of the right-side panel of the **General** tab.

Field / Entity	Entity Name	Description / Function
Analog Sync Gate **Not used for HDMI**	Select buttons	Enables you to put the analog composite sync on one of the components when analog composite sync is selected as the sync type . Multiple selections can be made.
	R	Puts the analog composite sync on the Red component.
	G	Puts the analog composite sync on the Green

Field / Entity	Entity Name	Description / Function
		component.
	B	Puts the analog composite sync on the Blue component.
Digital Sync Gate **Not used for HDMI**	Select buttons	
	H	Enables and disables the digital horizontal sync output.
	V	Enables and disables the digital vertical sync output. To use digital vertical sync, the digital separate H and V sync must be selected.
	C	Enables and disables the digital vertical sync output.
Digital Sync Polarity **Not used for HDMI**	Select buttons	
	H	Determines whether the digital horizontal sync pulse polarity is positive going or negative going.
	V	Determines whether the digital vertical sync pulse polarity is positive going or negative going.
	C	Determines whether the digital composite sync pulse polarity is positive going or negative going.
Video Gate	Select buttons	Enables you to gate ON or OFF any of the video components. More than one can be selected.
	R	Gates ON or OFF the Red component. Parameter: REDG
	G	Gates ON or OFF the Green component. Parameter: GRNG.
	B	Gates ON or OFF the Blue component. Parameter: BLUG.

10.3 New Format - Digital Video Tab

The **Format Editor Digital Video** tab is shown below.

Format Editor: <Not Saved>

Range 0
Clocks per Pixel 1
Pixels per Pixel 1
AVI Video Identification Code 1
Number of Links ● 1 ○ 2

Protocol Type DVI
Sampling Mode Default
Bits per Color Component Default
Video Swing 1 1.000000 Vp-p
Video Swing 2 1.000000 Vp-p

The table that follows describes each of the fields in the **Digital Video** tab.

Field / Entity	Entity Type	Description / Function
Range	Entry field	Specifies the quantization range for the digital video. Parameter: DVQM. The values available are described in CIA-861E: • 0 - Full Range for computer applications. • 1 – for testing the undershoot/overshoot signal code margins. • 2 – Limited range for reduced range required by television standards.
Clocks per Pixel	Entry field	Specifies the number of clocks per pixel (double clocking factor for whole line. Parameter: NCPP. This parameter is used to boost the clock rate to the minimum supported by TMDS interface. Allowable values are:

Field / Entity	Entity Type	Description / Function
		• 1 - one clock per pixel. • 2 - two clocks per pixel.
Pixels per Pixel	Entry field	Specifies the number of pixels per pixel. This parameter specifies the pixel repetition factor for the active portion of the line. Allowable values are: • 0 - disables repetition mode • 1 to 10 - enables pixel repetition (inserts extra left and right pixel repetition bars) Parameter: NPPP.
AVI Video Identification Code	Entry field	The digital video code corresponding to the EIA/CEA-861 standard. Parameter: DVIC.
Number of Links **Not used for DP**	Radio button	
	1	Sets the number of links to 1 by the DVI output.
	2	Sets the number of links to 2 for the DVI output
Protocol Type	Pull-down select	Specifies which digital output is active through the HDMI interface. Allowable values are: • DVI - Enables DVI mode out the DVI output or the HDMI output. • HDMI - Enables HDMI mode out the HDMI output. Parameter: XVSI
Sampling Mode	Pull-down select	Specifies the digital sampling mode. Allowable values are: • Default - RGB 4:4:4. • 4:2:2 - Color difference components are sampled at half the pixel rate. Luminance is sampled at the full pixel rate. Requires that the YCbCr color mode be selected with the DVST command. • 4:4:4 - Color difference components and luminance component is sampled at the full pixel rate. Requires that the YCbCr color mode be selected with the DVST command. Parameter: DVSM
Bits per Color Component	Pull-down select	Specifies the number of bits per component. Allowable values are: • Default - Use the default setting in the generator. • 6 - Six bits per component. • 8 - Eight bits per component. • 10 - Ten bits per component. • 12 - Twelve bits per component. Parameter: NBPC

10.4 New Format - Digital Audio Tab

The **Format Editor Digital Audio** tab is shown below. The table that follows describes each of the fields in the tab.

Signal Interface: SPDIF

Signal Type: IEC 60958-3 Consumer LPCM

Level Shift: 0 -dBFs

Sampling Rate: 48000.000000 Hz

Number of Streams: 1

Number of Channels: 2

Bits per Sample: 16

Contents Gated: 3

Contents Available: 3

Mix Down Gate: ☑

Channels Available: 3

Channels Gated: 3

The table below describes each of the fields in the **Digital Audio** tab.

Field	Type	Description / Function
Signal Interface **Not used for DP**	Pull-down select	Sets the digital audio signal interface. The valid values are: • None - Use DP. • SPDIF. • AES3 (not used). • AESid (not used). • TOSlink optical (not used). • MiniPlug (not used).
Signal Type	Pull-down select	Sets the digital audio signal interface. The valid values are: • None

Field	Type	Description / Function
		• IEC 60958-3 Consumer LPCM. • IEC 60958-4 Professional LPCM. • IEC 61937 w/AC-3 (Dolby Digital). • MP2 (Video CD) (not used). • MP3 (MPEG1 Layer 3) (not used). • MPEG2 5.1 channels Advanced Audio Coding (AAC) • MPEG2 7.1 channel CBR or VBR • IEC 61937 w/'DTS • ATRAC
Level Shift	Entry field	Sets the digital audio level shift value for linear PCM. The valid values are: 0 - 15 dBFS. Parameter is: DALS
Sampling Rate	Entry field	Sets the digital audio sampling rate for linear PCM. The valid values are: • 32.0kHz • 44.1kHz • 48.0kHz • 88.2kHz • 96.0kHz • 176.4kHz • 192.0kHz Parameter is: ARAT
Number of Streams	Entry field	Sets the digital audio streams. The valid value is: 1. Parameter is: NDAS.
Number of Channels	Entry field	Sets the digital audio sampling rate for linear PCM. The valid values are: 2 through 8 Parameter is: NDAC.
Bits per Sample	Pull-down select	Sets the digital audio sampling rate for linear PCM. The valid values are: • 16 • 20 • 24 Parameter is: NBPA.
Contents Gated	Entry field	Sets the digital audio content gate. The valid values are: 0 through 4095. Refer to EIA/CEA-861-x.
Contents Available	Entry field	Sets the digital audio content available. The valid values are: 0 through 4095. Refer to EIA/CEA-861-x.
Mix Down Gate	Check box	Sets the digital audio down-mix gate. The valid values are: enabled (0)

Field	Type	Description / Function
Not applicable		or disabled (1).
Channels Available	Entry field	Sets the digital audio channels available. The valid values are: 0 through 255. Refer to EIA/CEA-861.
Channels Gated	Entry field	Sets the digital audio channel gate. The valid values are: 0 through 255. Refer to EIA/CEA-861.

10.5 New Format - AFD Tab

The **Format Editor AFD** tab is shown below. The table that follows describes each of the fields in the tab.

Active Format

Content Aspect Ratio 1.333333
Embedded Aspect Ratio 1.333333
Signal Aspect Ratio 1.333333
Emb. From Content Apert. Map 0
Signal from Emb. Apert. Map 0

Bars

Left 0 Pixels
Right 0 Pixels
Top 0 Pixels
Bottom 0 Pixels

The table that follows describes each of the text entry fields in the **AFD** tab.

Heading	Field	Description / Function
Active Format	**Content Aspect Ratio**	Sets the aspect ratio of the source image content. The valid parameter range is: 0.75 to 2.39.
	Embedded Aspect Ratio	Sets the aspect ratio of the extended image content. The

Heading	Field	Description / Function
		valid parameter range is: 0.75 to 2.39.
	Signal Aspect Ratio	Sets the aspect ratio of the video signal image content. The valid parameter range is: 0.75 to 2.39.
	Extended From Content Apert. Map	Enables you to set the mapping type for mapping CXAR-shaped image content into the extended EXAR-shaped aperture.
	Signal from Extended Apert. Map	Enables you to set the mapping type for mapping EXAR-shaped image content into the SXAR-shaped signal interface.
Bars	**Left**	Sets the left side letterbox bars in pixels.
	Right	Sets the right side letterbox bars in pixels.
	Top	Sets the top letterbox bars in pixels.
	Bottom	Sets the bottom letterbox bars in pixels.

10.6 Format Editor - Open

This subsection defines the **Open Format** dialog box. The **Open Format** dialog box is shown below. This enables you to open an existing format file from your 980 instrument.

Format Editor: null/240p2x_4.xml

Open Format

Local Files

720p24.xml
720p24_.xml
720p25.xml
720p29.xml
720p30.xml
720p50.xml
720p59.xml
720p60.xml

000074 ns

Time 1.00000

Act 720 Pixels

Bln 138 Pixels

Tot 858 Pixels

PD 19 Pixels

PW 62 Pixels

59.885932 Hz

Lines 15.238095 ms

Lines 1.460317 ms

Lines 16.698413 ms

Lines 0.317460 ms

Lines 0.190476 ms

Entry Units: ● Machine ○ Time

Scan Type: ● Progressive ○ Interlace

☐ Back Porch

☐ Clock Pulse

☐ PreEmphasis

☐ DC Balance

☐ Flat Front Porch

☐ TriLevel

☐ Repeat Field

Serration width Adjustment 0 Pixels

H to V Pulse Delay 0 Pixels

Horizontal Broad Pulse Delay 0 Pixels

Eq. Before 3 Lines

Eq. After 3 Lines

10.7 Format Editor - Save

This subsection defines the Save [File] dialog box. The Save dialog box is shown below. You use the Save function to store a format that you have defined. You can either save it to your PC (Local tab) or the 882 instrument (Remote tab).

Format Editor: /User/nh

Pixel Rate 25.200000 MHz 39.682540 ns

Save Format

Local Files

- User
  - hg
  - myformat
  - nh

New Rename Delete

Path: /User

Name:

The name can not be blank.

Ok Cancel

Rt 31.500000 ... 0 Hz

Tune 1.000000 Base 3

Act	640 Pixels	15.238095	ms
Bln	160 Pixels	1.428571	ms
Tot	800 Pixels	16.666667	ms
PD	16 Pixels	0.317460	ms
PW	6000 Pixels	0.063492	ms

Serration width Adjustment 0 Pixels

H to V Pulse Delay 0 Pixels

Horizontal Broad Pulse Delay 0 Pixels

Eq. Before 0 Lines

Eq. After 0 Lines

Entry Units
● Machine
○ Time

Scan Type
● Progressive
○ Interlace

☐ Back Porch

☐ Clock Pulse
☐ PreEmphasis
☐ DC Balance
☐ Flat Front Porch
☐ TriLevel
☐ Repeat Field

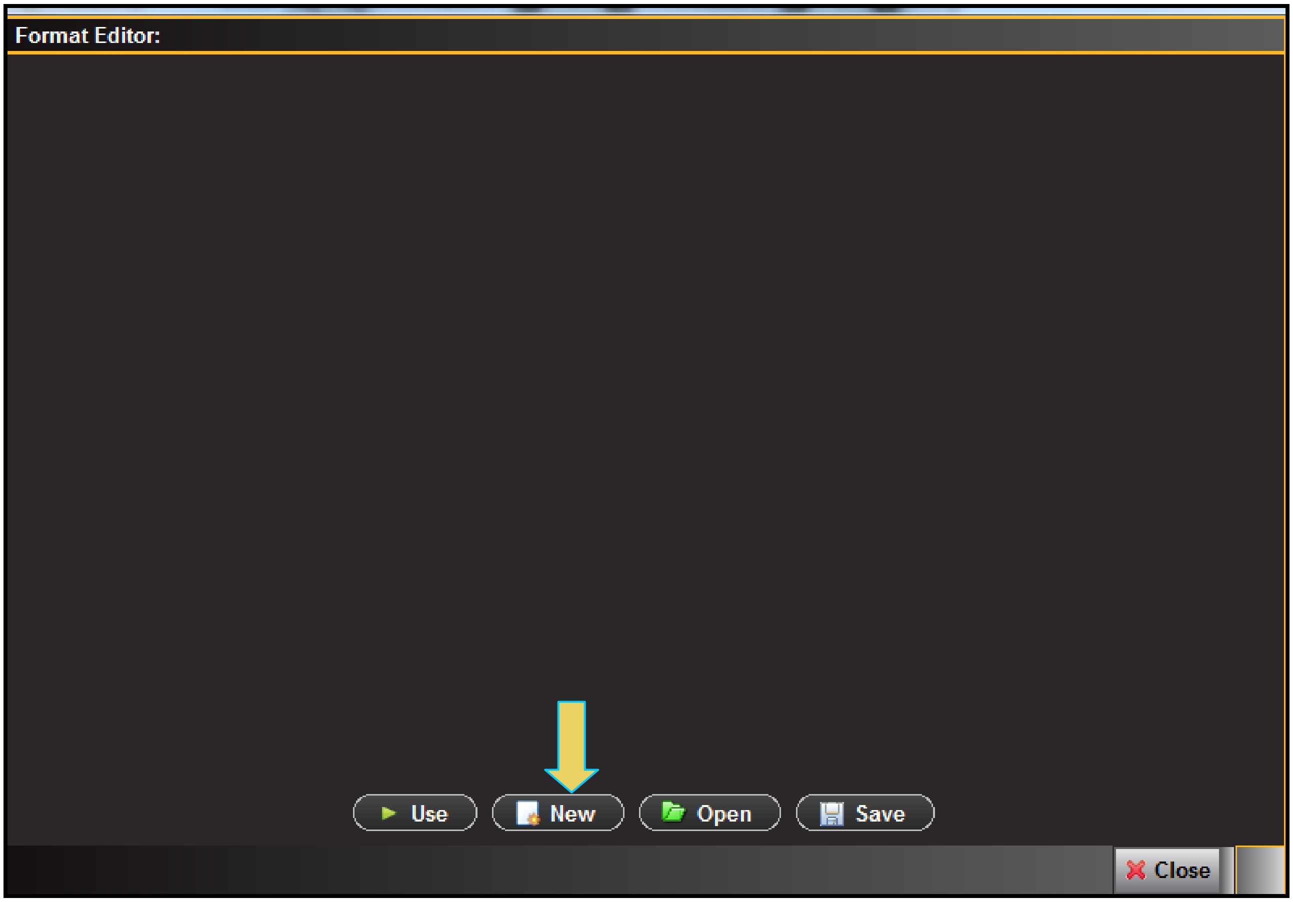
10.8 Creating a new format using the Format Editor

The procedure below describes how to create a new format using the Format Editor.

To create a new format using the Format Editor:

1. Access the Format Editor using the procedures described in Accessing the Format Editor.

   The **Format Editor** appears.



3. Click the **New** activation button on the bottom of the panel (indicated above).

   The **Timing** tab of the format definition page appears as shown below.

Pixel Rate 25.200000 MHz 39.682540 ns

	Horizontal				Vertical			
Rt	31.500000	KHz			60.000000	Hz		
Act	640	Pixels	25.396825	us	480	Lines	15.238095	ms
Bln	160	Pixels	6.349206	us	45	Lines	1.428571	ms
Tot	800	Pixels	31.746032	us	525	Lines	16.666667	ms
PD	16	Pixels	0.634921	us	10	Lines	0.317460	ms
PW	96	Pixels	3.809524	us	2	Lines	0.063492	ms

Tune 1.000000 Base 31.500000 KHz

Serration width Adjustment 0 Pixels

H to V Pulse Delay 0 Pixels

Horizontal Broad Pulse Delay 0 Pixels

Eq. Before 0 Lines

Eq. After 0 Lines

Entry Units
● Machine
○ Time

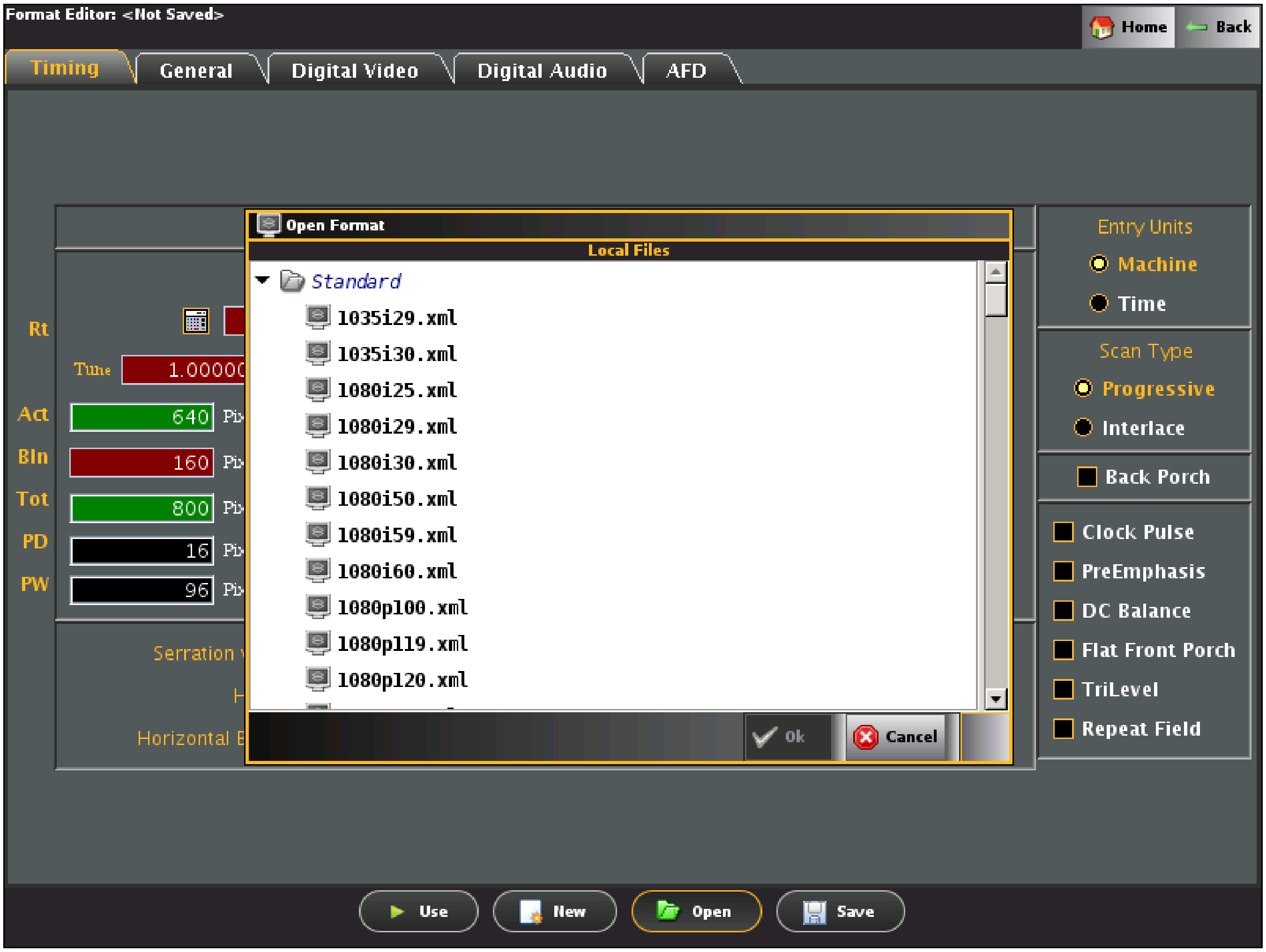
Scan Type
● Progressive
○ Interlace

☐ Back Porch

☐ Clock Pulse
☐ PreEmphasis
☐ DC Balance
☐ Flat Front Porch
☐ TriLevel
☐ Repeat Field

4. Open an existing file to work from by clicking on the **Open** activation button near the bottom of the window (indicated above).

   The open file dialog box appears as shown below.



5. Scroll and select a format file to use as a starting point for defining your new format.

6. The format parameters of the selected format will appear in the new format **Timing** window as shown below.

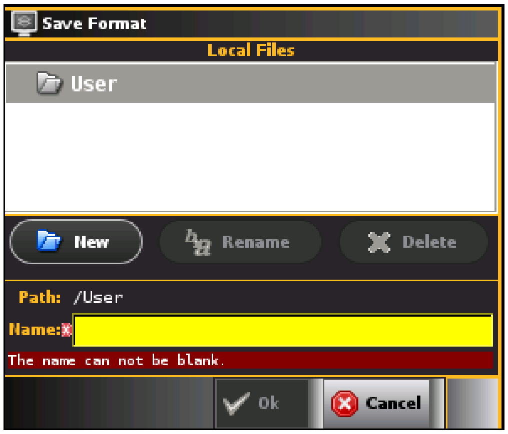
7. Modify the parameters as required for the new format. You can reference the parameter definitions in the tables presented earlier in this chapter. The following guidelines will help you modify the format parameters.

   - When selecting a parameter to modify on the **Timing** tab, ensure that the value is editable. To be editable, the field either needs to have a pencil icon next to it or a black field background. Gray fields are disabled for editing. Fields in red (with the calculator icon) cannot be modified. However you can change whether a field can be modified by clicking on the calculator icon which will cause it to change to a pencil icon allowing you to change its value.
   - Upon modifying a format value hit the enter key to invoke the change. The Format Editor applies the new value to the timing algorithm and updates any values dependent on the value you entered (or changed).

     For example, to change the horizontal resolution to 660, enter the value in the
     Active field under Pixels in the Horizontal area.
     You will notice that the Format Editor has calculated and written values to the **Blank** and **Period** fields as indicated by the red calculator (▦) symbol. Although the Period value has not changed, the Format Editor still indicates it is a calculated value by displaying the red calculator.

8. Save the new format.

   a. Click the **Save** activation button or the select **Save** from the **File** pull-down menu to save the format. The Save dialog box appears as shown below.



The name can not be blank.

   b. Enter new format name in Name field.

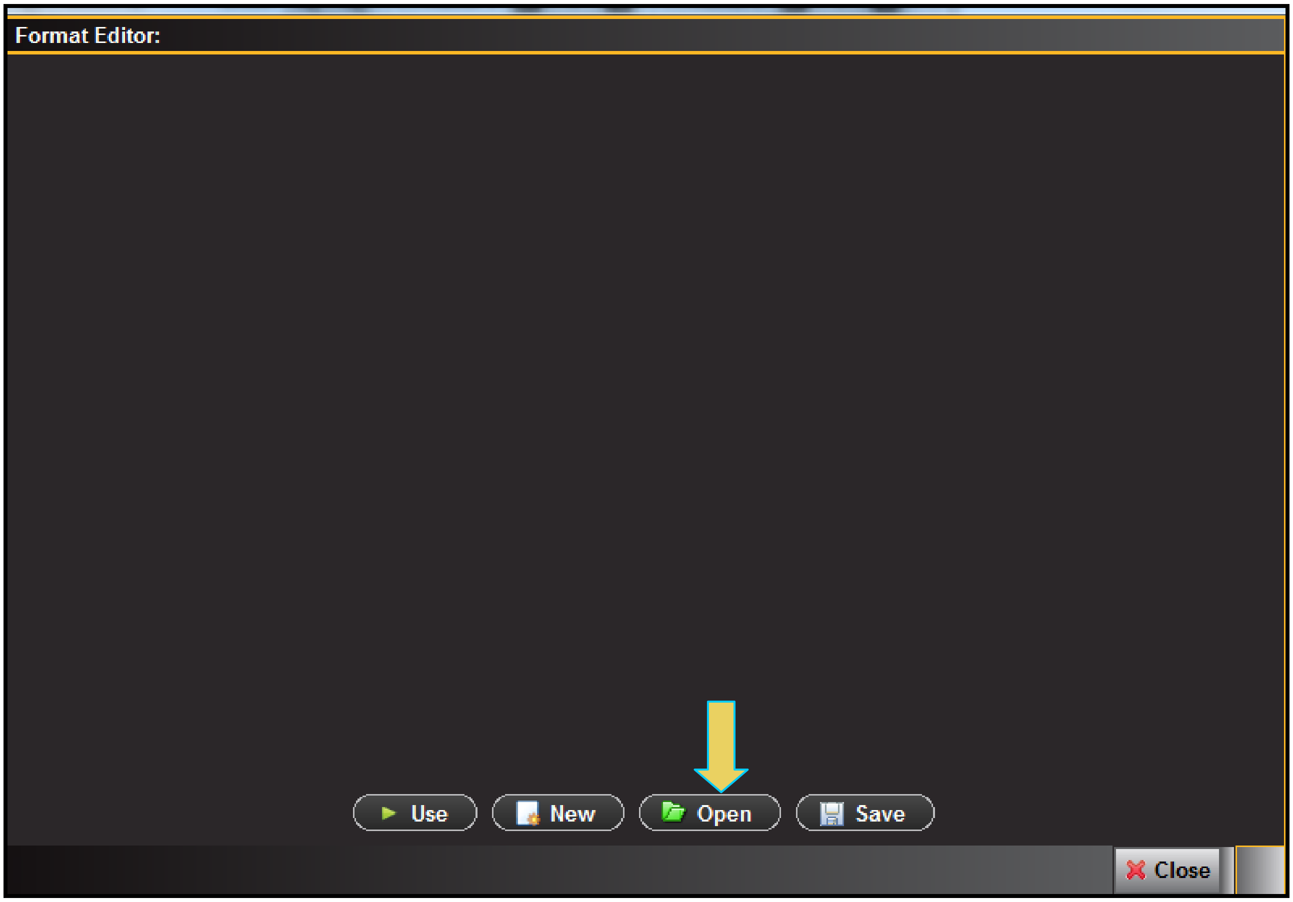
10.9 Modifying an existing format using the Format Editor

The procedure below describes how to make a few changes on an existing format using the **Format Editor**. This enables you to quickly run tests a display by tweaking a few timing parameters at a time.

To modify an existing format with the Format Editor:

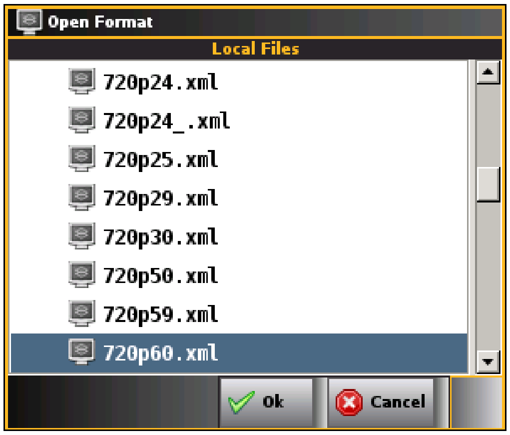
1. Access the **Format Editor** using the procedures described in Accessing the Format Editor.

   The **Format Editor** appears.



4. Click the **Open** activation button on the bottom of the panel (indicated above).

   A dialog box enabling you to scroll and select a format appears as shown below.



720p24.xml
720p24_.xml
720p25.xml
720p29.xml
720p30.xml
720p50.xml
720p59.xml
720p60.xml

Format Editor: /Standard/720p60.xml

Pixel Rate 74.250000 MHz 13.468013 ns

	Horizontal				Vertical			
Rt	45.000000	KHz			60.000000	Hz		
	Tune 1.000000		Base 45.000000	KHz				
Act	1280	Pixels	17.239057	us	720	Lines	16.000000	ms
Bln	370	Pixels	4.983165	us	30	Lines	0.666667	ms
Tot	1650	Pixels	22.222222	us	750	Lines	16.666667	ms
PD	110	Pixels	1.481481	us	5	Lines	0.111111	ms
PW	40	Pixels	0.538721	us	5	Lines	0.111111	ms

Serration width Adjustment 0 Pixels
H to V Pulse Delay 0 Pixels
Horizontal Broad Pulse Delay 0 Pixels
Eq. Before 0 Lines
Eq. After 0 Lines

Entry Units
● Machine
○ Time

Scan Type
● Progressive
○ Interlace

☐ Back Porch

☐ Clock Pulse
☐ PreEmphasis
☐ DC Balance
☐ Flat Front Porch
☑ TriLevel
☐ Repeat Field

The format parameters of the selected format will appear in the new format **Timing** window as shown below.

7. Modify the parameters as required for the new format. The following guidelines will help you modify the format parameters.

   - When selecting a parameter to modify on the **Timing** tab, ensure that the value is editable. To be editable, the field either needs to have a pencil icon next to it or a black field background. Gray fields are disabled for editing. Fields in red (with the calculator icon) cannot be modified. However you can change whether a field can be modified by clicking on the calculator icon which will cause it to change to a pencil icon allowing you to change its value.

- Upon modifying a format value hit the enter key to invoke the change. The **Format Editor** applies the new value to the timing algorithm and updates any values dependent on the value you entered (or changed).

  For example, to change the horizontal resolution to 660, enter the value in the **Active** field under Pixels in the Horizontal area.
  You will notice that the Format Editor has calculated and written values to the **Blank** and **Period** fields as indicated by the red calculator (🖩) symbol. Although the Period value has not changed, the **Format Editor** still indicates it is a calculated value by displaying the red calculator.
- To apply the format settings on the generator, click the **Use** activation button on the lower right side.

8. Use (apply) the modified format by clicking on the **Use** activation button on the bottom of window.

   Monitor the display under test for roper operation.

11 Source Verification with Basic Analyzer (Optional)

The 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module is equipped with a DP 1.4 Rx port for the optional Network Analyzer features. There are two options available:

1) Basic Analyzer – Emulates a DP 1.4 sink device including EDID, DPCD, MST, Link Training emulation. Provides real time view of the incoming source video and metadata including status of mainstream attributes, secondary stream attributes, link training, MST, HDCP. Also provides support for viewing the Aux Channel transactions using the Quantum Data Auxiliary Channel Analyzer (ACA) application when testing a DP source.

2) Protocol Analyzer (requires the Basic Analyzer license to be installed) – Provides capture and store of the main link protocol, video and metadata including main stream attributes and secondary data from an incoming DP source device. **Note**: Description and procedures for this option is not included in this version of the User Guide.

11.1 Accessing the Basic Analyzer features

Use the following procedures to access the Network Analyzer feature.

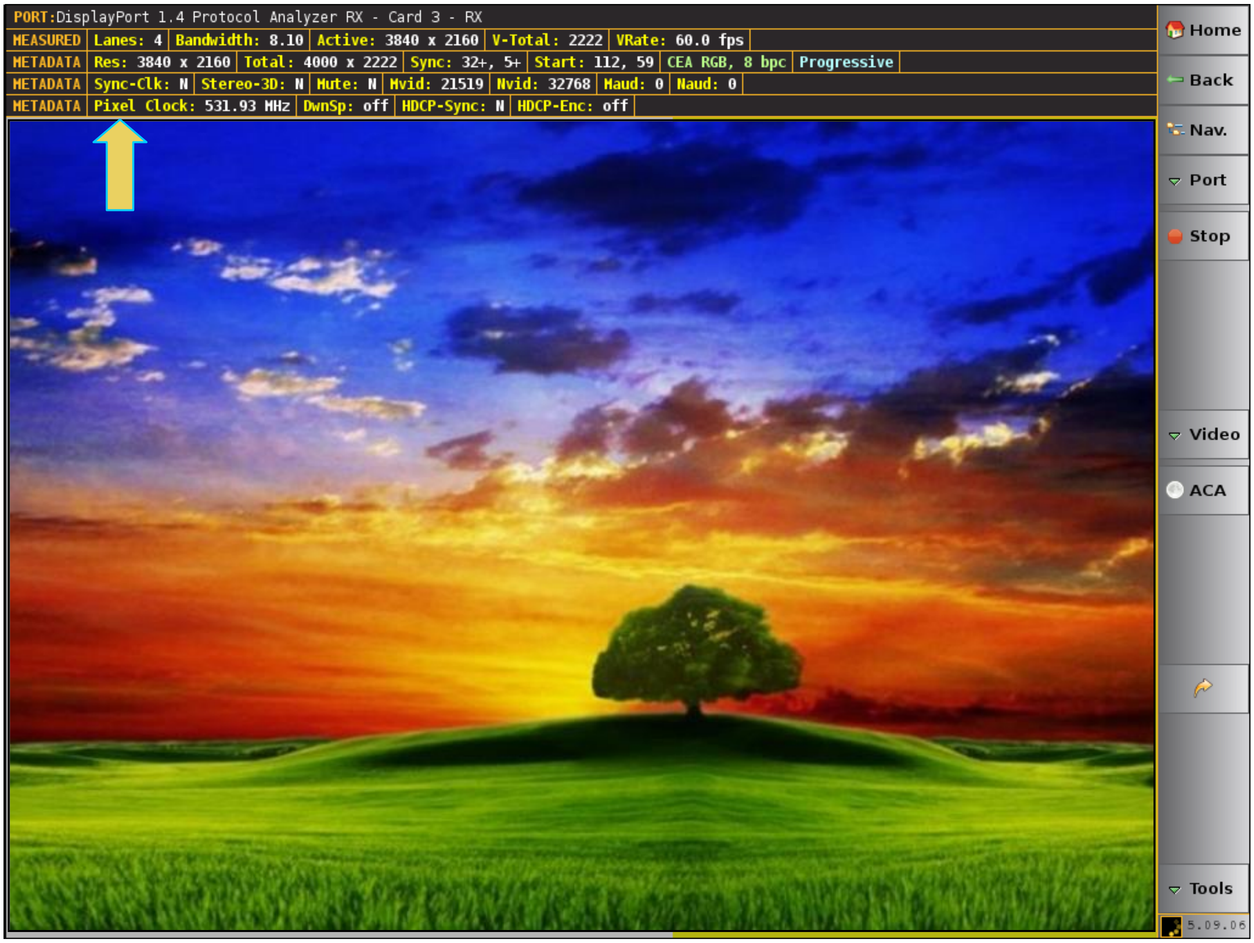
To access the Network Analyzer:

1 Access the **Format Editor** through the **Card Control** Page of the **Apps** panel as shown below. Select the icon for the DP Video Generator Rx Card (not shown).


quantumdata
Card Control
Generator
HDMI
Protocol Analyzer
RX - Card 6
HDMI
Video Generator
RX - Card 7
Aux. Channel
Analyzer
Capture Control
HEAC
Page 1 of 4
Card Control
Compliance Tests
Editors
Other
Back
Navigator
DHCP: 192.168.254.143
ATP Version: 4.9.38 (5 cards detected)

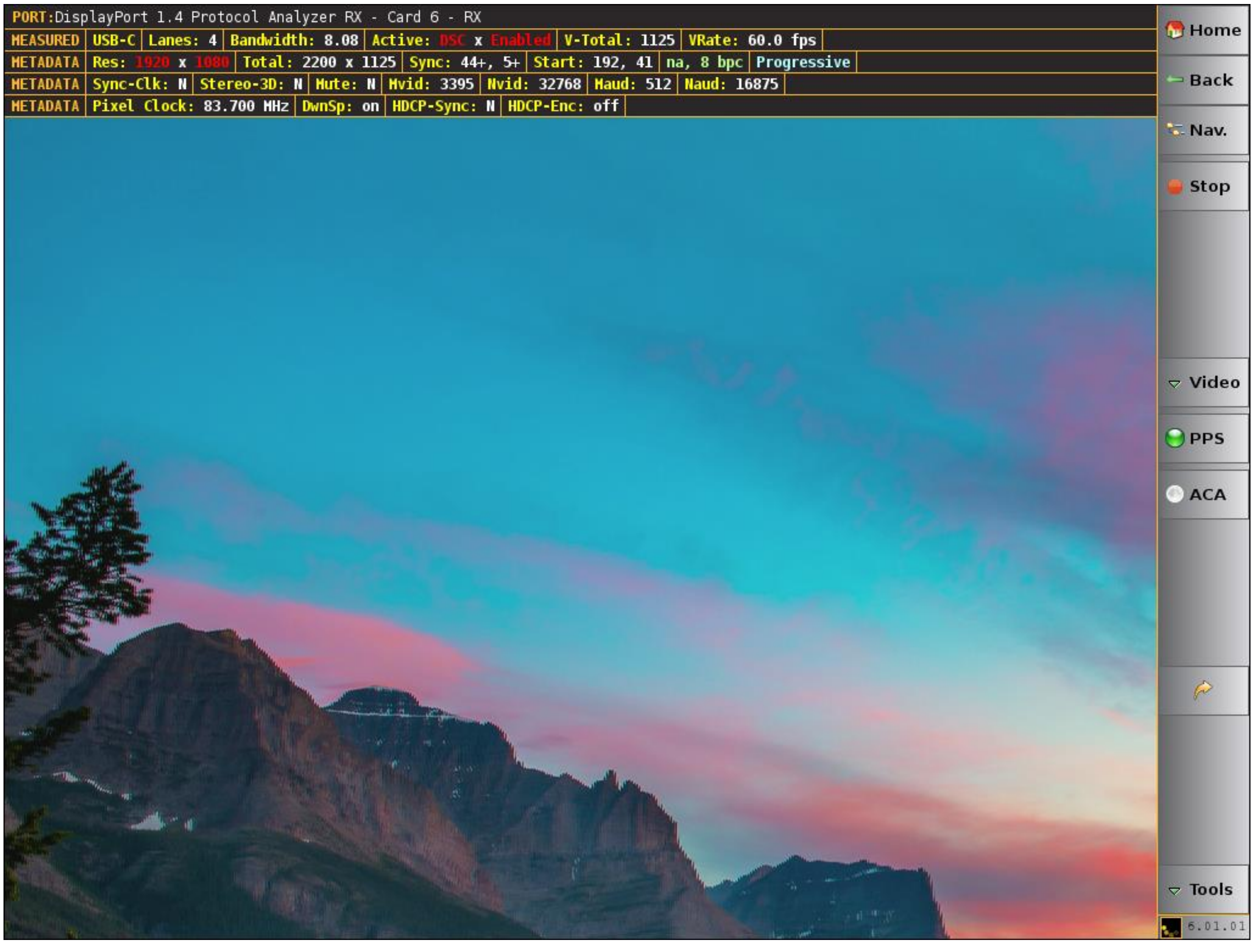
The Analyzer panel appears showing the incoming video image. The module's Rx analyzer port provides periodic video frame captures enabling you to view frames of video. This feature provides a basic confidence test to verify that the incoming video is essentially correct.

There is a dashboard on the top of the panel indicating the essential video characteristics. There is a set of controls on the right.



```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 3 - RX
MEASURED | Lanes: 4 | Bandwidth: 8.10 | Active: 3840 x 2160 | V-Total: 2222 | VRate: 60.0 fps
METADATA | Res: 3840 x 2160 | Total: 4000 x 2222 | Sync: 32+, 5+ | Start: 112, 59 | CEA RGB, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 21519 | Nvid: 32768 | Maud: 0 | Naud: 0
METADATA | Pixel Clock: 531.93 MHz | DwnSp: off | HDCP-Sync: N | HDCP-Enc: off
```

The following example shows the USB-C DP alt mode analyzer port active with DSC.



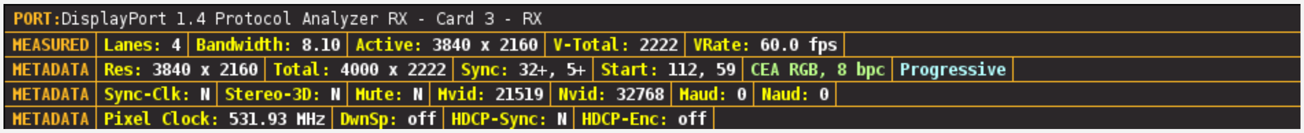
```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 6 - RX
MEASURED | USB-C | Lanes: 4 | Bandwidth: 8.08 | Active: DSC x Enabled | V-Total: 1125 | VRate: 60.0 fps
METADATA | Res: 1920 x 1080 | Total: 2200 x 1125 | Sync: 44+, 5+ | Start: 192, 41 | na, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 3395 | Nvid: 32768 | Maud: 512 | Naud: 16875
METADATA | Pixel Clock: 83.700 MHz | DwnSp: on | HDCP-Sync: N | HDCP-Enc: off
```

11.2 Network Analyzer Dashboard

This subsection describes the dashboard components on the top of the Network Analyzer panel. Refer to the table below for a description of these components.

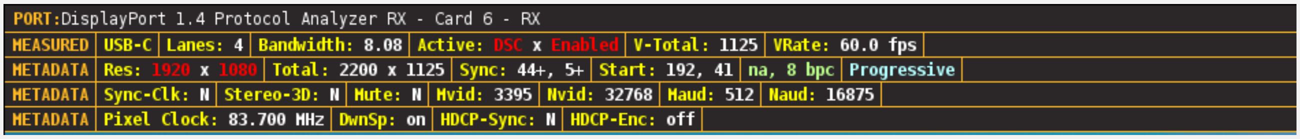
Network Analyzer – Dashboard Items

Example with standard DP Rx port active



```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 3 - RX
MEASURED | Lanes: 4 | Bandwidth: 8.10 | Active: 3840 x 2160 | V-Total: 2222 | VRate: 60.0 fps
METADATA | Res: 3840 x 2160 | Total: 4000 x 2222 | Sync: 32+, 5+ | Start: 112, 59 | CEA RGB, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 21519 | Nvid: 32768 | Maud: 0 | Naud: 0
METADATA | Pixel Clock: 531.93 MHz | DwnSp: off | HDCP-Sync: N | HDCP-Enc: off
```

Example with USB-C DP Alt Mode Rx port active and DSC



```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 6 - RX
MEASURED | USB-C | Lanes: 4 | Bandwidth: 8.08 | Active: DSC x Enabled | V-Total: 1125 | VRate: 60.0 fps
METADATA | Res: 1920 x 1080 | Total: 2200 x 1125 | Sync: 44+, 5+ | Start: 192, 41 | na, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 3395 | Nvid: 32768 | Maud: 512 | Naud: 16875
METADATA | Pixel Clock: 83.700 MHz | DwnSp: on | HDCP-Sync: N | HDCP-Enc: off
```

The following items are on the Real Time dashboard:

Top Row Items – Module and Port:

Network Analyzer – Dashboard Items

- **Port** –The Port area shows the current Rx port that is being displayed on the Network Analyzer.
-  PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 3 - RX. Currently the only analyzer port is the 980 HDMI Video Generator port.

Second Row Items:

- **USB-C**  USB-C - The number of lanes used during link training.
- **Lanes**  Lanes: 4 - The number of lanes used during link training.
- **Bandwidth**  Bandwidth: 8.10 - The lane rate (per lane).
- **Active (video resolution)**  Active: 3840 x 2160 - This is the measured video resolution.

  Note: If DSC is active this will be indicated  Active: DSC x Enabled.
- **V Total**  V-Total: : 1125 - This is the measured total vertical video lines per frame.

Third Row Items:

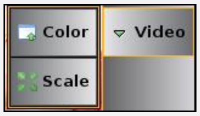
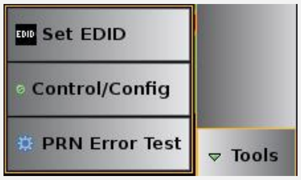
- **Res[olution]**  Active: 3840 x 2160 - The active video resolution in horizontal pixels and vertical lines determined from the main stream attributes.
- **Total (video) pixels and lines**  Total: 4000 x 2222 - The total video in horizontal pixels and vertical lines determined from the main stream attributes.
- **Sync**  Sync: 44+, 5+ - The number of horizontal pixels in the blanking and it polarity (e.g. 44 pixels, positive) and the number of vertical lines in the blanking and its polarity (e.g. 5 lines, positive).
- **Start**  Start: 192, 41 - The starting pixel and line in the active video determined from the main stream attributes.
- **Colorimetry and bit depth**  AdobeRGB 8 bpc - The colorimetry and bit depth determined from the main stream attributes.
- **Scan**  Prog - The scan type used, progressive (e.g. Prog) or interlaced (Inter) determined from the main stream attributes.

Fourth Row Items:

- **Sync -Clk**  Sync-Clk: N - Indicates if the Link Clock and Main Video Stream clock are asynchronous or synchronous. A value of N means async; a value of Y means synchronous. This value is determined by the main stream attributes.
- **Stereo-3D**  Stereo-3D: N - The status of 3D audio determined from the main stream attributes.
- **Mute**  Mute: Y - The AudioMute flag status determined from the main stream attributes.
- **HDCP-Sync**  HDCP-Sync: N - The HDCP sync detect of the Video Blanking VB-ID bits. Y for sync detected; No for HDCP sync not detected.
- **Mvid**  Mvid: 9011 - The Mvid value used for stream clock recovery. This is determined from the main stream attributes.
- **Nvid**  Nvid: 32768 - The Nvid value used for stream clock recovery. This is determined from the main stream attributes.

11.3 Main Control Panel

This subsection describes the main control panel for the Network Analyzer. Refer to the table below for a description of these controls.

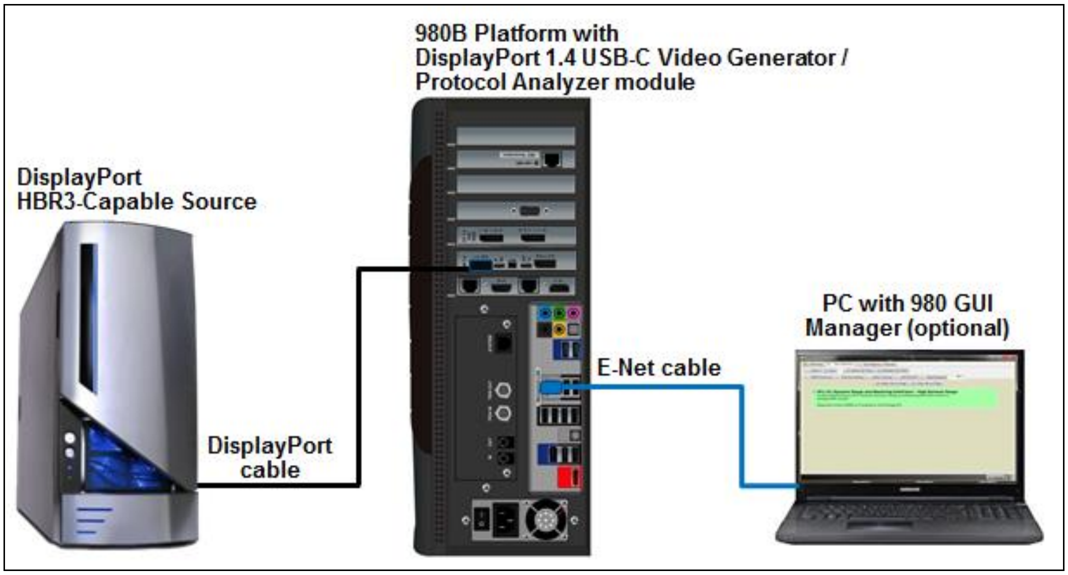
Network Analyzer – Control Panel	**Control Button Descriptions**
Main Control Panel (two views – Active / Inactive) 	The following controls are provided in the main control panel on the right edge of the Real Time mode interface. Each of the buttons have a pull-down menu associated with them. The purpose of each button and their basic control functions are described below: ▪ Home – The Home button is a navigation button that when pressed takes you back to the home screen **Apps** Panel. ▪ Back – The Back button is a navigation button that when pressed takes you back to the previously viewed screen. ▪ Nav – The Nav button when pressed takes you to the navigation panel where you can access various data files. ▪ Port – The Port button enables you to toggle back and forth between the Rx Network Analyzer function of the 980 HDMI Video Generator module and the Rx Real Time view of the 980 HDMI Protocol Analyzer module. ▪ Start/Stop –The Start / Stop button / is used to enable and disable the showing of the incoming video image. ▪ Video – The video button and associated pull-down menu (not shown) is used to display the Video Info panel which provides timing, resolution and other basic information about the incoming video.  ○ Color – The Color button and associated dialog box enables you to identify the color of any particular pixel. ○ Scale – The Scale button and associated dialog box enables you to set the size, quality and aspect ratio of the incoming video image. ▪ Back - The arrow button enables you to toggle between the current view and the previous view. ▪ Mode - The Mode button enables you to toggle HDCP on or off on the 980 HDMI Video Generator's Rx port. ▪ Tools - The Tools button enables you to set the EDID, configure the Tx and Rx ports, view link training status, generate a hot plug with the associated flyout controls and run a pseudo-random noise test on a cable: 

11.4 Connecting a DisplayPort source to the Rx Analyzer port

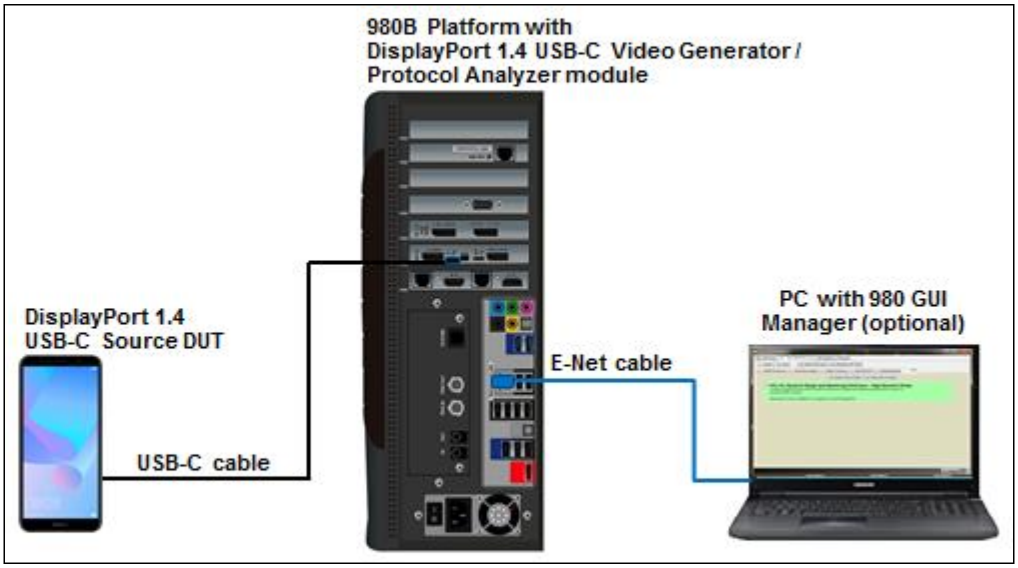
This subsection provides procedures on how to connect to the DP Rx Analyzer.

1. Connect the DP source device to the DP module's Rx Analyzer port as shown below.

   Note the second PC shown is used for the 980 GUI Manager application.



Connection for DP sink emulation – 980B

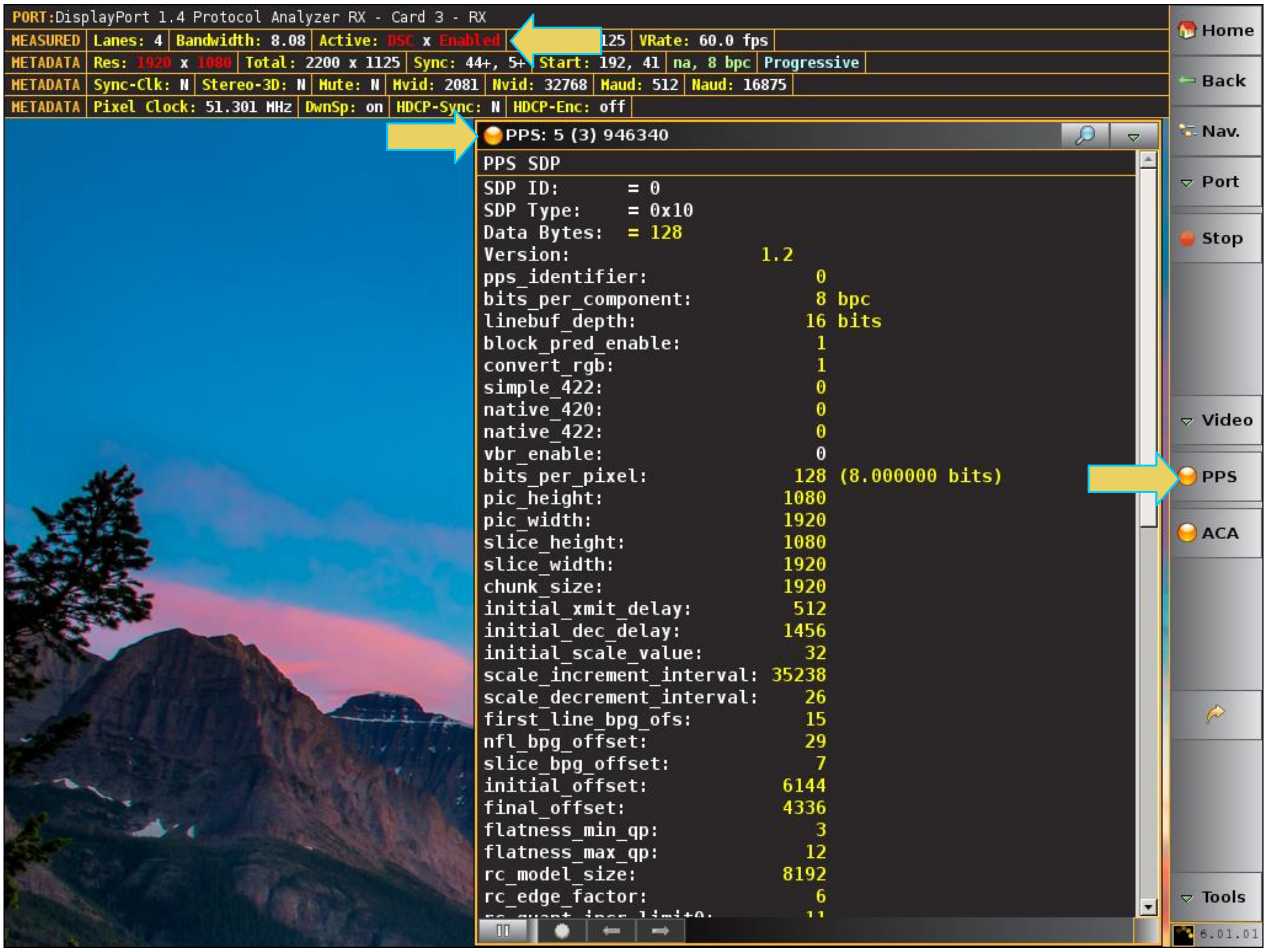


Connection for USB-C DP Alt Mode Sink Emulation

11.5 DSC Real Time (Snapshot) Analysis

If you have purchased the DSC analysis feature you will be able to view the incoming DSC decompressed frame. Along with the DSC video which is presented as a series of snapshots (not “real time”), you will be able to see the DSC metadata in the Picture Parameter Set (PPS). The PPS panel is shown below. It is accessible form the PPS control button on the right side panel (see screen example below). You will see an indication that the video is DSC enabled on the status bar.

Note: The value shown for the Pixel Clock represents the DSC data rate, not the actual pixel rate of the video.



```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 3 - RX
MEASURED | Lanes: 4 | Bandwidth: 8.08 | Active: DSC x Enabled | 125 | VRate: 60.0 fps
METADATA | Res: 1920 x 1080 | Total: 2200 x 1125 | Sync: 44+, 5+ | Start: 192, 41 | na, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 2081 | Nvid: 32768 | Maud: 512 | Naud: 16875
METADATA | Pixel Clock: 51.301 MHz | DwnSp: on | HDCP-Sync: N | HDCP-Enc: off
```

```
PPS: 5 (3) 946340
PPS SDP
SDP ID:       = 0
SDP Type:     = 0x10
Data Bytes:   = 128
Version:                  1.2
pps_identifier:             0
bits_per_component:         8 bpc
linebuf_depth:             16 bits
block_pred_enable:          1
convert_rgb:                1
simple_422:                 0
native_420:                 0
native_422:                 0
vbr_enable:                 0
bits_per_pixel:           128 (8.000000 bits)
pic_height:              1080
pic_width:               1920
slice_height:            1080
slice_width:             1920
chunk_size:              1920
initial_xmit_delay:       512
initial_dec_delay:       1456
initial_scale_value:       32
scale_increment_interval: 35238
scale_decrement_interval:  26
first_line_bpg_ofs:        15
nfl_bpg_offset:            29
slice_bpg_offset:           7
initial_offset:          6144
final_offset:            4336
flatness_min_qp:            3
flatness_max_qp:           12
rc_model_size:           8192
rc_edge_factor:             6
```

11.6 DSC Test CRC Verification

If you have purchased the DSC analysis feature you will be able to verify the Test CRC of the incoming DSC decompressed frame to support test automation on Display Stream Compressed (DSC) frames. The DisplayPort specification requires registers in a DSC-capable sink device for exposing calculated CRCs on the decompressed (“reconstructed”) pixel values. This enables a DSC source developer to acquire an objective verification that their compression engine is working properly. Prior to this, a developer would have to view the compressed image frames received by the 980 DP Protocol Analyzer and subjectively assess the compression through a visual inspection.

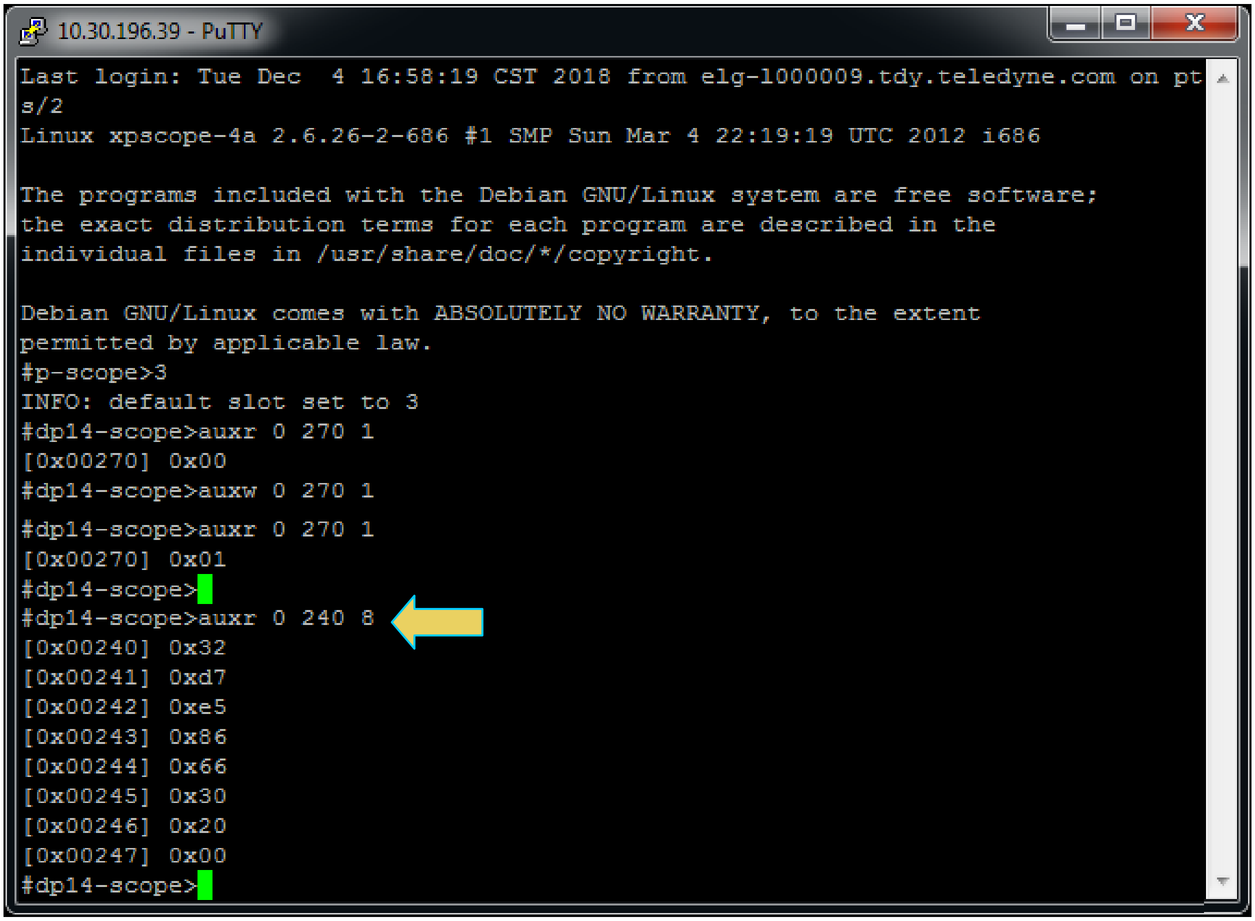
Here is how it works: The source DUT transmits a DSC compressed frame to the DSC sink. The Test CRC registers in the sink (in this case the 980 analyzer emulating a sink) now expose the calculated values to be read by the source, thus enabling the verification. Developers of a DSC-capable source can read these registers over an Aux Channel read through their automated test application to make the verification. Here is an example command sequence.

Use a command terminal program such as Putty.

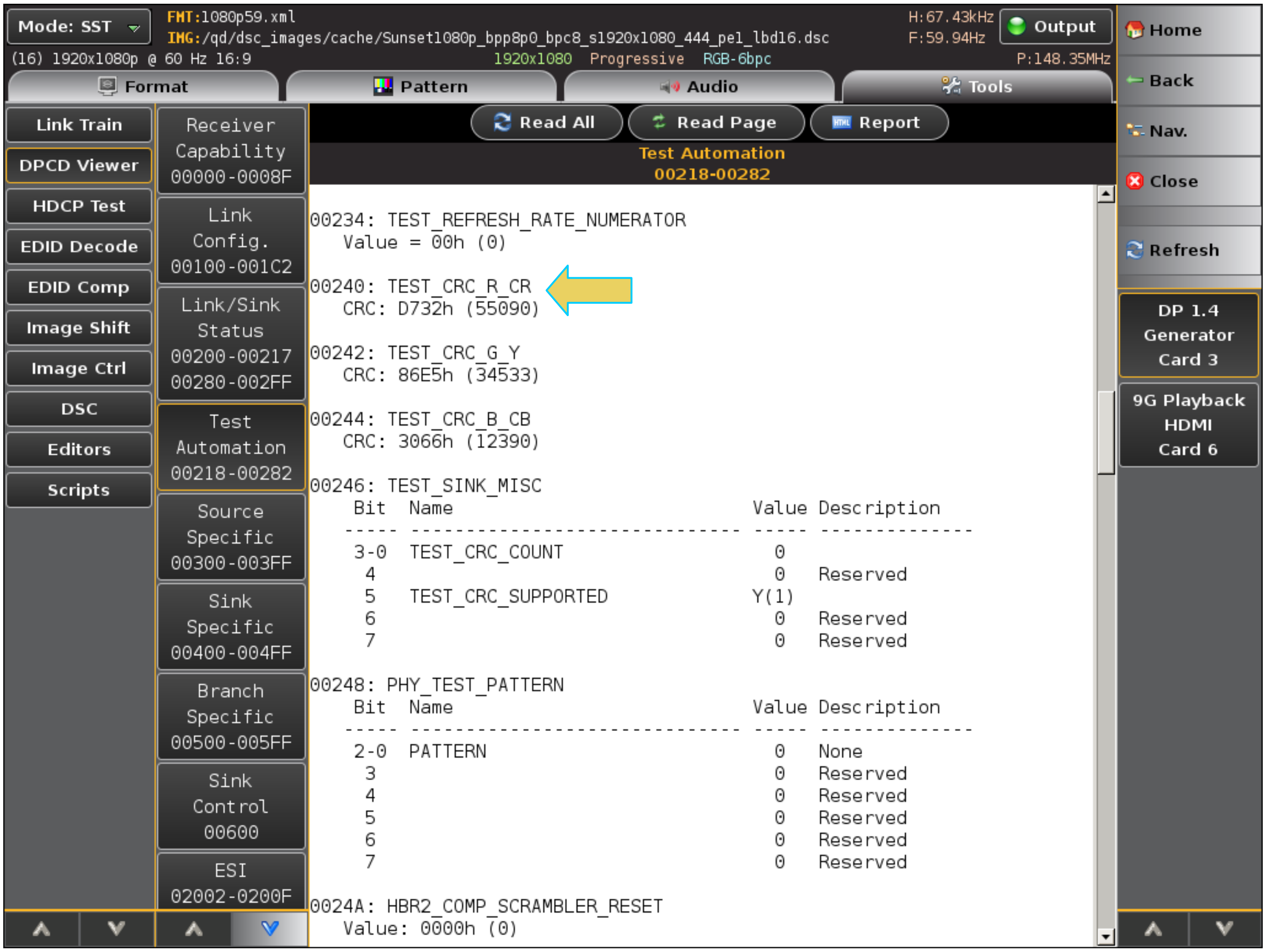
1. Connect via Telnet to the 980B IP address.
2. Log in with username: qd and password: qd.
3. Enter the slot number of the 980 DisplayPort module (example 3).
4. Enter the DPCD read commands over the aux channel using the 980 aux read (auxr) and write (auxw) commands as shown in the Putty terminal session below.

In the example below, the DPCD Test CRC registers are first enabled (write to register 270). Then you read the Test CRC registers (240).

Note: The screen shot following this terminal screen shows the 980 DP 1.4 Video Generator reading these same registers through the DPCD Viewer utility.



```
Last login: Tue Dec  4 16:58:19 CST 2018 from elg-1000009.tdy.teledyne.com on pt
s/2
Linux xpscope-4a 2.6.26-2-686 #1 SMP Sun Mar 4 22:19:19 UTC 2012 i686

The programs included with the Debian GNU/Linux system are free software;
the exact distribution terms for each program are described in the
individual files in /usr/share/doc/*/copyright.

Debian GNU/Linux comes with ABSOLUTELY NO WARRANTY, to the extent
permitted by applicable law.
#p-scope>3
INFO: default slot set to 3
#dp14-scope>auxr 0 270 1
[0x00270] 0x00
#dp14-scope>auxw 0 270 1
#dp14-scope>auxr 0 270 1
[0x00270] 0x01
#dp14-scope>
#dp14-scope>auxr 0 240 8
[0x00240] 0x32
[0x00241] 0xd7
[0x00242] 0xe5
[0x00243] 0x86
[0x00244] 0x66
[0x00245] 0x30
[0x00246] 0x20
[0x00247] 0x00
#dp14-scope>
```



```
00234: TEST_REFRESH_RATE_NUMERATOR
   Value = 00h (0)

00240: TEST_CRC_R_CR
   CRC: D732h (55090)

00242: TEST_CRC_G_Y
   CRC: 86E5h (34533)

00244: TEST_CRC_B_CB
   CRC: 3066h (12390)

00246: TEST_SINK_MISC
    Bit  Name                           Value Description
   ----- ------------------------------ ----- -------------
    3-0  TEST_CRC_COUNT                   0
     4                                    0   Reserved
     5   TEST_CRC_SUPPORTED             Y(1)
     6                                    0   Reserved
     7                                    0   Reserved

00248: PHY_TEST_PATTERN
    Bit  Name                           Value Description
   ----- ------------------------------ ----- -------------
    2-0  PATTERN                          0   None
     3                                    0   Reserved
     4                                    0   Reserved
     5                                    0   Reserved
     6                                    0   Reserved
     7                                    0   Reserved

0024A: HBR2_COMP_SCRAMBLER_RESET
   Value: 0000h (0)
```

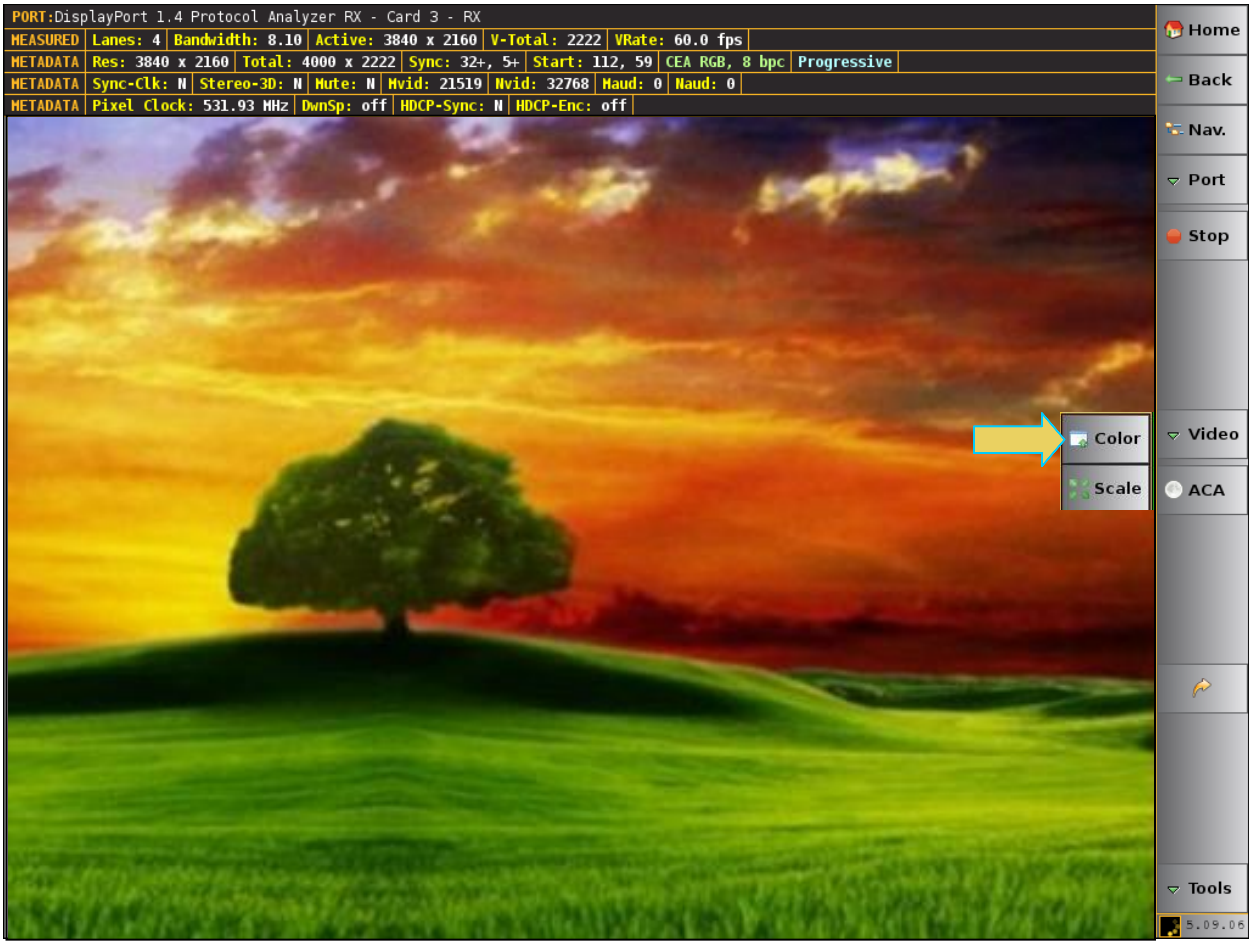
11.7 Controlling the Network Analyzer

This subsection provides procedures on how to control the Network Analyzer features.

11.7.1 Viewing the Color values

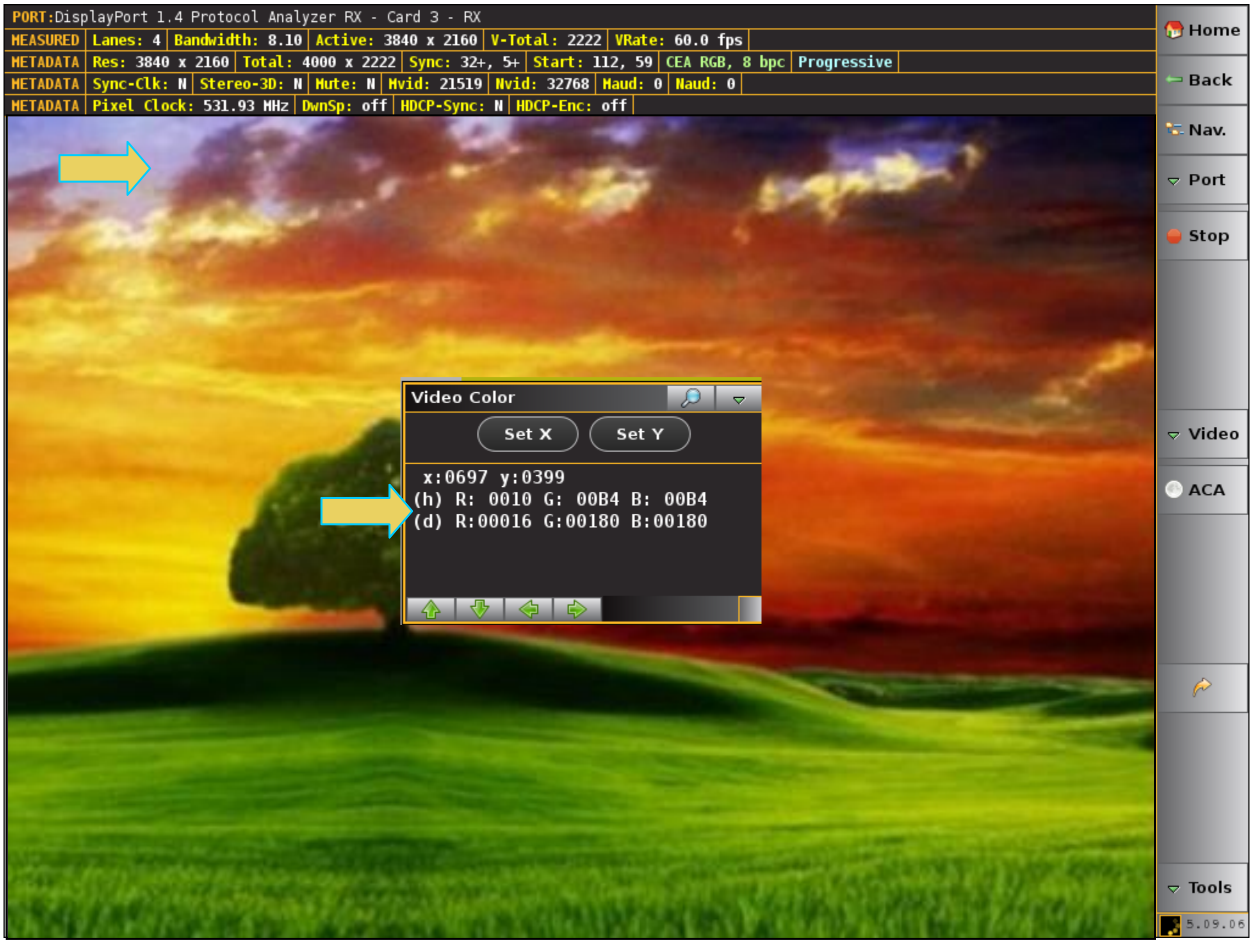
The 980 DP Video Analyzer enables you to determine the color values of any particular pixel.

1. Access the Color dialog box from the Video fly-out menu.



```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 3 - RX
MEASURED | Lanes: 4 | Bandwidth: 8.10 | Active: 3840 x 2160 | V-Total: 2222 | VRate: 60.0 fps
METADATA | Res: 3840 x 2160 | Total: 4000 x 2222 | Sync: 32+, 5+ | Start: 112, 59 | CEA RGB, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 21519 | Nvid: 32768 | Maud: 0 | Naud: 0
METADATA | Pixel Clock: 531.93 MHz | DwnSp: off | HDCP-Sync: N | HDCP-Enc: off
```

2. Move your finger or stylus to a location on the video. You can also move to the adjacent pixels with the green arrow buttons provided in the dialog box.



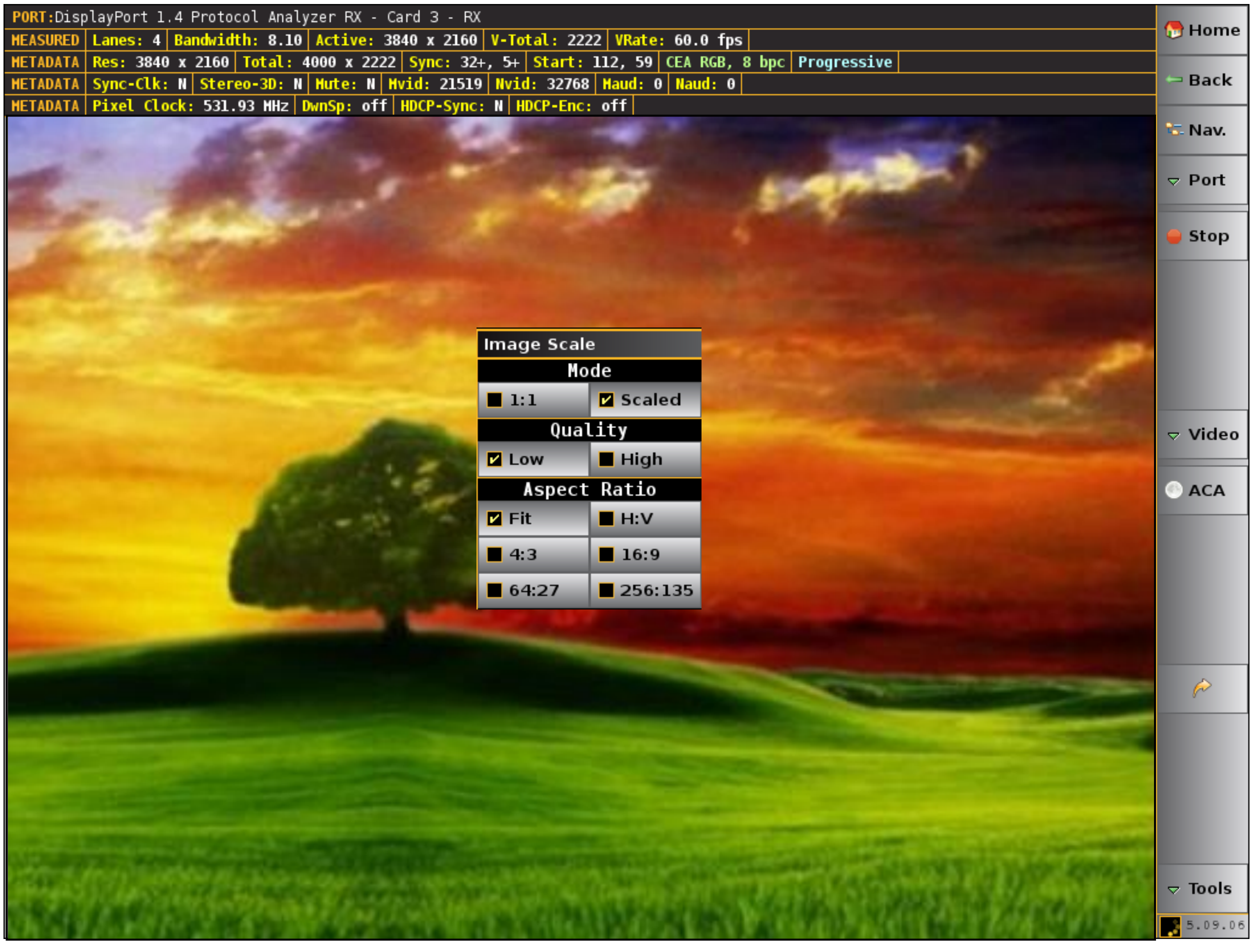
```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 3 - RX
MEASURED | Lanes: 4 | Bandwidth: 8.10 | Active: 3840 x 2160 | V-Total: 2222 | VRate: 60.0 fps
METADATA | Res: 3840 x 2160 | Total: 4000 x 2222 | Sync: 32+, 5+ | Start: 112, 59 | CEA RGB, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 21519 | Nvid: 32768 | Maud: 0 | Naud: 0
METADATA | Pixel Clock: 531.93 MHz | DwnSp: off | HDCP-Sync: N | HDCP-Enc: off
```

```
 x:0697 y:0399
(h) R: 0010 G: 00B4 B: 00B4
(d) R:00016 G:00180 B:00180
```

3. Read the pixel values on the dialog box provided. The pixel values (X for the horizontal – Y for the vertical) are provided in both hex and decimal.

11.7.2 Setting the video image size and aspect ratio

The 980 DP Video Analyzer enables you to set the size and aspect ratio of the incoming video image.



PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 3 - RX

MEASURED | Lanes: 4 | Bandwidth: 8.10 | Active: 3840 x 2160 | V-Total: 2222 | VRate: 60.0 fps

METADATA | Res: 3840 x 2160 | Total: 4000 x 2222 | Sync: 32+, 5+ | Start: 112, 59 | CEA RGB, 8 bpc | Progressive

METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 21519 | Nvid: 32768 | Maud: 0 | Naud: 0

METADATA | Pixel Clock: 531.93 MHz | DwnSp: off | HDCP-Sync: N | HDCP-Enc: off

Image Scale

Mode

☐ 1:1 ☑ Scaled

Quality

☑ Low ☐ High

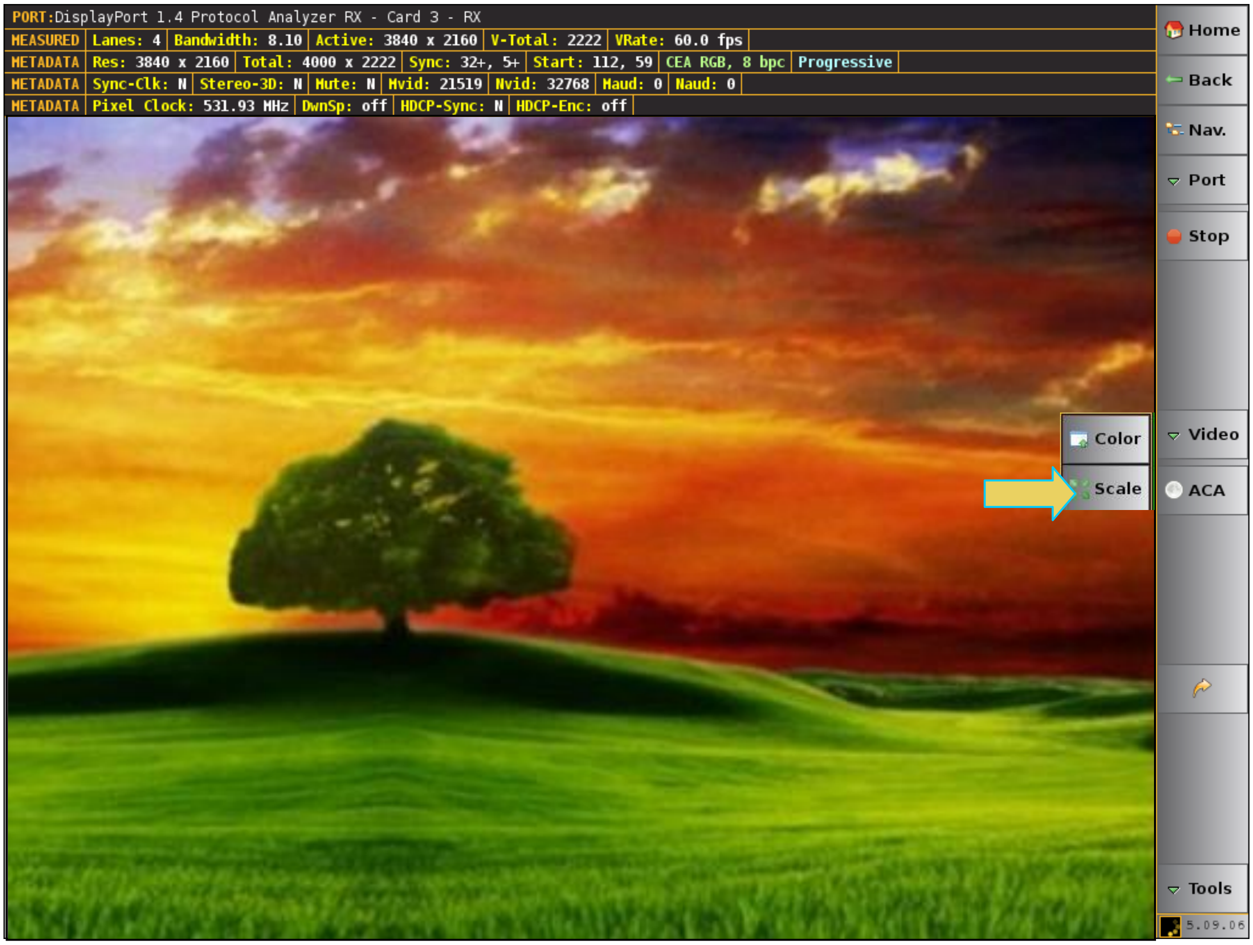
Aspect Ratio

☑ Fit ☐ H:V

☐ 4:3 ☐ 16:9

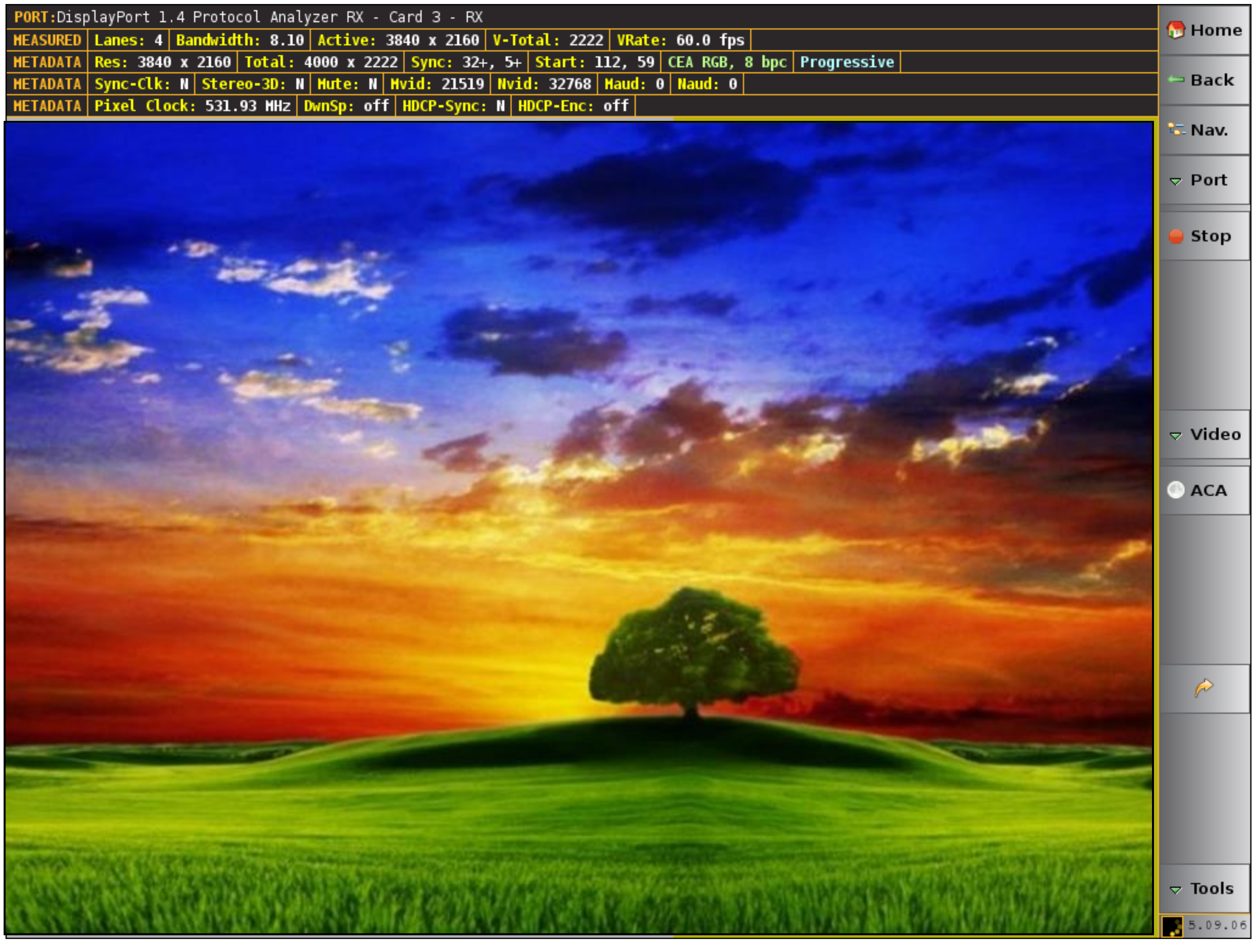
☐ 64:27 ☐ 256:135

1. Access the **Image Scale** dialog box from the Video fly-out menu.



```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 3 - RX
MEASURED | Lanes: 4 | Bandwidth: 8.10 | Active: 3840 x 2160 | V-Total: 2222 | VRate: 60.0 fps
METADATA | Res: 3840 x 2160 | Total: 4000 x 2222 | Sync: 32+, 5+ | Start: 112, 59 | CEA RGB, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 21519 | Nvid: 32768 | Maud: 0 | Naud: 0
METADATA | Pixel Clock: 531.93 MHz | DwnSp: off | HDCP-Sync: N | HDCP-Enc: off
```

The example below shows Image Scale set to Scaled.



```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 3 - RX
MEASURED | Lanes: 4 | Bandwidth: 8.10 | Active: 3840 x 2160 | V-Total: 2222 | VRate: 60.0 fps
METADATA | Res: 3840 x 2160 | Total: 4000 x 2222 | Sync: 32+, 5+ | Start: 112, 59 | CEA RGB, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 21519 | Nvid: 32768 | Maud: 0 | Naud: 0
METADATA | Pixel Clock: 531.93 MHz | DwnSp: off | HDCP-Sync: N | HDCP-Enc: off
```

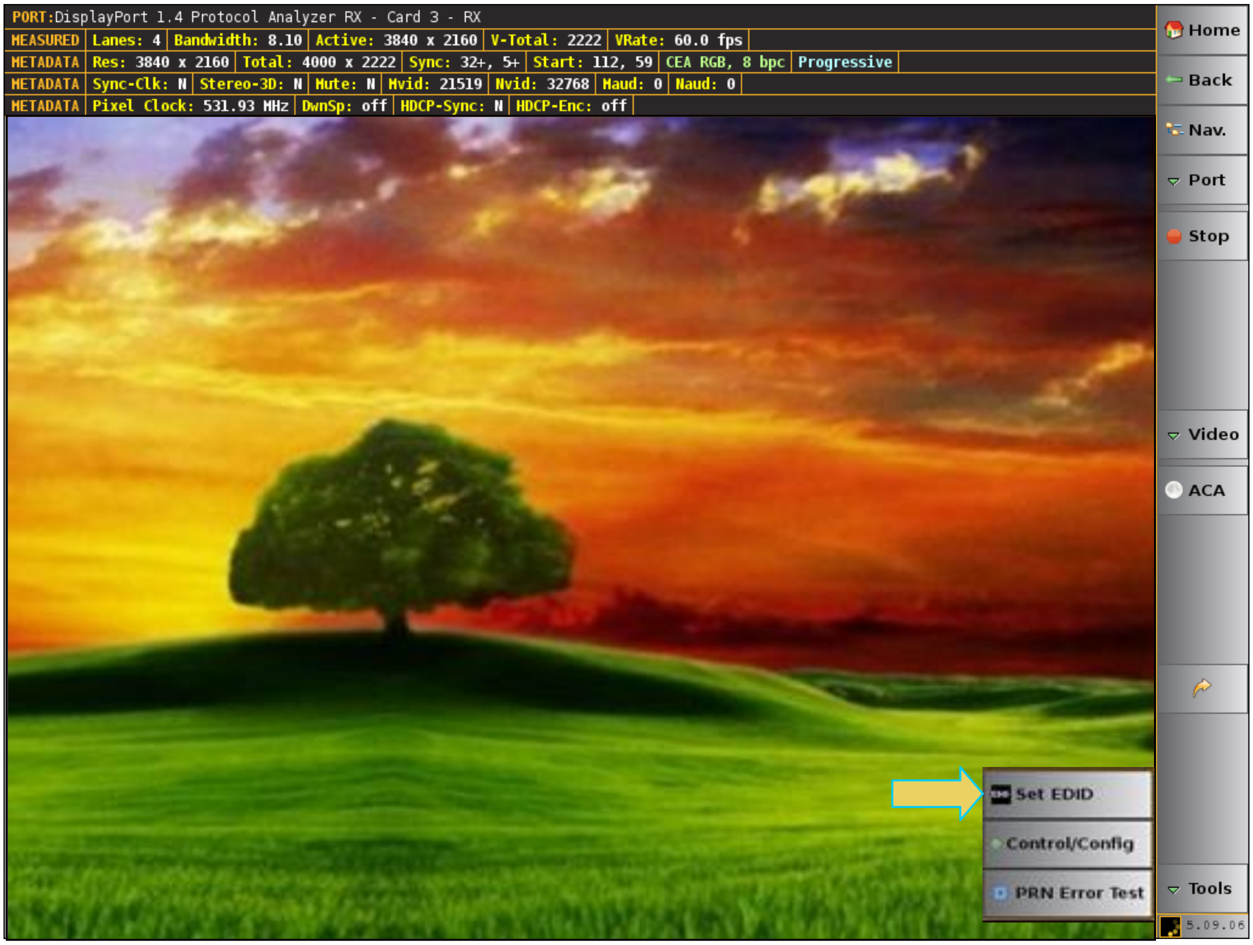
2. Set the size to either 1:1 or Scaled. The 1:1 setting means that the image appears in its true size. In this mode the image can be moved by dragging to view all areas of the image. The Scaled setting means that the image appears scaled to fit within the viewing area of the 980's embedded display.

   Note: In order to set the Quality and the Aspect Ratio you have to set the size to 1:1.

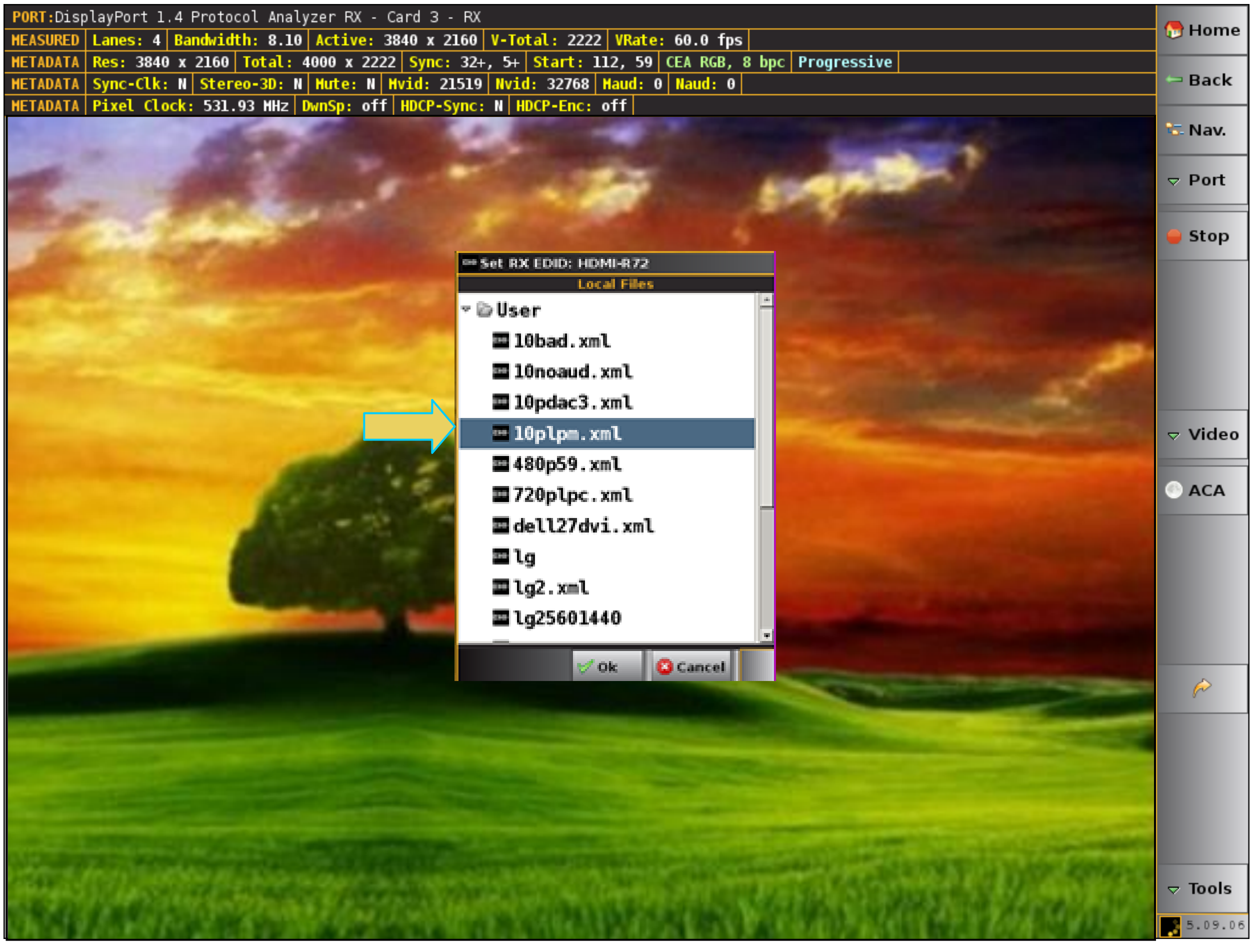
11.7.3 Setting the EDID for the Rx port

The 980 DP Video Analyzer enables you to set Rx ports EDID for emulation. The 980 GUI provides an EDID Editor enabling you to create your own custom EDIDs. You can also capture EDIDs from the 980 DP Video Generator's Tx ports and save them for testing on the Rx port. Also note that Quantum Data provides a free EDID Library available at: http://www.quantumdata.com/edid/.

1. Access the Set EDID dialog box from the Tools fly-out menu.



```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 3 - RX
MEASURED | Lanes: 4 | Bandwidth: 8.10 | Active: 3840 x 2160 | V-Total: 2222 | VRate: 60.0 fps
METADATA | Res: 3840 x 2160 | Total: 4000 x 2222 | Sync: 32+, 5+ | Start: 112, 59 | CEA RGB, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 21519 | Nvid: 32768 | Maud: 0 | Naud: 0
METADATA | Pixel Clock: 531.93 MHz | DwnSp: off | HDCP-Sync: N | HDCP-Enc: off
```



```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 3 - RX
MEASURED | Lanes: 4 | Bandwidth: 8.10 | Active: 3840 x 2160 | V-Total: 2222 | VRate: 60.0 fps
METADATA | Res: 3840 x 2160 | Total: 4000 x 2222 | Sync: 32+, 5+ | Start: 112, 59 | CEA RGB, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 21519 | Nvid: 32768 | Maud: 0 | Naud: 0
METADATA | Pixel Clock: 531.93 MHz | DwnSp: off | HDCP-Sync: N | HDCP-Enc: off
```

2. Select the EDID that you wish to emulate on the module's Rx port and then click on OK.

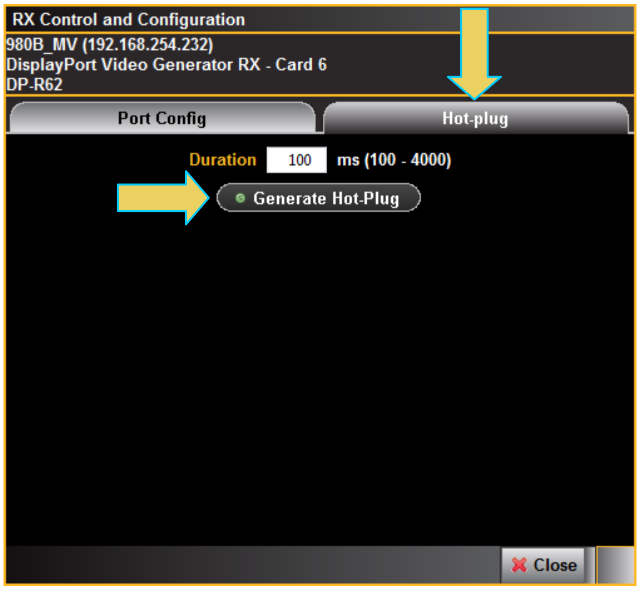
   The 980 DP Video Generator's Rx port will emulate the EDID you selected.

   Refer to the section in the User Guide entitled Capturing EDIDs of a connected display for instructions on how to capture EDIDs from HDTVs.

11.7.4 Generating Hot Plug

The 980 DP Video Analyzer enables you to generate a hot plug to cause a source device to read and EDID and initiate HDCP authentication.

1. Initiate a hot plug from the Tools fly-out menu.
2. Select the Hot Plug tab and click on the Generate Hot Plug activation button to initiate a hot plug. Refer to the dialog box below.

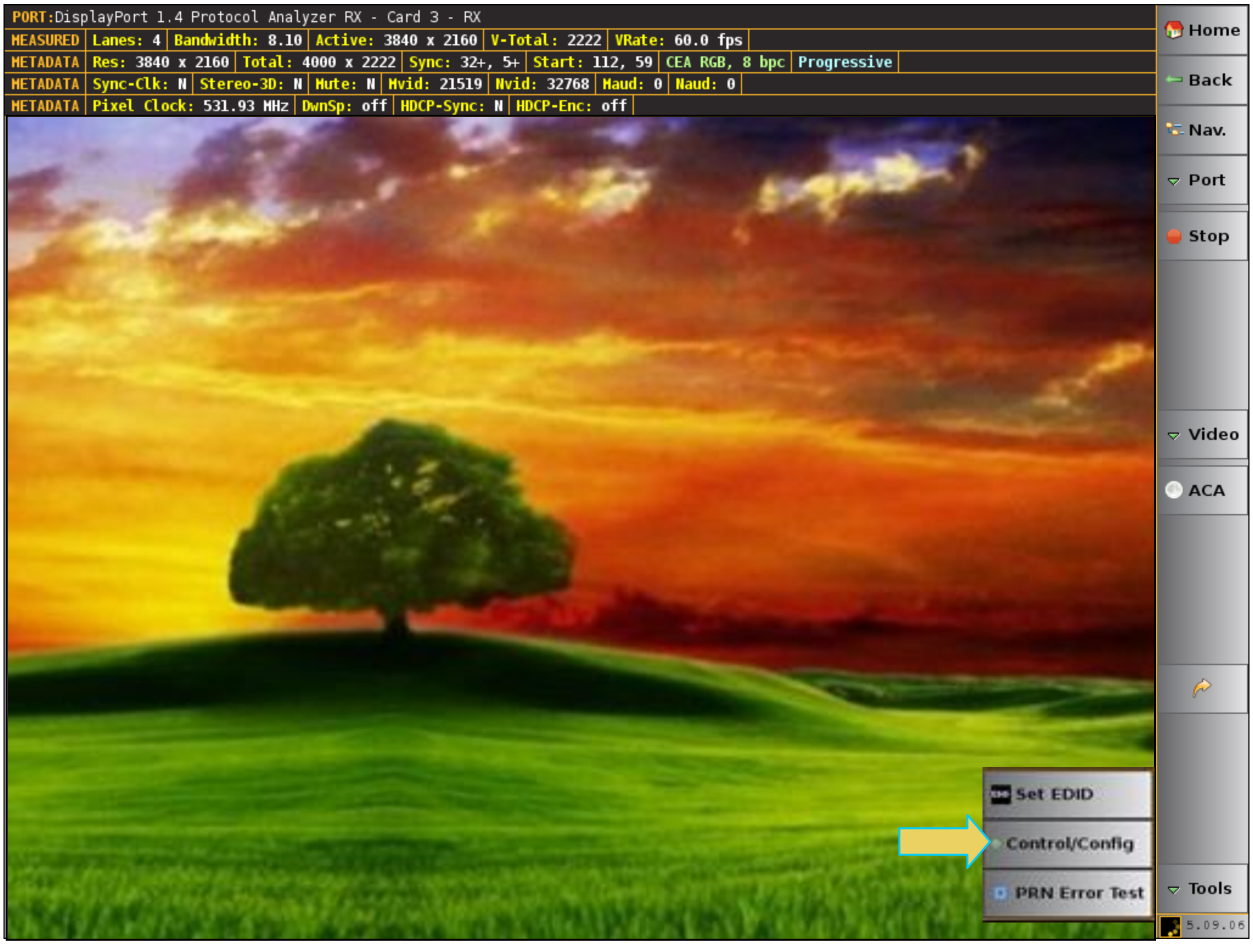


11.8 Emulating an MST Rx port

The 980 DP Video Generator / Analyzer module’s Basic Analyzer option can emulate a DisplayPort Multi-Stream Transport (MST) branch device and MST sinks nodes. The emulation capability includes the ability to present EDIDs from downstream MST sink devices and to provide a response to DPCD reads. The DP Video Analyzer Rx port will respond to MST negotiation requests from MST-capable DP source devices. Currently the EDID presented will be the same for all downstream MST sink nodes. All DPCD reads will be NAKed.

To enable MST emulation:

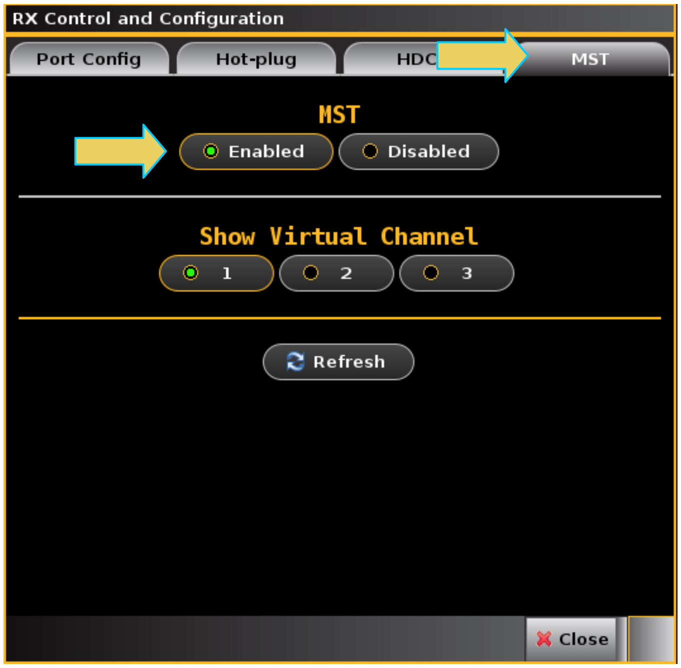
1. Select **Control/Config** from the Tools flyout menu as shown below.



```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 3 - RX
MEASURED | Lanes: 4 | Bandwidth: 8.10 | Active: 3840 x 2160 | V-Total: 2222 | VRate: 60.0 fps
METADATA | Res: 3840 x 2160 | Total: 4000 x 2222 | Sync: 32+, 5+ | Start: 112, 59 | CEA RGB, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 21519 | Nvid: 32768 | Maud: 0 | Naud: 0
METADATA | Pixel Clock: 531.93 MHz | DwnSp: off | HDCP-Sync: N | HDCP-Enc: off
```

The **Rx Control and Configuration** menu appears as shown below.

2. Access the MST tab from the **Rx Control and Configuration** dialog box as shown below.



RX Control and Configuration

MST

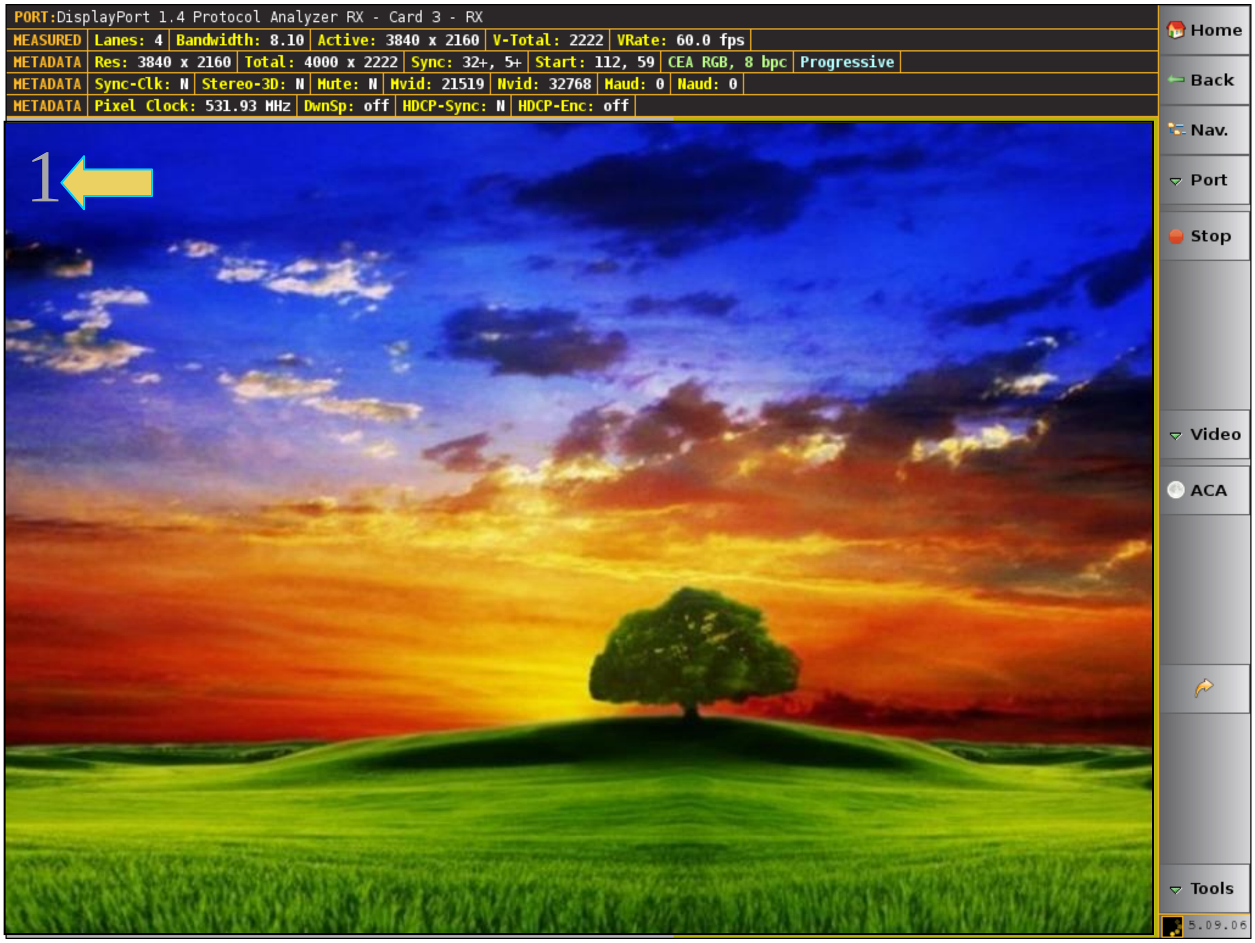
● Enabled ○ Disabled

Show Virtual Channel

● 1 ○ 2 ○ 3

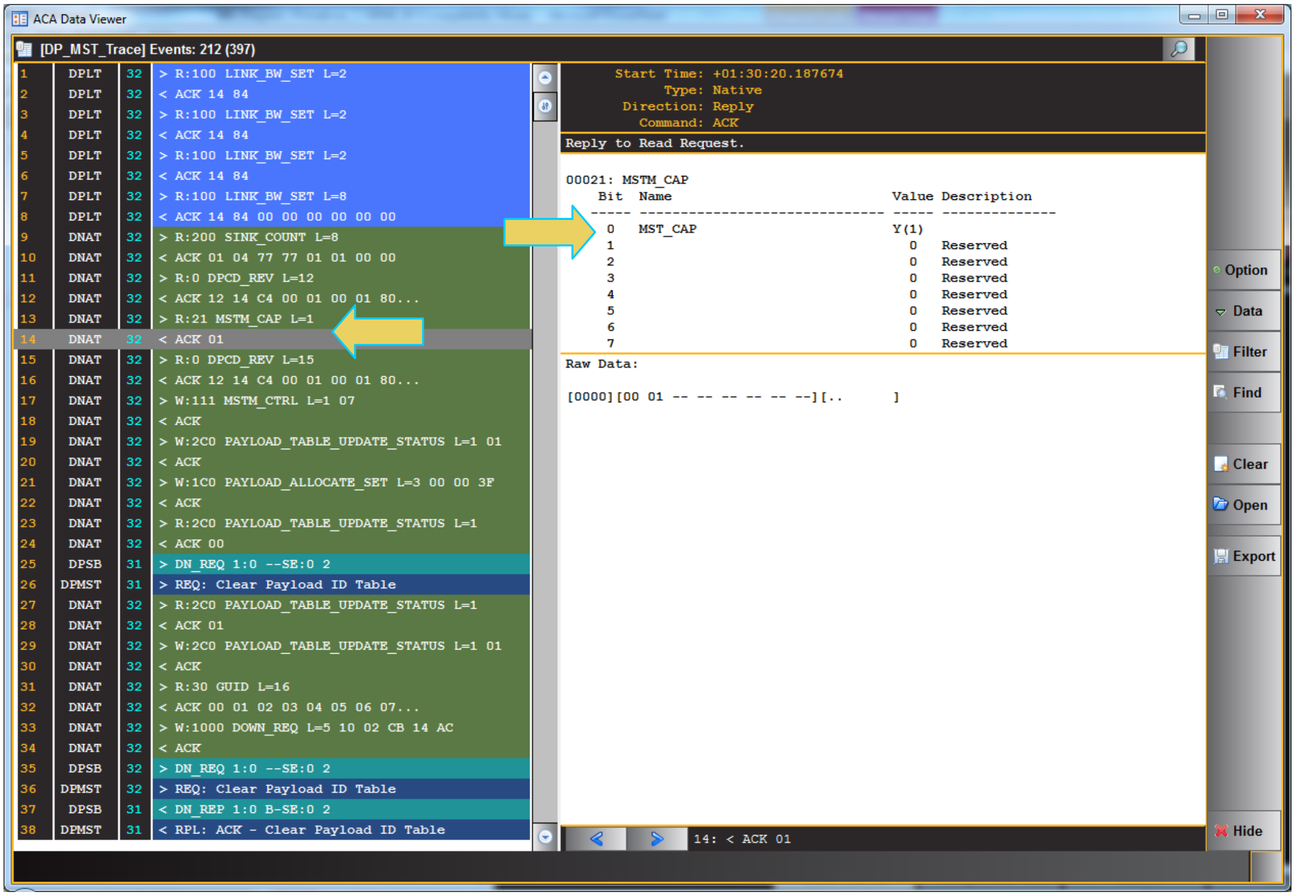
3. Enable MST and select the virtual channel to show on the Real Time display.

   In the example above, the video from MST stream 1 would appear on the 980 Real Time display window. The example below shows a special case where the 980 DP module Tx is looped back to the module's Rx port. In this case the module's Tx MST emulator places a 1 (or 2,3,4) in the upper left of the video.



```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 3 - RX
MEASURED | Lanes: 4 | Bandwidth: 8.10 | Active: 3840 x 2160 | V-Total: 2222 | VRate: 60.0 fps
METADATA | Res: 3840 x 2160 | Total: 4000 x 2222 | Sync: 32+, 5+ | Start: 112, 59 | CEA RGB, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 21519 | Nvid: 32768 | Maud: 0 | Naud: 0
METADATA | Pixel Clock: 531.93 MHz | DwnSp: off | HDCP-Sync: N | HDCP-Enc: off
```

Note: You can also monitor the MST sideband negotiations from the Quantum Data ACA utility as shown in the example below.



```
[DP_MST_Trace] Events: 212 (397)
1   DPLT   32  > R:100 LINK_BW_SET L=2
2   DPLT   32  < ACK 14 84
3   DPLT   32  > R:100 LINK_BW_SET L=2
4   DPLT   32  < ACK 14 84
5   DPLT   32  > R:100 LINK_BW_SET L=2
6   DPLT   32  < ACK 14 84
7   DPLT   32  > R:100 LINK_BW_SET L=8
8   DPLT   32  < ACK 14 84 00 00 00 00 00 00
9   DNAT   32  > R:200 SINK_COUNT L=8
10  DNAT   32  < ACK 01 04 77 77 01 01 00 00
11  DNAT   32  > R:0 DPCD_REV L=12
12  DNAT   32  < ACK 12 14 C4 00 01 00 01 80...
13  DNAT   32  > R:21 MSTM_CAP L=1
14  DNAT   32  < ACK 01
15  DNAT   32  > R:0 DPCD_REV L=15
16  DNAT   32  < ACK 12 14 C4 00 01 00 01 80...
17  DNAT   32  > W:111 MSTM_CTRL L=1 07
18  DNAT   32  < ACK
19  DNAT   32  > W:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1 01
20  DNAT   32  < ACK
21  DNAT   32  > W:1C0 PAYLOAD_ALLOCATE_SET L=3 00 00 3F
22  DNAT   32  < ACK
23  DNAT   32  > R:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1
24  DNAT   32  < ACK 00
25  DPSB   31  > DN_REQ 1:0 --SE:0 2
26  DPMST  31  > REQ: Clear Payload ID Table
27  DNAT   32  > R:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1
28  DNAT   32  < ACK 01
29  DNAT   32  > W:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1 01
30  DNAT   32  < ACK
31  DNAT   32  > R:30 GUID L=16
32  DNAT   32  < ACK 00 01 02 03 04 05 06 07...
33  DNAT   32  > W:1000 DOWN_REQ L=5 10 02 CB 14 AC
34  DNAT   32  < ACK
35  DPSB   32  > DN_REQ 1:0 --SE:0 2
36  DPMST  32  > REQ: Clear Payload ID Table
37  DPSB   31  < DN_REP 1:0 B-SE:0 2
38  DPMST  31  < RPL: ACK - Clear Payload ID Table
```

```
     Start Time: +01:30:20.187674
           Type: Native
      Direction: Reply
        Command: ACK
Reply to Read Request.

00021: MSTM_CAP
    Bit  Name                           Value Description
   ----- ------------------------------ ----- -------------
     0   MST_CAP                        Y(1)
     1                                    0   Reserved
     2                                    0   Reserved
     3                                    0   Reserved
     4                                    0   Reserved
     5                                    0   Reserved
     6                                    0   Reserved
     7                                    0   Reserved
Raw Data:

[0000][00 01 -- -- -- -- -- --][..      ]
```

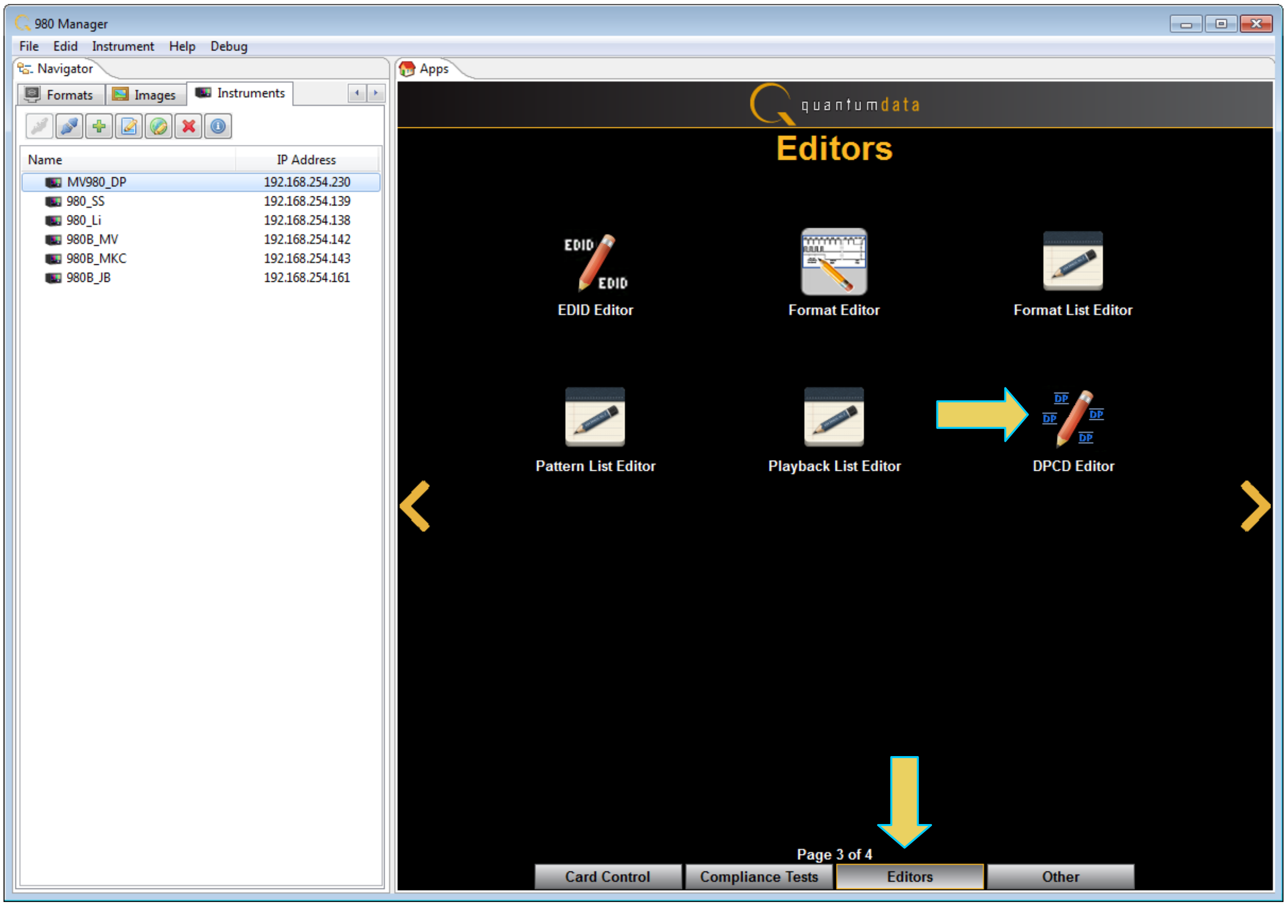
```
14: < ACK 01
```

11.9 DPCD Editor

This subsection provides procedures on how to edit the DP Rx analyzer port's DPCD registers. The 980 DP Video Analyzer provides a set of dialog boxes that enable you to edit the DPCD registers through pull down menus and text fields. You can save these edited configurations for recall when testing DP sources. This enables you to emulate a variety of DPCD register configurations on the Rx port.

The DPCD Editor is available either on the remote GUI or the embedded GUI.

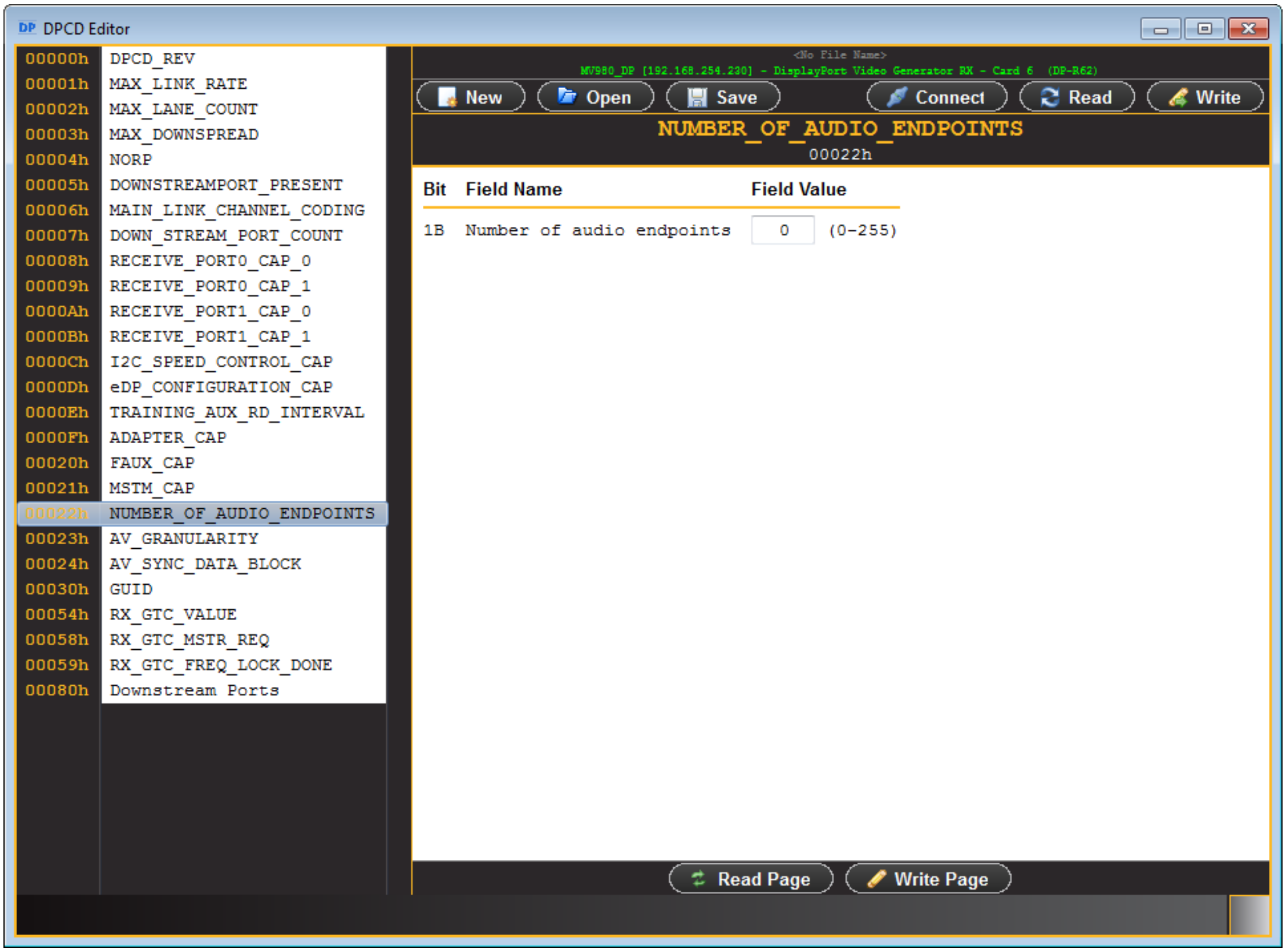
1. Access the DPCD Editor from the Editors page.



Name	IP Address
MV980_DP	192.168.254.230
980_SS	192.168.254.139
980_Li	192.168.254.138
980B_MV	192.168.254.142
980B_MKC	192.168.254.143
980B_JB	192.168.254.161

The following sample screen shots show some of the DPCD editing windows. Note that each register set is selected on the left and the editing tools are available on the main area of the dialog box on the right side.

The following screen shows the DPCD Editor main screen.



<No File Name>
MV980_DP [192.168.254.230] - DisplayPort Video Generator RX - Card 6 (DP-R62)

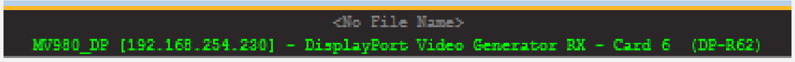
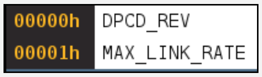
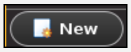
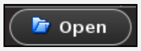
00000h	DPCD_REV
00001h	MAX_LINK_RATE
00002h	MAX_LANE_COUNT
00003h	MAX_DOWNSPREAD
00004h	NORP
00005h	DOWNSTREAMPORT_PRESENT
00006h	MAIN_LINK_CHANNEL_CODING
00007h	DOWN_STREAM_PORT_COUNT
00008h	RECEIVE_PORT0_CAP_0
00009h	RECEIVE_PORT0_CAP_1
0000Ah	RECEIVE_PORT1_CAP_0
0000Bh	RECEIVE_PORT1_CAP_1
0000Ch	I2C_SPEED_CONTROL_CAP
0000Dh	eDP_CONFIGURATION_CAP
0000Eh	TRAINING_AUX_RD_INTERVAL
0000Fh	ADAPTER_CAP
00020h	FAUX_CAP
00021h	MSTM_CAP
00022h	NUMBER_OF_AUDIO_ENDPOINTS
00023h	AV_GRANULARITY
00024h	AV_SYNC_DATA_BLOCK
00030h	GUID
00054h	RX_GTC_VALUE
00058h	RX_GTC_MSTR_REQ
00059h	RX_GTC_FREQ_LOCK_DONE
00080h	Downstream Ports

NUMBER_OF_AUDIO_ENDPOINTS
00022h

Bit	Field Name	Field Value	
1B	Number of audio endpoints	0	(0-255)

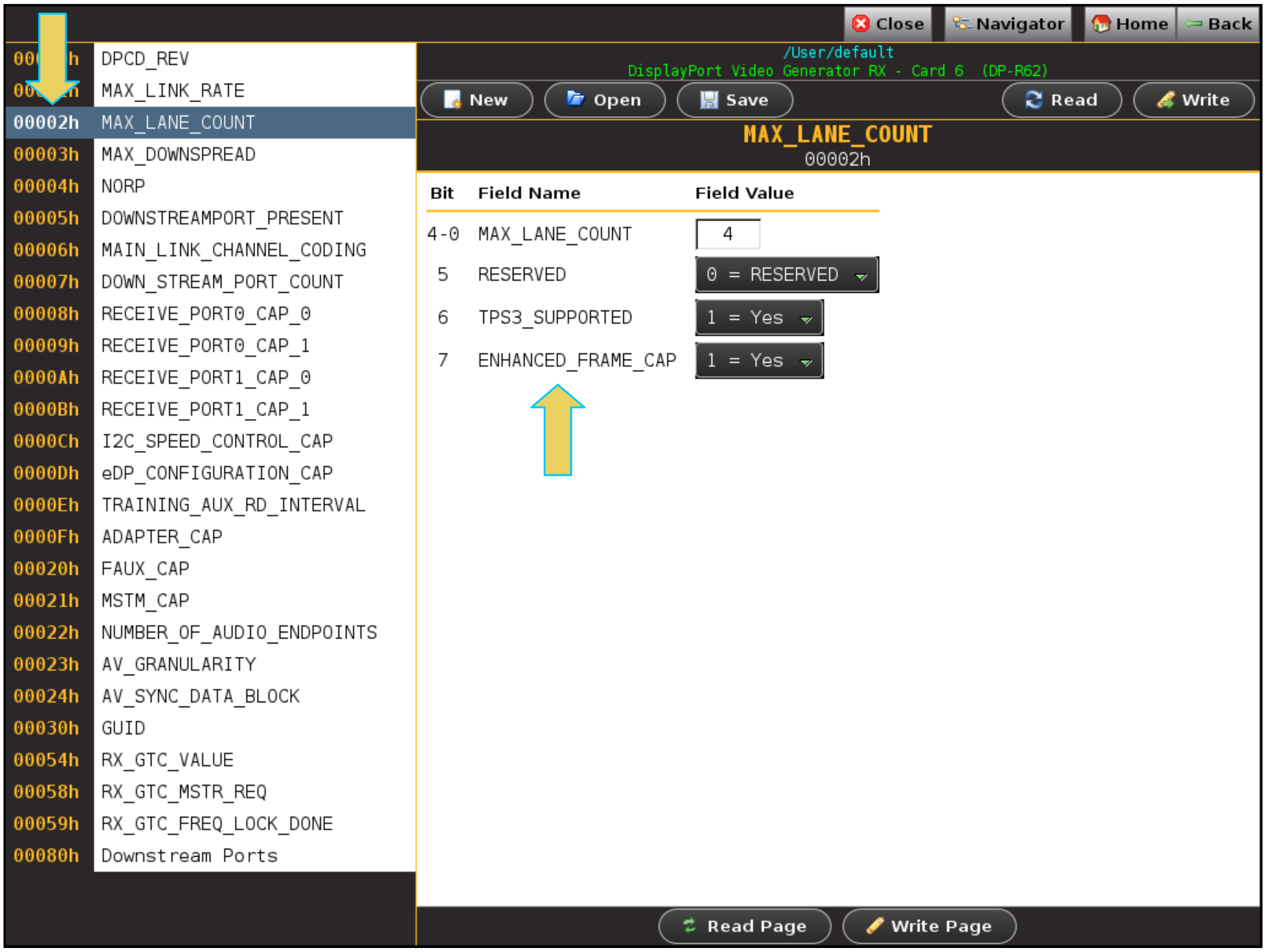
There are a set of controls available with the DPCD Editor. These are defined in the table below:

DPCD Editor controls

Item	Description
Status Text Area	Indicates the current directory where the edited DPCD registers will be stored and opened from. Also, when using the external 980 GUI Manager from a host PC and connecting to a 980 system, this text area shows the IP address of the 980 system that the external 980 GUI Manager is connected to.  <No File Name> MV980_DP [192.168.254.230] - DisplayPort Video Generator RX - Card 6 (DP-R62)
	DP module description indicating the card slot location. Example slot 6.
Register Address  00000h DPCD_REV 00001h MAX_LINK_RATE	Shows the various DPCD register blocks and enables selection of them for editing their contents.
New 	Enables you to create a new file for editing. A dialog box will appear enabling you to assign a name to the DPCD file.
Open 	Enables you to open a DPCD configuration file for editing.

DPCD Editor controls	
Item	**Description**
Connect	Available only from the External 980 GUI Manager (not shown on the embedded GUI). Enables you to connect to a particular 980 system from the External GUI Manager.
Save	Enables you to save a DPCD configuration file for later reuse. A dialog box will appear enabling you to assign a name to the DPCD file.
Read	Enables you to read the entire current DPCD configuration of the 980 DP Rx device. This populates the dialog boxes with the current register settings.
Write	This writes the entire contents of the edited DPCD file to the 980 DP module's Rx port for emulation.
Read Page	Enables you to read the DPCD register values of the selected page of the 980 DP Rx device. This populates dialog boxes with the current register settings.
Write Page	This writes the contents of the register values on the selected page of the DPCD to the 980 DP module's Rx port for emulation.

The following screen examples show several of the DPCD Editor's address blocks (pages).

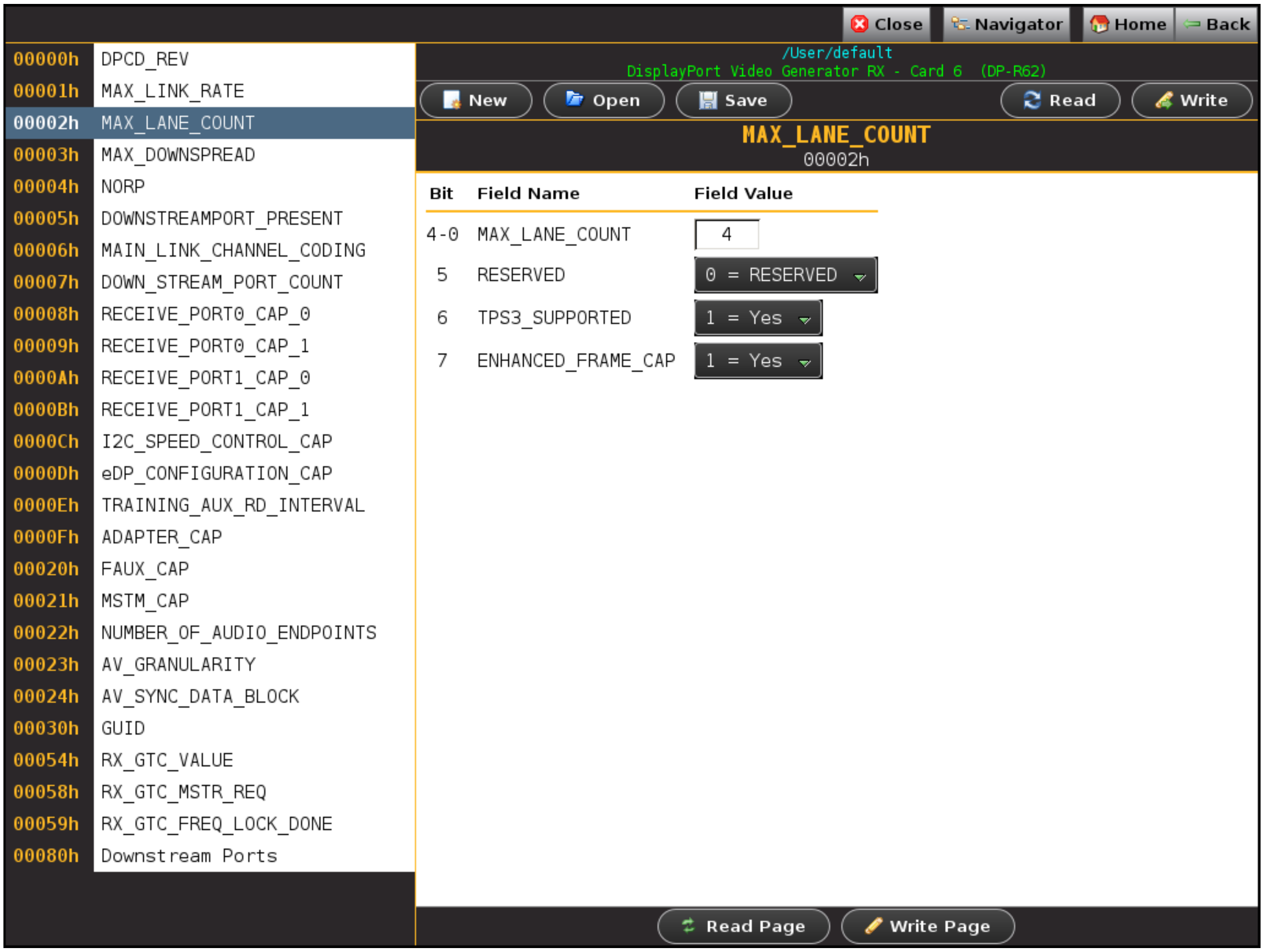


/User/default
DisplayPort Video Generator RX - Card 6 (DP-R62)

00 h	DPCD_REV
00 h	MAX_LINK_RATE
00002h	MAX_LANE_COUNT
00003h	MAX_DOWNSPREAD
00004h	NORP
00005h	DOWNSTREAMPORT_PRESENT
00006h	MAIN_LINK_CHANNEL_CODING
00007h	DOWN_STREAM_PORT_COUNT
00008h	RECEIVE_PORT0_CAP_0
00009h	RECEIVE_PORT0_CAP_1
0000Ah	RECEIVE_PORT1_CAP_0
0000Bh	RECEIVE_PORT1_CAP_1
0000Ch	I2C_SPEED_CONTROL_CAP
0000Dh	eDP_CONFIGURATION_CAP
0000Eh	TRAINING_AUX_RD_INTERVAL
0000Fh	ADAPTER_CAP
00020h	FAUX_CAP
00021h	MSTM_CAP
00022h	NUMBER_OF_AUDIO_ENDPOINTS
00023h	AV_GRANULARITY
00024h	AV_SYNC_DATA_BLOCK
00030h	GUID
00054h	RX_GTC_VALUE
00058h	RX_GTC_MSTR_REQ
00059h	RX_GTC_FREQ_LOCK_DONE
00080h	Downstream Ports

MAX_LANE_COUNT
00002h

Bit	Field Name	Field Value
4-0	MAX_LANE_COUNT	4
5	RESERVED	0 = RESERVED
6	TPS3_SUPPORTED	1 = Yes
7	ENHANCED_FRAME_CAP	1 = Yes

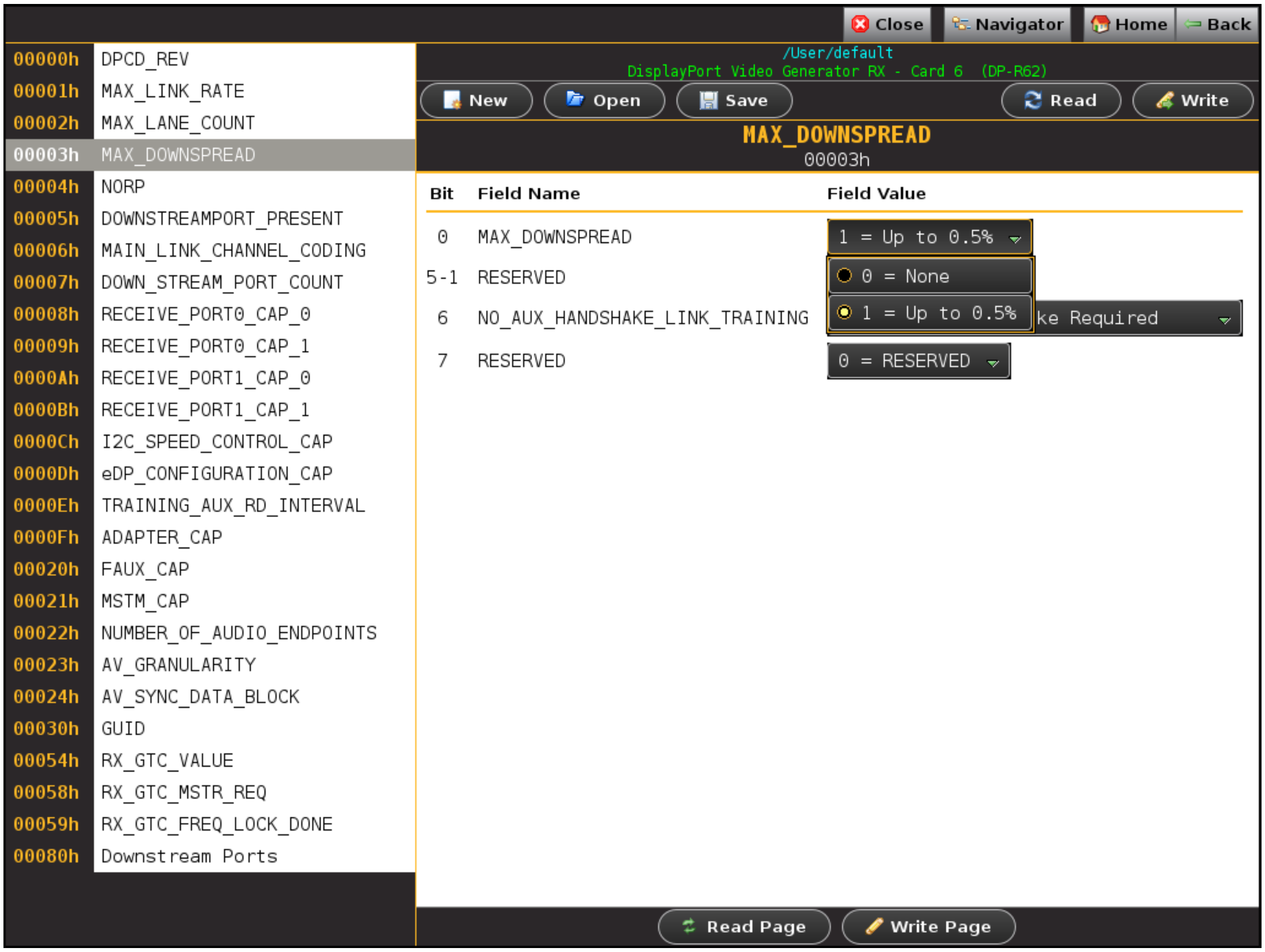


00000h	DPCD_REV
00001h	MAX_LINK_RATE
00002h	MAX_LANE_COUNT
00003h	MAX_DOWNSPREAD
00004h	NORP
00005h	DOWNSTREAMPORT_PRESENT
00006h	MAIN_LINK_CHANNEL_CODING
00007h	DOWN_STREAM_PORT_COUNT
00008h	RECEIVE_PORT0_CAP_0
00009h	RECEIVE_PORT0_CAP_1
0000Ah	RECEIVE_PORT1_CAP_0
0000Bh	RECEIVE_PORT1_CAP_1
0000Ch	I2C_SPEED_CONTROL_CAP
0000Dh	eDP_CONFIGURATION_CAP
0000Eh	TRAINING_AUX_RD_INTERVAL
0000Fh	ADAPTER_CAP
00020h	FAUX_CAP
00021h	MSTM_CAP
00022h	NUMBER_OF_AUDIO_ENDPOINTS
00023h	AV_GRANULARITY
00024h	AV_SYNC_DATA_BLOCK
00030h	GUID
00054h	RX_GTC_VALUE
00058h	RX_GTC_MSTR_REQ
00059h	RX_GTC_FREQ_LOCK_DONE
00080h	Downstream Ports

/User/default
DisplayPort Video Generator RX - Card 6 (DP-R62)

MAX_LANE_COUNT
00002h

Bit	Field Name	Field Value
4-0	MAX_LANE_COUNT	4
5	RESERVED	0 = RESERVED
6	TPS3_SUPPORTED	1 = Yes
7	ENHANCED_FRAME_CAP	1 = Yes

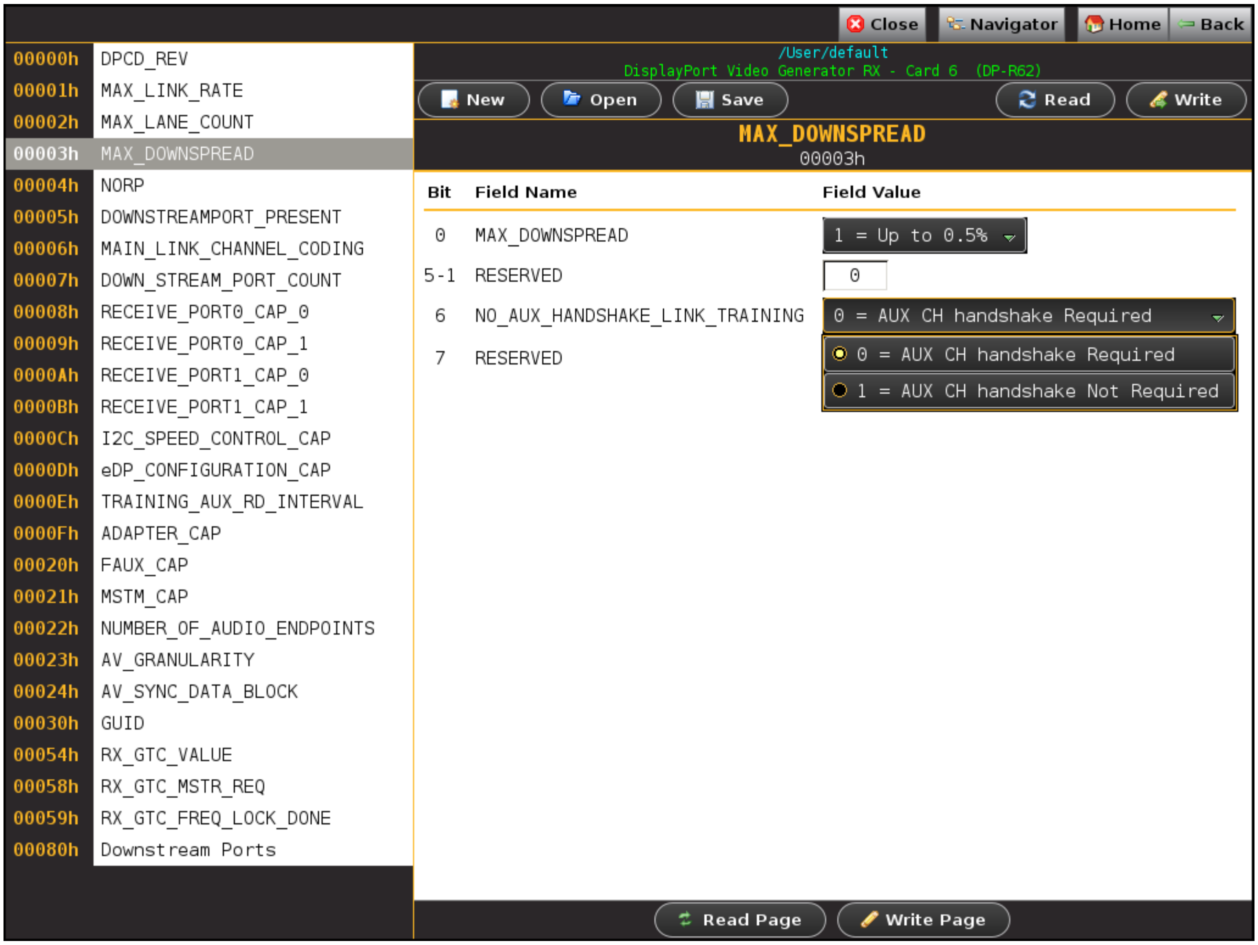


/User/default
DisplayPort Video Generator RX - Card 6 (DP-R62)

00000h	DPCD_REV
00001h	MAX_LINK_RATE
00002h	MAX_LANE_COUNT
00003h	MAX_DOWNSPREAD
00004h	NORP
00005h	DOWNSTREAMPORT_PRESENT
00006h	MAIN_LINK_CHANNEL_CODING
00007h	DOWN_STREAM_PORT_COUNT
00008h	RECEIVE_PORT0_CAP_0
00009h	RECEIVE_PORT0_CAP_1
0000Ah	RECEIVE_PORT1_CAP_0
0000Bh	RECEIVE_PORT1_CAP_1
0000Ch	I2C_SPEED_CONTROL_CAP
0000Dh	eDP_CONFIGURATION_CAP
0000Eh	TRAINING_AUX_RD_INTERVAL
0000Fh	ADAPTER_CAP
00020h	FAUX_CAP
00021h	MSTM_CAP
00022h	NUMBER_OF_AUDIO_ENDPOINTS
00023h	AV_GRANULARITY
00024h	AV_SYNC_DATA_BLOCK
00030h	GUID
00054h	RX_GTC_VALUE
00058h	RX_GTC_MSTR_REQ
00059h	RX_GTC_FREQ_LOCK_DONE
00080h	Downstream Ports

MAX_DOWNSPREAD
00003h

Bit	Field Name	Field Value
0	MAX_DOWNSPREAD	1 = Up to 0.5%
5-1	RESERVED	○ 0 = None
6	NO_AUX_HANDSHAKE_LINK_TRAINING	● 1 = Up to 0.5% ke Required
7	RESERVED	0 = RESERVED



00000h	DPCD_REV
00001h	MAX_LINK_RATE
00002h	MAX_LANE_COUNT
00003h	MAX_DOWNSPREAD
00004h	NORP
00005h	DOWNSTREAMPORT_PRESENT
00006h	MAIN_LINK_CHANNEL_CODING
00007h	DOWN_STREAM_PORT_COUNT
00008h	RECEIVE_PORT0_CAP_0
00009h	RECEIVE_PORT0_CAP_1
0000Ah	RECEIVE_PORT1_CAP_0
0000Bh	RECEIVE_PORT1_CAP_1
0000Ch	I2C_SPEED_CONTROL_CAP
0000Dh	eDP_CONFIGURATION_CAP
0000Eh	TRAINING_AUX_RD_INTERVAL
0000Fh	ADAPTER_CAP
00020h	FAUX_CAP
00021h	MSTM_CAP
00022h	NUMBER_OF_AUDIO_ENDPOINTS
00023h	AV_GRANULARITY
00024h	AV_SYNC_DATA_BLOCK
00030h	GUID
00054h	RX_GTC_VALUE
00058h	RX_GTC_MSTR_REQ
00059h	RX_GTC_FREQ_LOCK_DONE
00080h	Downstream Ports

/User/default

DisplayPort Video Generator RX - Card 6 (DP-R62)

MAX_DOWNSPREAD

00003h

Bit	Field Name	Field Value
0	MAX_DOWNSPREAD	1 = Up to 0.5%
5-1	RESERVED	0
6	NO_AUX_HANDSHAKE_LINK_TRAINING	0 = AUX CH handshake Required
7	RESERVED	

● 0 = AUX CH handshake Required

○ 1 = AUX CH handshake Not Required

/User/default
DisplayPort Video Generator RX - Card 6 (DP-R62)

DOWNSTREAMPORT_PRESENT
00005h

00000h	DPCD_REV
00001h	MAX_LINK_RATE
00002h	MAX_LANE_COUNT
00003h	MAX_DOWNSPREAD
00004h	NORP
00005h	DOWNSTREAMPORT_PRESENT
00006h	MAIN_LINK_CHANNEL_CODING
00007h	DOWN_STREAM_PORT_COUNT
00008h	RECEIVE_PORT0_CAP_0
00009h	RECEIVE_PORT0_CAP_1
0000Ah	RECEIVE_PORT1_CAP_0
0000Bh	RECEIVE_PORT1_CAP_1
0000Ch	I2C_SPEED_CONTROL_CAP
0000Dh	eDP_CONFIGURATION_CAP
0000Eh	TRAINING_AUX_RD_INTERVAL
0000Fh	ADAPTER_CAP
00020h	FAUX_CAP
00021h	MSTM_CAP
00022h	NUMBER_OF_AUDIO_ENDPOINTS
00023h	AV_GRANULARITY
00024h	AV_SYNC_DATA_BLOCK
00030h	GUID
00054h	RX_GTC_VALUE
00058h	RX_GTC_MSTR_REQ
00059h	RX_GTC_FREQ_LOCK_DONE
00080h	Downstream Ports

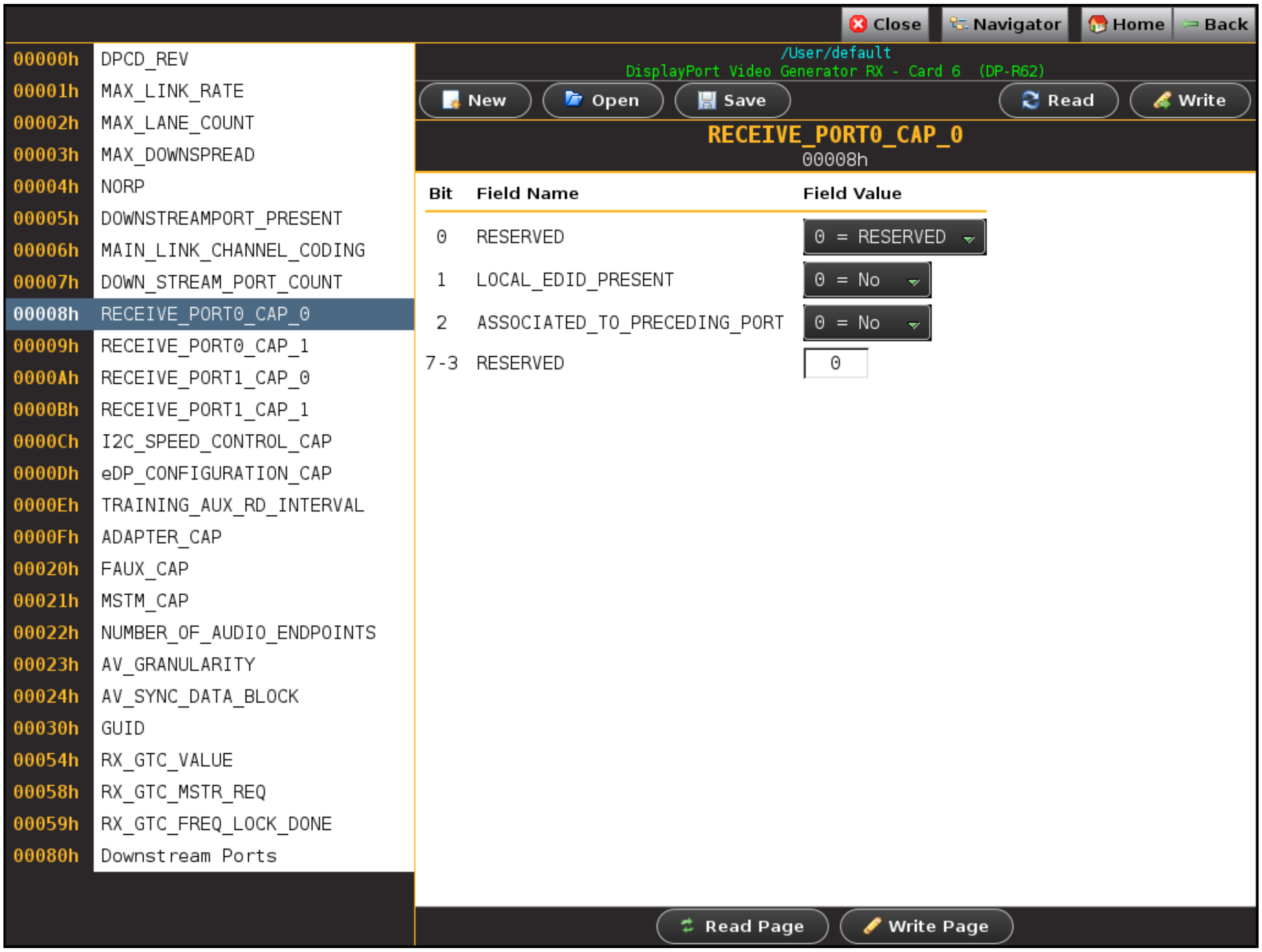
Bit	Field Name	Field Value
0	DWN_STRM_PORT_PRESENT	0 = No ● 0 = No ○ 1 = Yes
2-1	DWN_STRM_PORT_TYPE	Port
3	FORMAT_CONVERSION	
4	DETAILED_CAP_INFO_AVAILABLE	0 = No
7-5	RESERVED	0

00000h	DPCD_REV
00001h	MAX_LINK_RATE
00002h	MAX_LANE_COUNT
00003h	MAX_DOWNSPREAD
00004h	NORP
00005h	DOWNSTREAMPORT_PRESENT
00006h	MAIN_LINK_CHANNEL_CODING
00007h	DOWN_STREAM_PORT_COUNT
00008h	RECEIVE_PORT0_CAP_0
00009h	RECEIVE_PORT0_CAP_1
0000Ah	RECEIVE_PORT1_CAP_0
0000Bh	RECEIVE_PORT1_CAP_1
0000Ch	I2C_SPEED_CONTROL_CAP
0000Dh	eDP_CONFIGURATION_CAP
0000Eh	TRAINING_AUX_RD_INTERVAL
0000Fh	ADAPTER_CAP
00020h	FAUX_CAP
00021h	MSTM_CAP
00022h	NUMBER_OF_AUDIO_ENDPOINTS
00023h	AV_GRANULARITY
00024h	AV_SYNC_DATA_BLOCK
00030h	GUID
00054h	RX_GTC_VALUE
00058h	RX_GTC_MSTR_REQ
00059h	RX_GTC_FREQ_LOCK_DONE
00080h	Downstream Ports

DOWN_STREAM_PORT_COUNT

00007h

Bit	Field Name	Field Value
3-0	DWN_STRM_PORT_COUNT	0
5-4	RESERVED	0
6	MSA_TIMING_PAR_IGNORED	0 = No
7	OUI Support	● 0 = No ○ 1 = Yes



00000h	DPCD_REV
00001h	MAX_LINK_RATE
00002h	MAX_LANE_COUNT
00003h	MAX_DOWNSPREAD
00004h	NORP
00005h	DOWNSTREAMPORT_PRESENT
00006h	MAIN_LINK_CHANNEL_CODING
00007h	DOWN_STREAM_PORT_COUNT
00008h	RECEIVE_PORT0_CAP_0
00009h	RECEIVE_PORT0_CAP_1
0000Ah	RECEIVE_PORT1_CAP_0
0000Bh	RECEIVE_PORT1_CAP_1
0000Ch	I2C_SPEED_CONTROL_CAP
0000Dh	eDP_CONFIGURATION_CAP
0000Eh	TRAINING_AUX_RD_INTERVAL
0000Fh	ADAPTER_CAP
00020h	FAUX_CAP
00021h	MSTM_CAP
00022h	NUMBER_OF_AUDIO_ENDPOINTS
00023h	AV_GRANULARITY
00024h	AV_SYNC_DATA_BLOCK
00030h	GUID
00054h	RX_GTC_VALUE
00058h	RX_GTC_MSTR_REQ
00059h	RX_GTC_FREQ_LOCK_DONE
00080h	Downstream Ports

RECEIVE_PORT0_CAP_0
00008h

Bit	Field Name	Field Value
0	RESERVED	0 = RESERVED
1	LOCAL_EDID_PRESENT	0 = No
2	ASSOCIATED_TO_PRECEDING_PORT	0 = No
7-3	RESERVED	0

/User/default
DisplayPort Video Generator RX - Card 6 (DP-R62)

00000h	DPCD_REV
00001h	MAX_LINK_RATE
00002h	MAX_LANE_COUNT
00003h	MAX_DOWNSPREAD
00004h	NORP
00005h	DOWNSTREAMPORT_PRESENT
00006h	MAIN_LINK_CHANNEL_CODING
00007h	DOWN_STREAM_PORT_COUNT
00008h	RECEIVE_PORT0_CAP_0
00009h	RECEIVE_PORT0_CAP_1
0000Ah	RECEIVE_PORT1_CAP_0
0000Bh	RECEIVE_PORT1_CAP_1
0000Ch	I2C_SPEED_CONTROL_CAP
0000Dh	eDP_CONFIGURATION_CAP
0000Eh	TRAINING_AUX_RD_INTERVAL
0000Fh	ADAPTER_CAP
00020h	FAUX_CAP
00021h	MSTM_CAP
00022h	NUMBER_OF_AUDIO_ENDPOINTS
00023h	AV_GRANULARITY
00024h	AV_SYNC_DATA_BLOCK
00030h	GUID
00054h	RX_GTC_VALUE
00058h	RX_GTC_MSTR_REQ
00059h	RX_GTC_FREQ_LOCK_DONE
00080h	Downstream Ports

MSTM_CAP
00021h

Bit	Field Name	Field Value
0	MST_CAP	0 = No
7-1	RESERVED	0

12 Source Verification with Protocol Analyzer (Optional)

The 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module is equipped with a DP 1.4 Rx port for the optional Network Analyzer features. There are two analyzer options available:

1) Basic Analyzer – Emulates a DP 1.4 sink device including EDID, DPCD, MST, Link Training emulation. Provides real time view of the incoming source video and metadata including status of mainstream attributes, secondary stream attributes, link training, MST, HDCP. Also provides support for viewing the Aux Channel transactions using the Quantum Data Auxiliary Channel Analyzer (ACA) application when testing a DP source.

2) Protocol Analyzer (requires the Basic Analyzer license to be installed) – Provides capture and store of the main link protocol, video and metadata including main stream attributes and secondary data from an incoming DP source device.

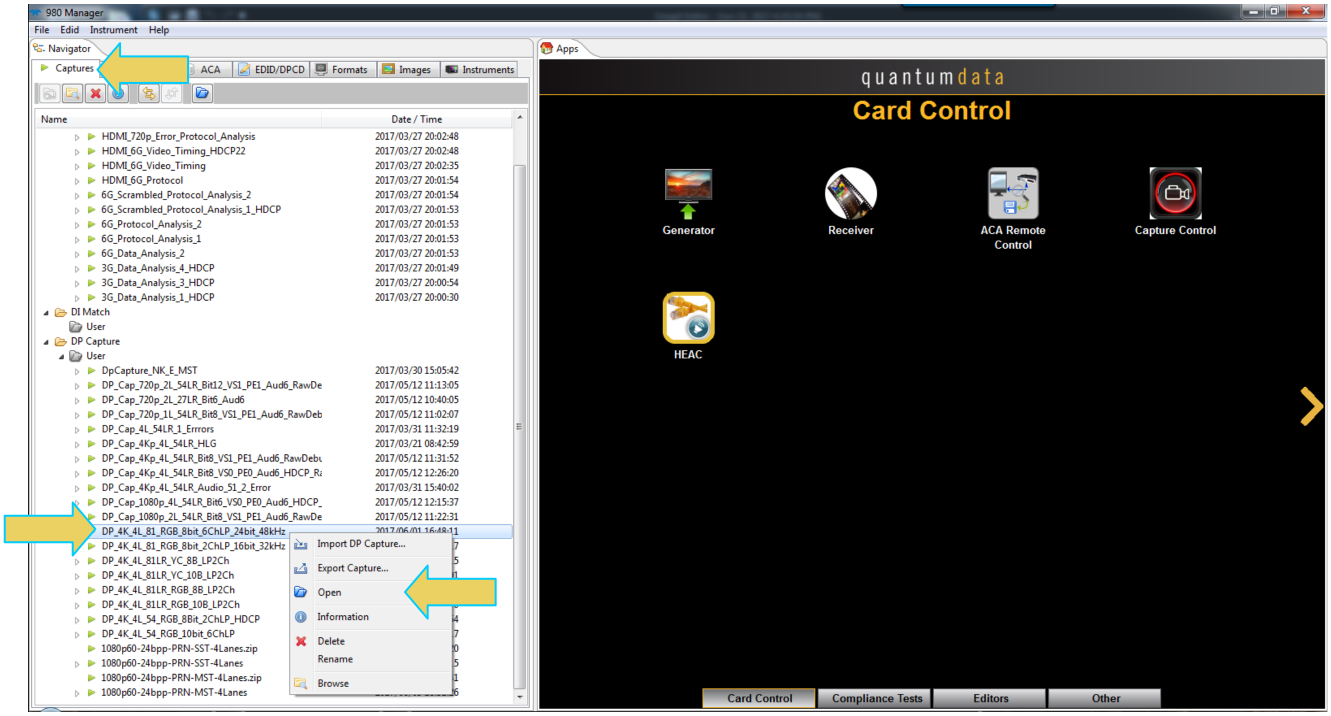
12.1 Operational workflow for capturing data with your 980 DP Protocol Analyzer

This subsection describes how to use the 980 DP Protocol Analyzer to capture and analyze DisplayPort source devices. Testing an DP source device involves the following high level steps:

1. Configure the 980 DP Protocol Analyzer Rx port with the proper EDID.
2. Connecting the DP source device.
3. View the incoming video in real time to check the status of the device under test.
4. Specify a trigger method.
5. Initiate the capturing of the data.
6. Examine the test data through the 980 GUI Manager at the high level view on the **Event Plot** panel or the Video Analysis panel.
7. Drill down to examine the data at the lower level through the details of the **Data Decode** panel view.
8. (Optional) You may wish to capture and view the raw hex data.

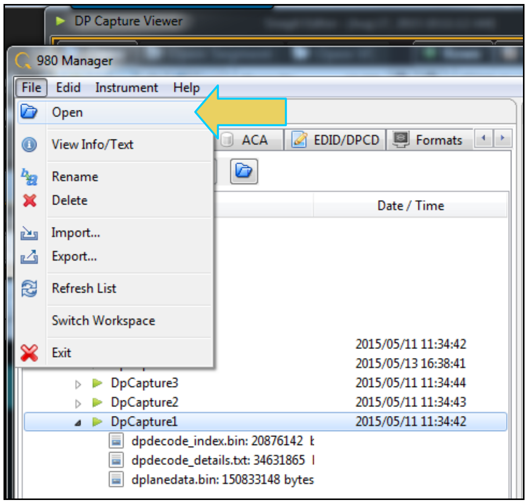
12.2 Opening an Existing Capture

The DisplayPort Protocol Analyzer feature enables you to save capture data for later examination. You can access existing captures through the **Navigator** utility as shown in the screen shot below. The right click menu enables you to open a capture. You can also open a capture from the **Open** option on the **File** menu on top (shown below).



Name	Date / Time
HDMI_720p_Error_Protocol_Analysis	2017/03/27 20:02:48
HDMI_6G_Video_Timing_HDCP22	2017/03/27 20:02:48
HDMI_6G_Video_Timing	2017/03/27 20:02:35
HDMI_6G_Protocol	2017/03/27 20:01:54
6G_Scrambled_Protocol_Analysis_2	2017/03/27 20:01:54
6G_Scrambled_Protocol_Analysis_1_HDCP	2017/03/27 20:01:53
6G_Protocol_Analysis_2	2017/03/27 20:01:53
6G_Protocol_Analysis_1	2017/03/27 20:01:53
6G_Data_Analysis_2	2017/03/27 20:01:53
3G_Data_Analysis_4_HDCP	2017/03/27 20:01:49
3G_Data_Analysis_3_HDCP	2017/03/27 20:00:54
3G_Data_Analysis_1_HDCP	2017/03/27 20:00:30
DI Match	
User	
DP Capture	
User	
DpCapture_NK_E_MST	2017/03/30 15:05:42
DP_Cap_720p_2L_54LR_Bit12_VS1_PE1_Aud6_RawDe	2017/05/12 11:13:05
DP_Cap_720p_2L_27LR_Bit6_Aud6	2017/05/12 10:40:05
DP_Cap_720p_1L_54LR_Bit8_VS1_PE1_Aud6_RawDeb	2017/05/12 11:02:07
DP_Cap_4L_54LR_1_Errrors	2017/03/31 11:32:19
DP_Cap_4Kp_4L_54LR_HLG	2017/03/21 08:42:59
DP_Cap_4Kp_4L_54LR_Bit8_VS1_PE1_Aud6_RawDebu	2017/05/12 11:31:52
DP_Cap_4Kp_4L_54LR_Bit8_VS0_PE0_Aud6_HDCP_Ra	2017/05/12 12:26:20
DP_Cap_4Kp_4L_54LR_Audio_51_2_Error	2017/03/31 15:40:02
DP_Cap_1080p_4L_54LR_Bit6_VS0_PE0_Aud6_HDCP_	2017/05/12 12:15:37
DP_Cap_1080p_2L_54LR_Bit8_VS1_PE1_Aud6_RawDe	2017/05/12 11:22:31
DP_4K_4L_81_RGB_8bit_6ChLP_24bit_48kHz	2017/06/01 16:48:11
DP_4K_4L_81_RGB_8bit_2ChLP_16bit_32kHz	
DP_4K_4L_81LR_YC_8B_LP2Ch	
DP_4K_4L_81LR_YC_10B_LP2Ch	
DP_4K_4L_81LR_RGB_8B_LP2Ch	
DP_4K_4L_81LR_RGB_10B_LP2Ch	
DP_4K_4L_54_RGB_8Bit_2ChLP_HDCP	
DP_4K_4L_54_RGB_10bit_6ChLP	
1080p60-24bpp-PRN-SST-4Lanes.zip	
1080p60-24bpp-PRN-SST-4Lanes	
1080p60-24bpp-PRN-MST-4Lanes.zip	
1080p60-24bpp-PRN-MST-4Lanes	

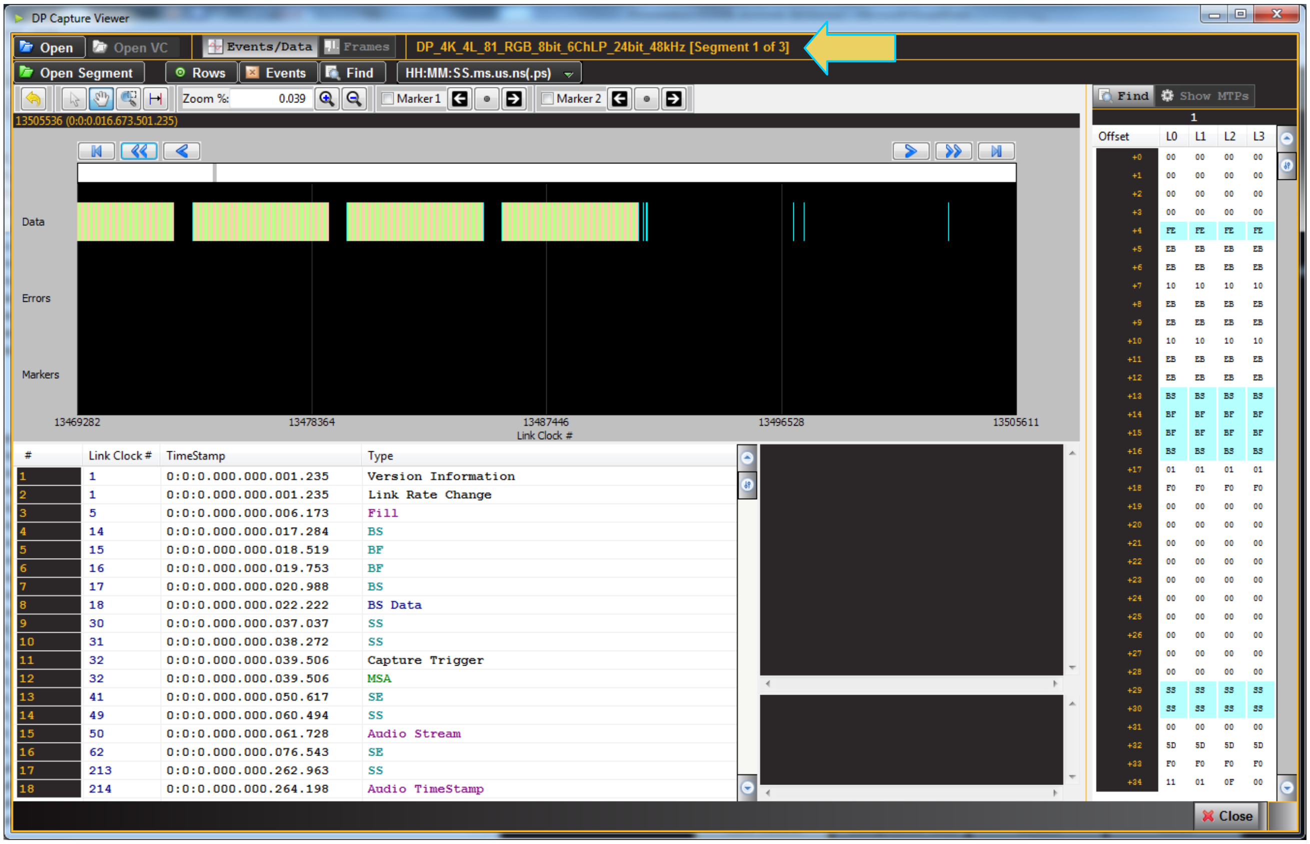
When you choose **Open** from the right click menu, or the **File** menu on the top set of tabs, the **Capture Viewer** window will open with the capture that was selected.



	Date / Time
	2015/05/11 11:34:42
	2015/05/13 16:38:41
DpCapture3	2015/05/11 11:34:44
DpCapture2	2015/05/11 11:34:43
DpCapture1	2015/05/11 11:34:42
dpdecode_index.bin: 20876142 b	
dpdecode_details.txt: 34631865	
dplanedata.bin: 150833148 bytes	

You can also **Delete** a capture through the **Navigator** from the right click menu or the **File** pull-down menu show in the examples above. You can rename a capture using the **Rename** option in the right click or **File** pull-down menu.

When a capture file opens, the name of the capture file is shown on the top as indicated below.

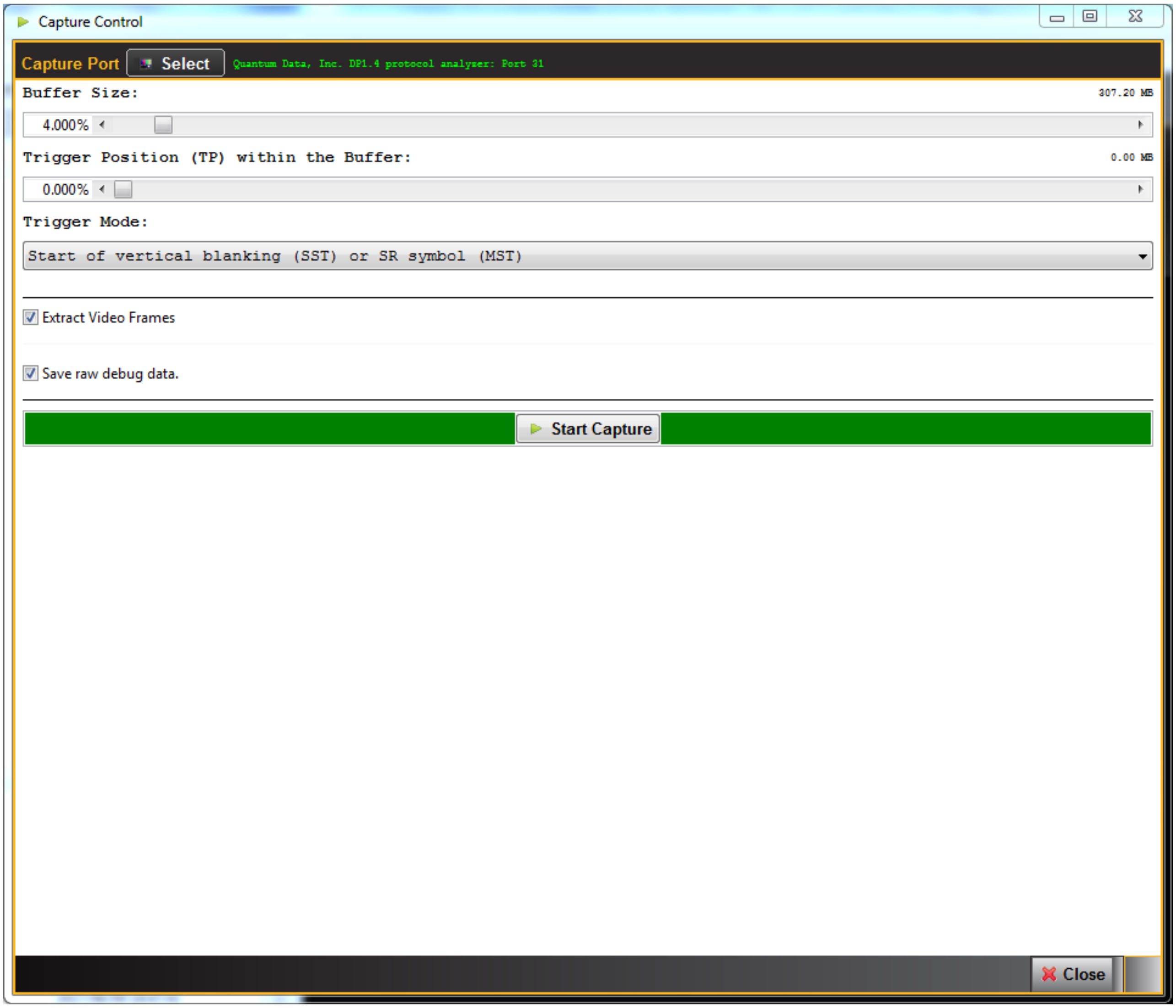


#	Link Clock #	TimeStamp	Type
1	1	0:0:0.000.000.001.235	Version Information
2	1	0:0:0.000.000.001.235	Link Rate Change
3	5	0:0:0.000.000.006.173	Fill
4	14	0:0:0.000.000.017.284	BS
5	15	0:0:0.000.000.018.519	BF
6	16	0:0:0.000.000.019.753	BF
7	17	0:0:0.000.000.020.988	BS
8	18	0:0:0.000.000.022.222	BS Data
9	30	0:0:0.000.000.037.037	SS
10	31	0:0:0.000.000.038.272	SS
11	32	0:0:0.000.000.039.506	Capture Trigger
12	32	0:0:0.000.000.039.506	MSA
13	41	0:0:0.000.000.050.617	SE
14	49	0:0:0.000.000.060.494	SS
15	50	0:0:0.000.000.061.728	Audio Stream
16	62	0:0:0.000.000.076.543	SE
17	213	0:0:0.000.000.262.963	SS
18	214	0:0:0.000.000.264.198	Audio TimeStamp

Offset	L0	L1	L2	L3
+0	00	00	00	00
+1	00	00	00	00
+2	00	00	00	00
+3	00	00	00	00
+4	FE	FE	FE	FE
+5	EB	EB	EB	EB
+6	EB	EB	EB	EB
+7	10	10	10	10
+8	EB	EB	EB	EB
+9	EB	EB	EB	EB
+10	10	10	10	10
+11	EB	EB	EB	EB
+12	EB	EB	EB	EB
+13	BS	BS	BS	BS
+14	BF	BF	BF	BF
+15	BF	BF	BF	BF
+16	BS	BS	BS	BS
+17	01	01	01	01
+18	F0	F0	F0	F0
+19	00	00	00	00
+20	00	00	00	00
+21	00	00	00	00
+22	00	00	00	00
+23	00	00	00	00
+24	00	00	00	00
+25	00	00	00	00
+26	00	00	00	00
+27	00	00	00	00
+28	00	00	00	00
+29	SS	SS	SS	SS
+30	SS	SS	SS	SS
+31	00	00	00	00
+32	5D	5D	5D	5D
+33	F0	F0	F0	F0
+34	11	01	0F	00

12.3 Capture Control Panel

You initiate a new capture through the **Capture Control** panel. The **Capture Control** panel enables you to setup the capture parameters. The figure below shows the **Capture Control** panel and its control and selection items.



Quantum Data, Inc. DP1.4 protocol analyzer: Port 31

Buffer Size: 307.20 MB

4.000%

Trigger Position (TP) within the Buffer: 0.00 MB

0.000%

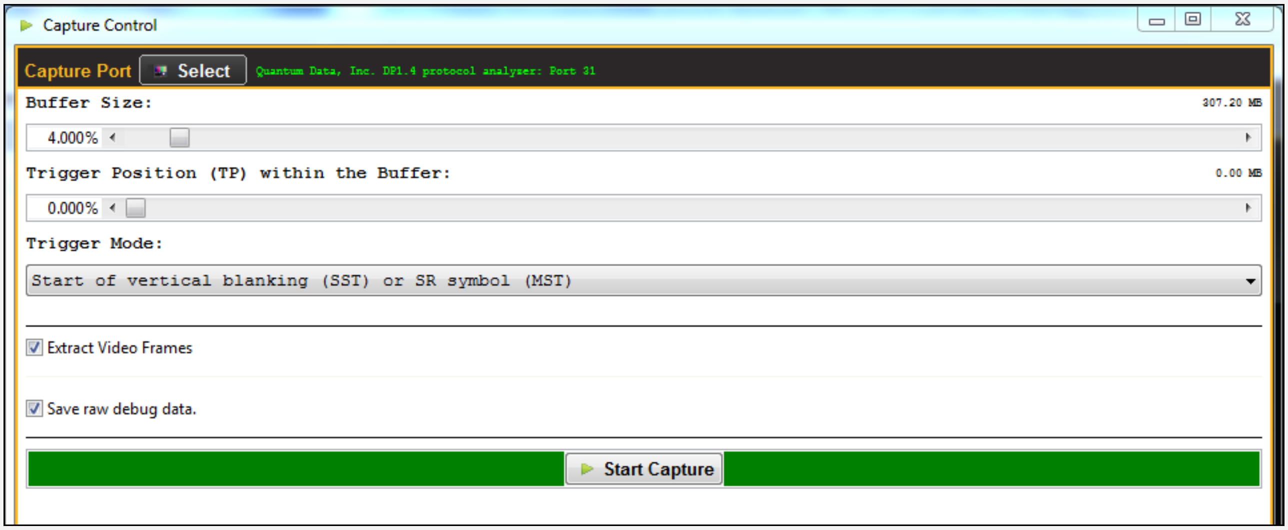
Trigger Mode:

Start of vertical blanking (SST) or SR symbol (MST)

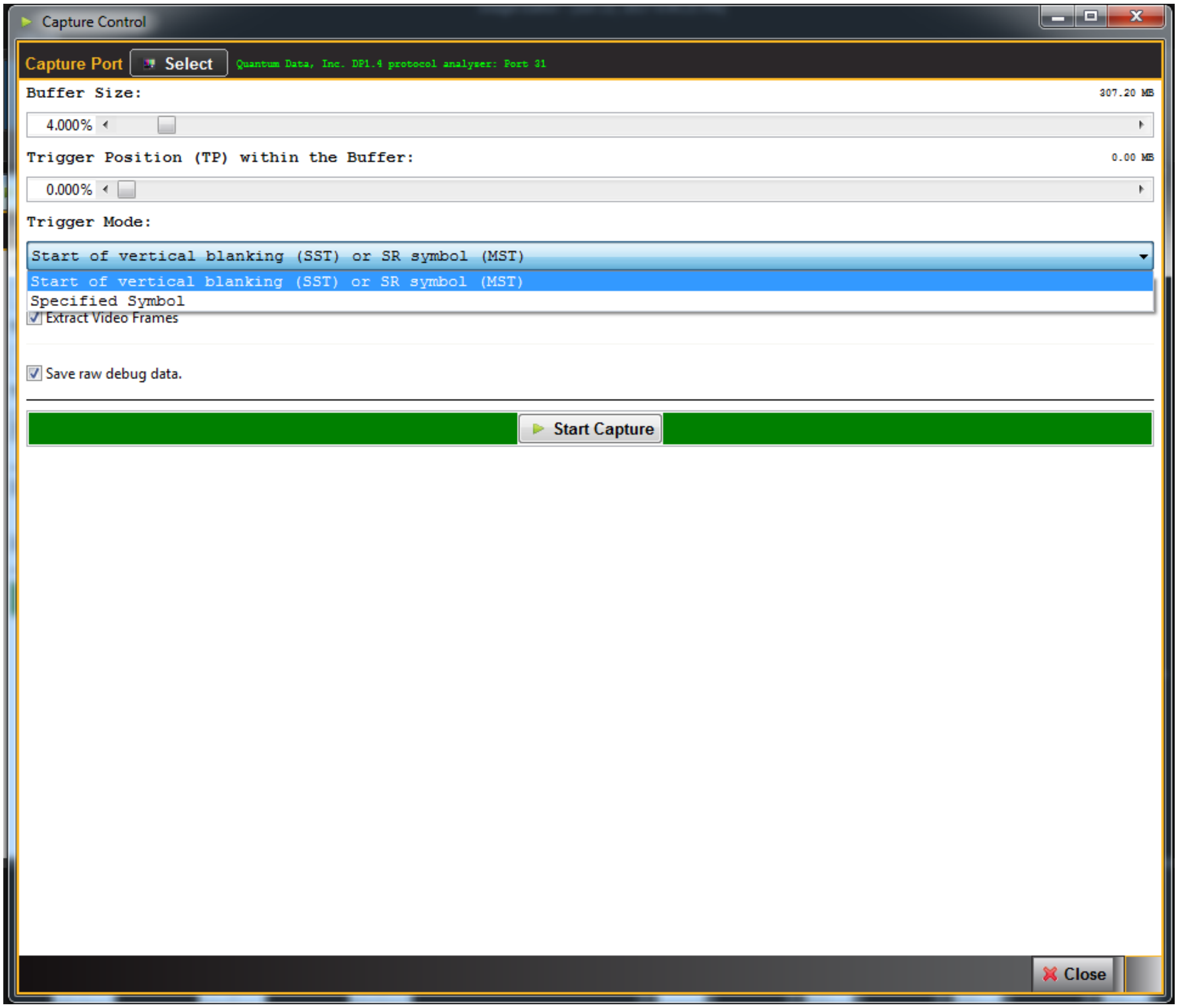
☑ Extract Video Frames

☑ Save raw debug data.

The following table describes the functions of the **Capture Control** panel.

Capture Control Panel - Function	**Item - Description**	
Instrument Selection Capture Control Capture Port Select Quantum Data, Inc. DP1.4 protocol analyzer: Port 31 Buffer Size: 307.20 MB 4.000% Trigger Position (TP) within the Buffer: 0.00 MB 0.000% Trigger Mode: Start of vertical blanking (SST) or SR symbol (MST) ☑ Extract Video Frames ☑ Save raw debug data. Start Capture		
Capture Trigger Configuration	Enables you to define the capture trigger criteria. Use the information below.	
	[Capture] Buffer Size Slidebar	Enables you to set the size of the captured data in percent. This is a slidebar that provides an indication (on the left) of the percent of the total possible size to be captured. A lower value will require less time for the captured data to accumulate.
	[Capture] Trigger Position within Buffer Slidebar	Enables you to set the position of the trigger event within the captured data. This slidebar determines how much of the data that has accumulated in the capture buffer has occurred before the trigger event. The slidebar has an indication (on the left) of the location of the trigger event within the captured data. The value is expressed as a percent. A value of 0% indicates that the trigger event occurs at the beginning of the resulting captured data and 100% indicates that the trigger event occurs at the end of the resulting captured data. A value of 50% indicates that the trigger event is in the middle of the captured data. **Note**: The Buffer Position Slidebar is not applicable when you select Vsync as the trigger condition.
	Trigger Mode	Enables you to specify the type of data that you

Capture Control Panel - Function	**Item - Description**	
	(Capture Tab)	want to capture. This could be: • Start of Vertical Blanking (SST) or SR symbol MST. • Specified Symbol (see below).
	Trigger Symbol (Capture Tab)	If Specified Symbol is selected then select one of: • BS=Blanking Start • BE=Blanking End • BF=Blanking Fill • C0-C7=VC Payload Fill Control code sequence • CP=Content Protection • FE=Fill End, FS=Fill Start • R0-2 • SE=Secondary Data End • SR=Scrambler Reset, • SS=Secondary Data Start • Other.
	Start Capture (Capture Tab)	Initiates a capture using the criteria defined in the **Trigger Mode** and **Trigger Symbol**.
	Extract Video Frames	Enables you to view the video frames that were captured.
	Save raw debug data	Enables you to save raw hex debug data.



Quantum Data, Inc. DP1.4 protocol analyzer: Port 31

Buffer Size: 307.20 MB

4.000%

Trigger Position (TP) within the Buffer: 0.00 MB

0.000%

Trigger Mode:

Start of vertical blanking (SST) or SR symbol (MST)

Start of vertical blanking (SST) or SR symbol (MST)
Specified Symbol

☑ Extract Video Frames

☑ Save raw debug data.

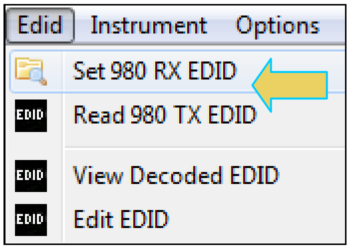
12.4 Configuring the 980 DP Protocol Analyzer with an EDID

Use the procedures below to provision the 980 DP Protocol Analyzer Rx port with an EDID to emulate a sink device.

To provision the EDID:

1. (optional) Load the EDID to use in the 980 DP Video Generator / Analyzer. This is the EDID that the module will be emulating on its Rx port.

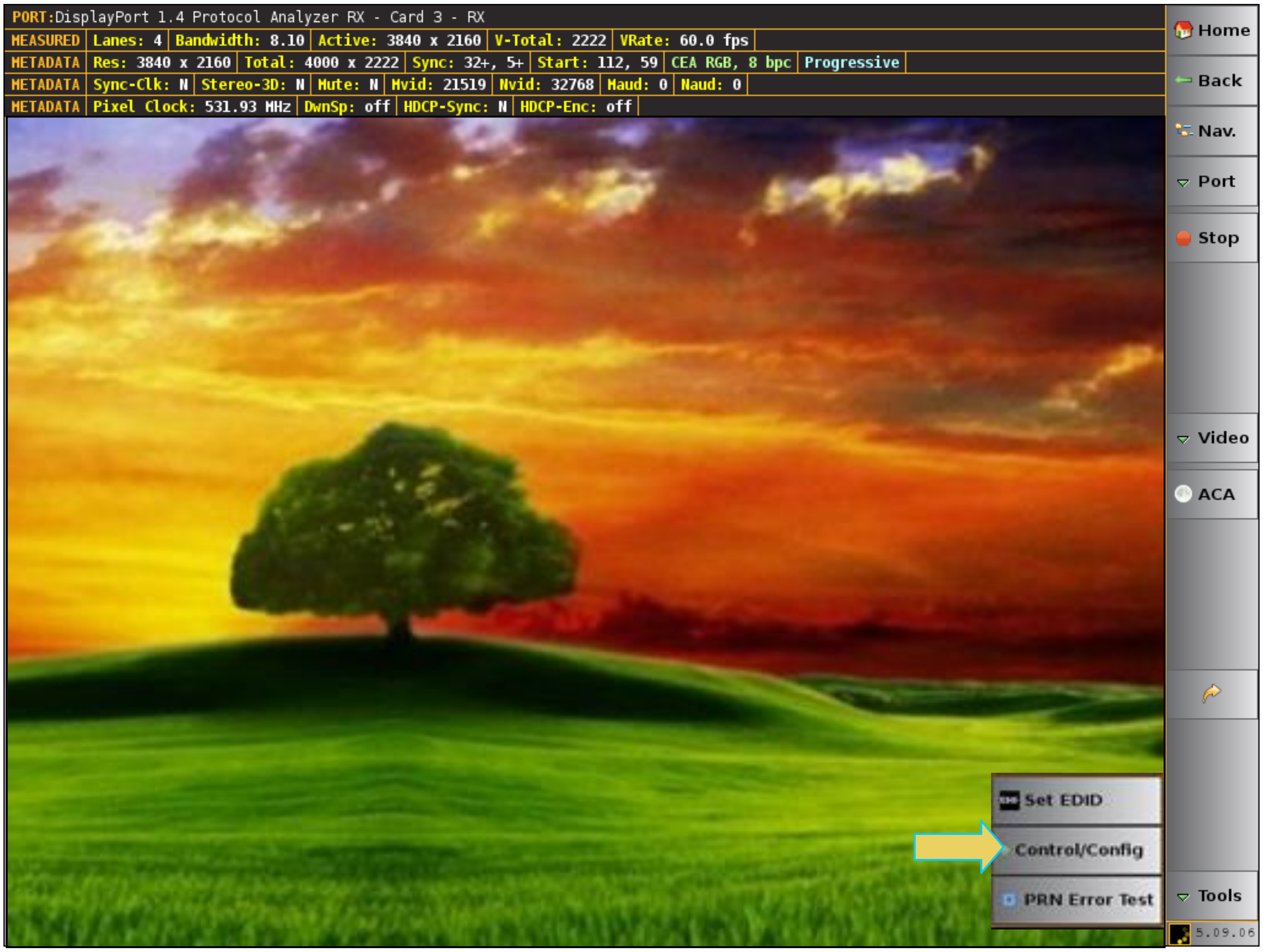
   The default EDID in the 980 DP Protocol Analyzer Rx has a preferred timing of 1080p60 with a maximum TMDS rate of 165MHz. You can provision the module with a different EDID. Sample EDIDs are available from the Quantum Data website on the downloads page (http://www.quantumdata.com/support/980readme.asp#edid). You can download these EDIDs to the host PC where the 980 GUI Manager is running. Select an EDID file by activating the **Set 980 Rx EDID** (shown on the screen below).



The dialog box shown below opens up.

If you wish to use a different EDID from an HDTV that you have available you can quickly provision the 980 module with that EDID.

Note you can also set the EDID from the **Tools** menu of the **Real Time** mode.



```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 3 - RX
MEASURED | Lanes: 4 | Bandwidth: 8.10 | Active: 3840 x 2160 | V-Total: 2222 | VRate: 60.0 fps
METADATA | Res: 3840 x 2160 | Total: 4000 x 2222 | Sync: 32+, 5+ | Start: 112, 59 | CEA RGB, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 21519 | Nvid: 32768 | Maud: 0 | Naud: 0
METADATA | Pixel Clock: 531.93 MHz | DwnSp: off | HDCP-Sync: N | HDCP-Enc: off
```

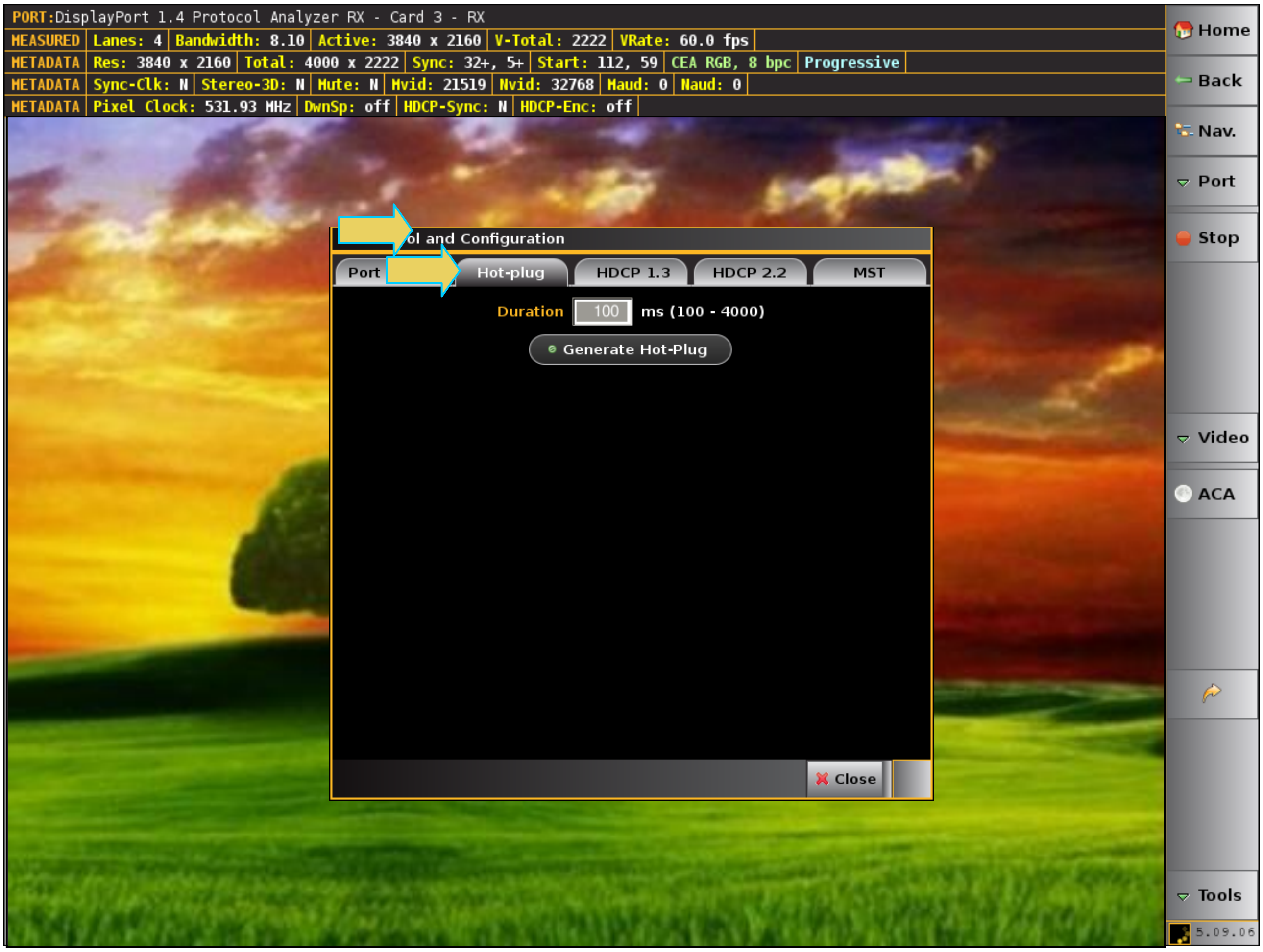
The same dialog box shown above appears when you select Set EDID.

2. Select an EDID to assign to the 980 DP Video Generator / Analyzer's Rx port. Click Ok after selecting the EDID.

   Note that there are two checkbox options on the dialog box. The following is a description of each:

   - Permanently set the Analyzer's EDID – This means that the EDID that you provision will persist through a reboot of the 980. Otherwise the default 980 EDID will be reprovisioned when a reboot occurs.
   - Issue Hot Plug – This means that 980 DP Analyzer will issue a hot plug when you click the OK activation button on this dialog box.

3. (optional) Set the Hot Plug duration and generator a hot plug. Access the **Rx Control and Configuration** dialog box from the **Tools** flyout menu. The **Rx Control and Configuration** dialog box is shown below:



PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 3 - RX

MEASURED | Lanes: 4 | Bandwidth: 8.10 | Active: 3840 x 2160 | V-Total: 2222 | VRate: 60.0 fps

METADATA | Res: 3840 x 2160 | Total: 4000 x 2222 | Sync: 32+, 5+ | Start: 112, 59 | CEA RGB, 8 bpc | Progressive

METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 21519 | Nvid: 32768 | Maud: 0 | Naud: 0

METADATA | Pixel Clock: 531.93 MHz | DwnSp: off | HDCP-Sync: N | HDCP-Enc: off

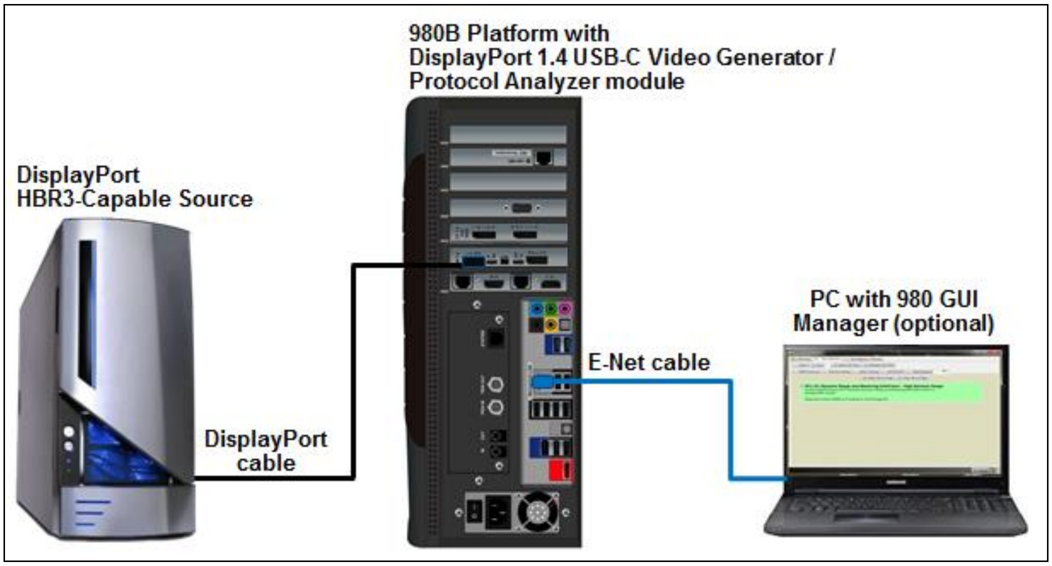
Duration 100 ms (100 - 4000)

12.5 Connecting a DisplayPort source to the Rx Analyzer port

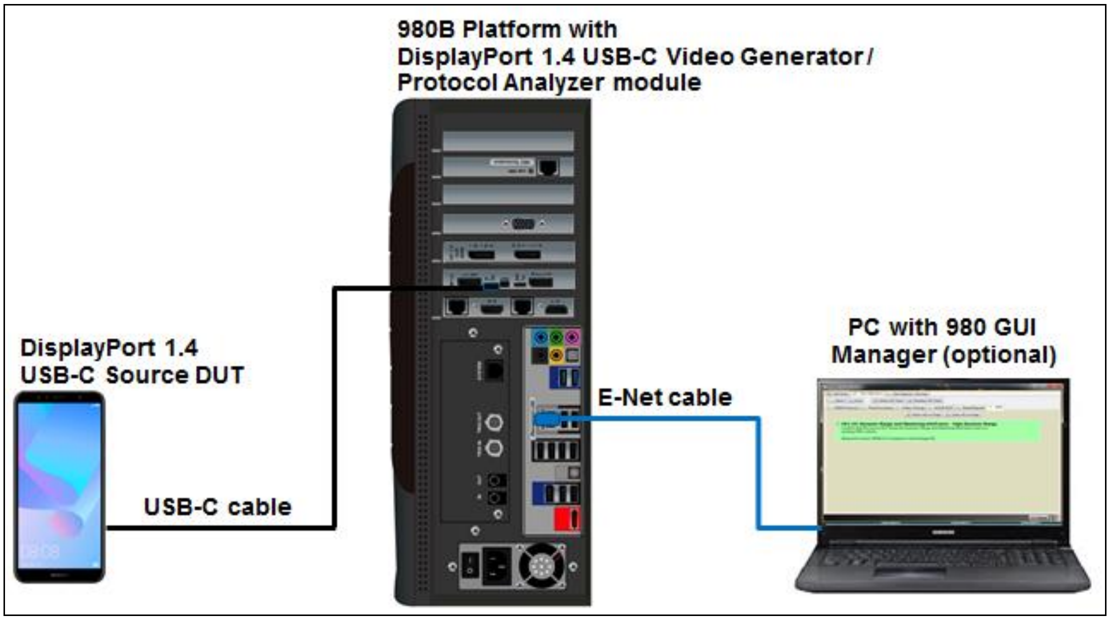
This subsection provides procedures on how to connect to the DP Rx Analyzer to the source device under test.

1. Connect the DP source device to the DP module’s Rx Analyzer port as shown below.

   Note the second PC shown is used for the 980 GUI Manager application.



DP Source DUT Connection to 980 DP Sink Emulation



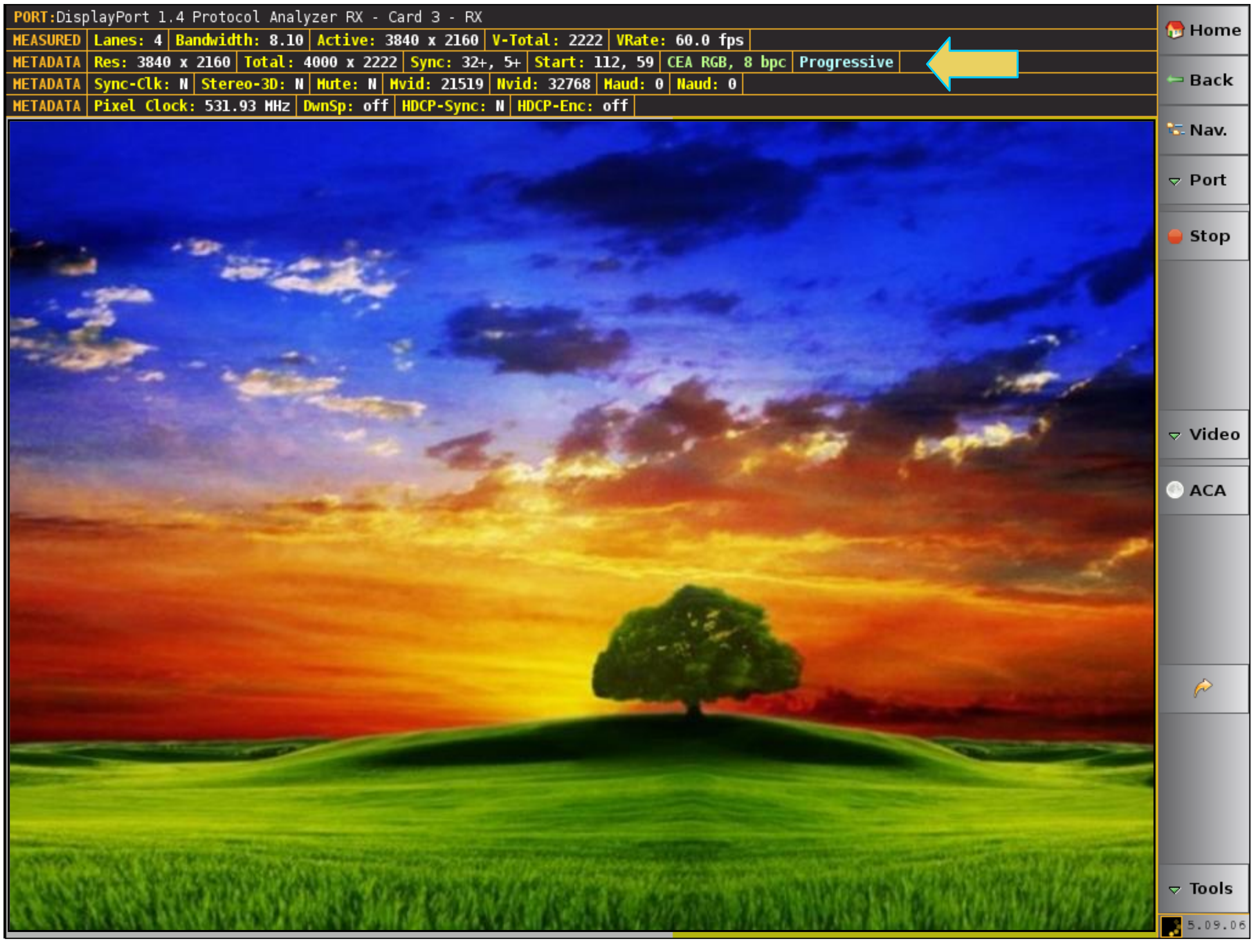
USB-C DP Alt Mode Source DUT Connection to 980 USB-C DP Alt Mode Sink Emulation

12.6 Verifying source video

Before you capture data you should verify that you are receiving DisplayPort video form the source.

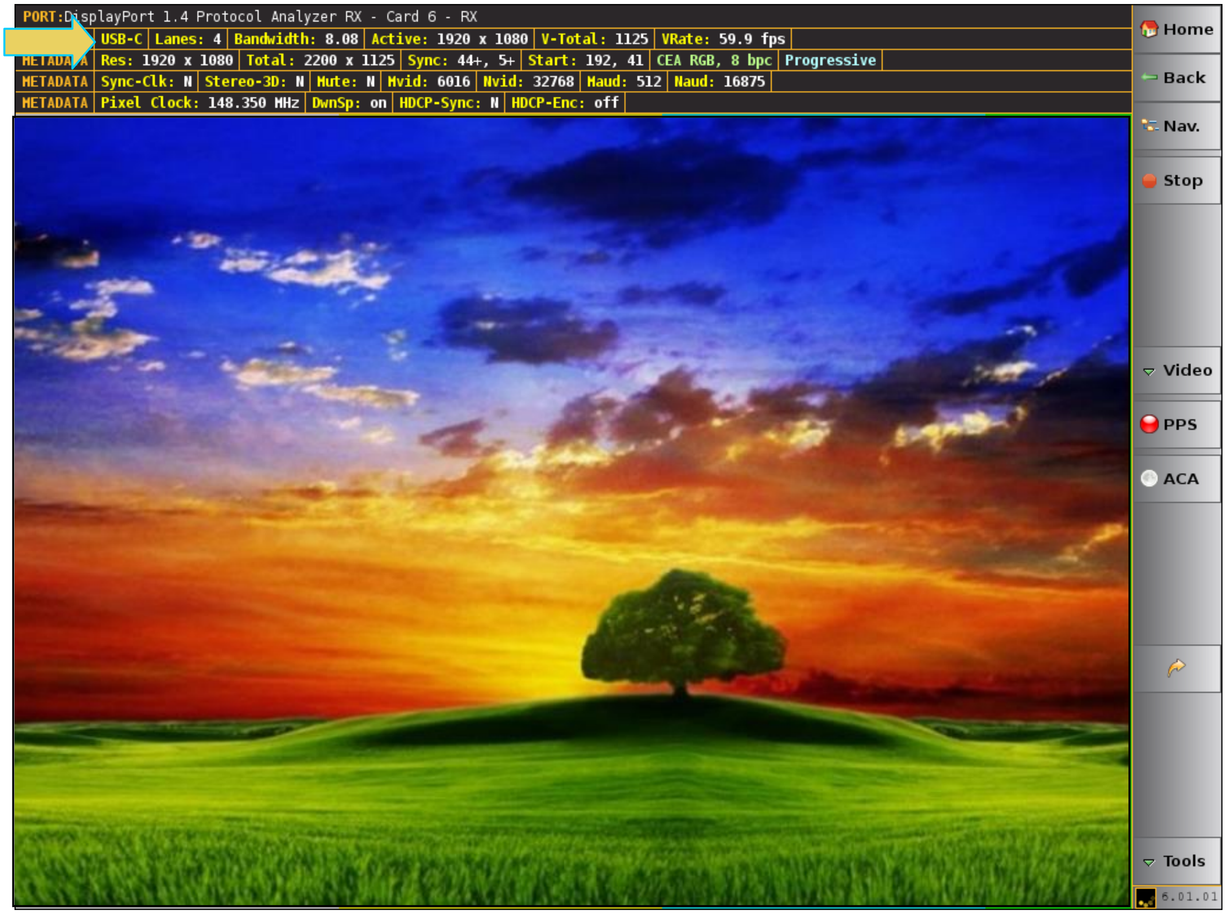
Verifying incoming DisplayPort source data

1. Verify the incoming video of the DisplayPort source to verify that the source is outputting the proper video. In the screen example below the video shown is a test pattern. Typically, the video you will see will be from a PC or some other source. Verify the information in the top status bar.



```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 3 - RX
MEASURED | Lanes: 4 | Bandwidth: 8.10 | Active: 3840 x 2160 | V-Total: 2222 | VRate: 60.0 fps
METADATA | Res: 3840 x 2160 | Total: 4000 x 2222 | Sync: 32+, 5+ | Start: 112, 59 | CEA RGB, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 21519 | Nvid: 32768 | Maud: 0 | Naud: 0
METADATA | Pixel Clock: 531.93 MHz | DwnSp: off | HDCP-Sync: N | HDCP-Enc: off
```

The following is an example of a Real Time view with USB-C source



```
PORT:DisplayPort 1.4 Protocol Analyzer RX - Card 6 - RX
         | USB-C | Lanes: 4 | Bandwidth: 8.08 | Active: 1920 x 1080 | V-Total: 1125 | VRate: 59.9 fps
METADA A | Res: 1920 x 1080 | Total: 2200 x 1125 | Sync: 44+, 5+ | Start: 192, 41 | CEA RGB, 8 bpc | Progressive
METADATA | Sync-Clk: N | Stereo-3D: N | Mute: N | Mvid: 6016 | Nvid: 32768 | Maud: 512 | Naud: 16875
METADATA | Pixel Clock: 148.350 MHz | DwnSp: on | HDCP-Sync: N | HDCP-Enc: off
```

12.7 Capturing DisplayPort source data

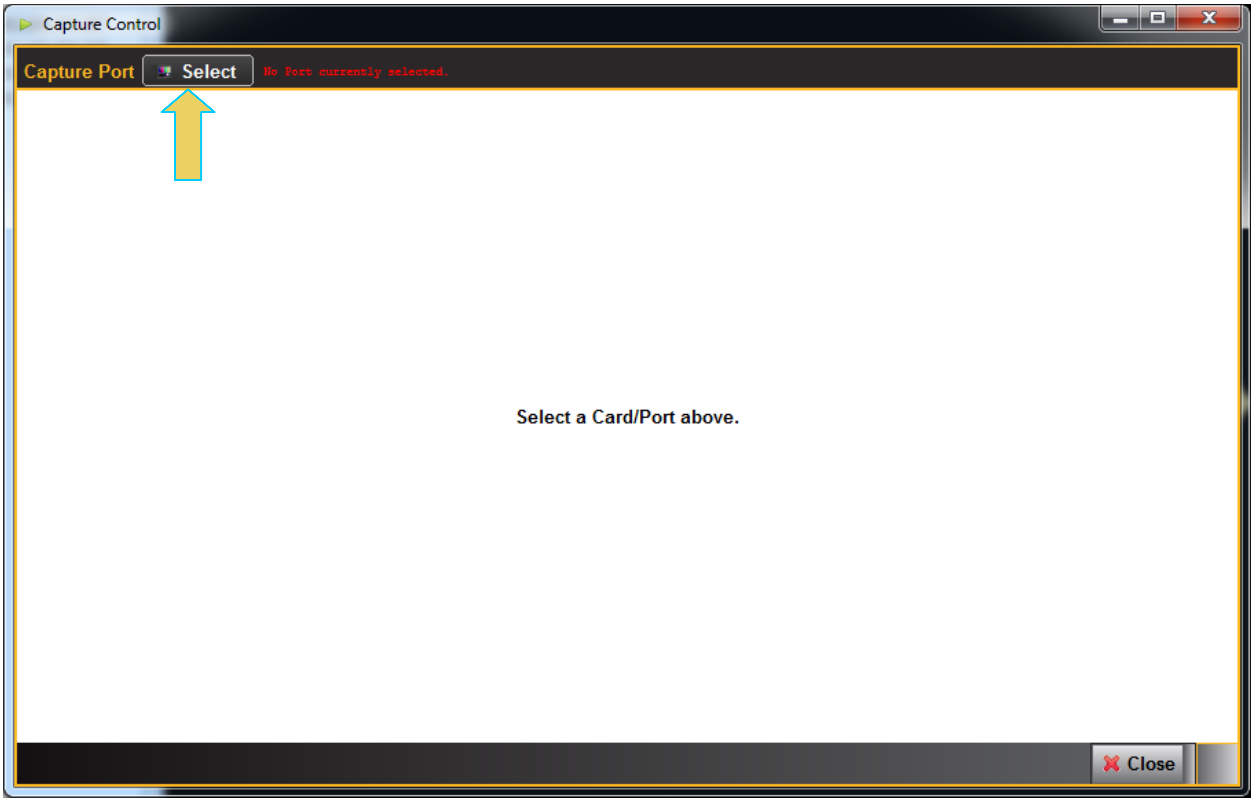
The procedures for running a capture of the DisplayPort source are described in this subsection. You can operate the Protocol Analyzer either through the 980s embedded display or via a PC through the external GUI Manager. Most of the examples in this section are taken from the embedded 980 GUI but the look and feel are quite similar between the two.

Capturing DisplayPort source data

1. Access the **Capture Control** application from the main window as shown below.

The **Capture Control** window opens as shown below.

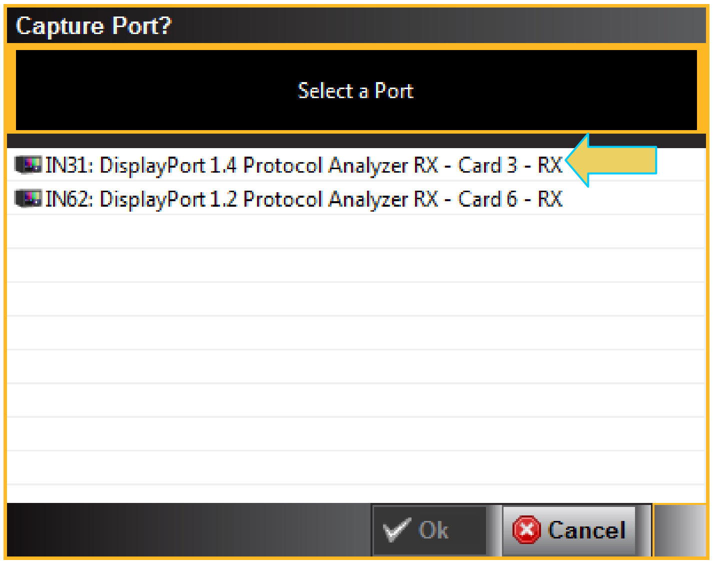
2. Select the port using the **Select** [Select] activation button as shown below.



No Port currently selected.

Select a Card/Port above.

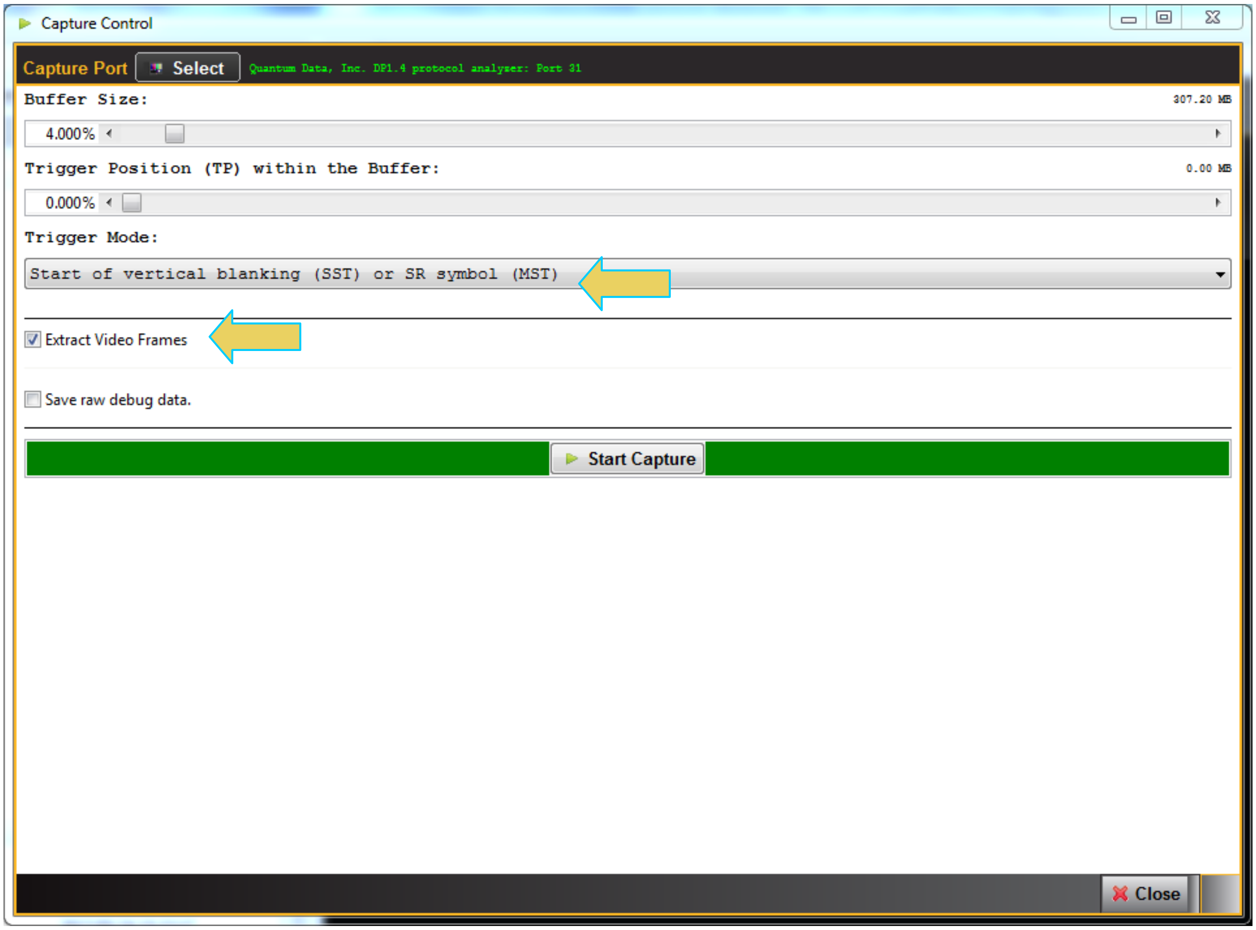
The **Capture Port** dialog box will appear enabling you to select which Protocol Analyzer module you wish to use. In this case it will be the DisplayPort Analyzer.



IN31: DisplayPort 1.4 Protocol Analyzer RX - Card 3 - RX
IN62: DisplayPort 1.2 Protocol Analyzer RX - Card 6 - RX

The **Capture Control** window opens as shown below.

3. Specify the **Buffer Size**, **Trigger Position** and **Trigger Mode** in accordance with the information provided earlier in this chapter.



Quantum Data, Inc. DP1.4 protocol analyzer: Port 31

Buffer Size: 307.20 MB

4.000%

Trigger Position (TP) within the Buffer: 0.00 MB

0.000%

Trigger Mode:

Start of vertical blanking (SST) or SR symbol (MST)

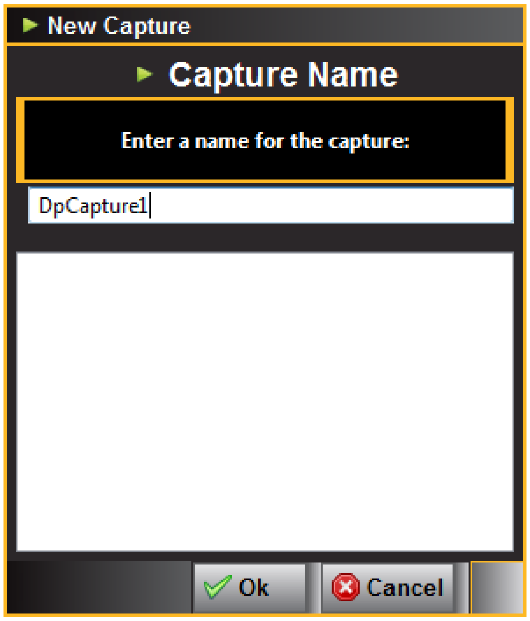
☑ Extract Video Frames

☐ Save raw debug data.

4. Specify whether or not you want to save the raw debug data as well (Save raw debug data).

5. Initiate the capture by clicking on the **Start Capture** activation button ▶ Start Capture.

   You will be prompted with a **New Capture** dialog box (below) given you an opportunity to assign a name to the capture file.

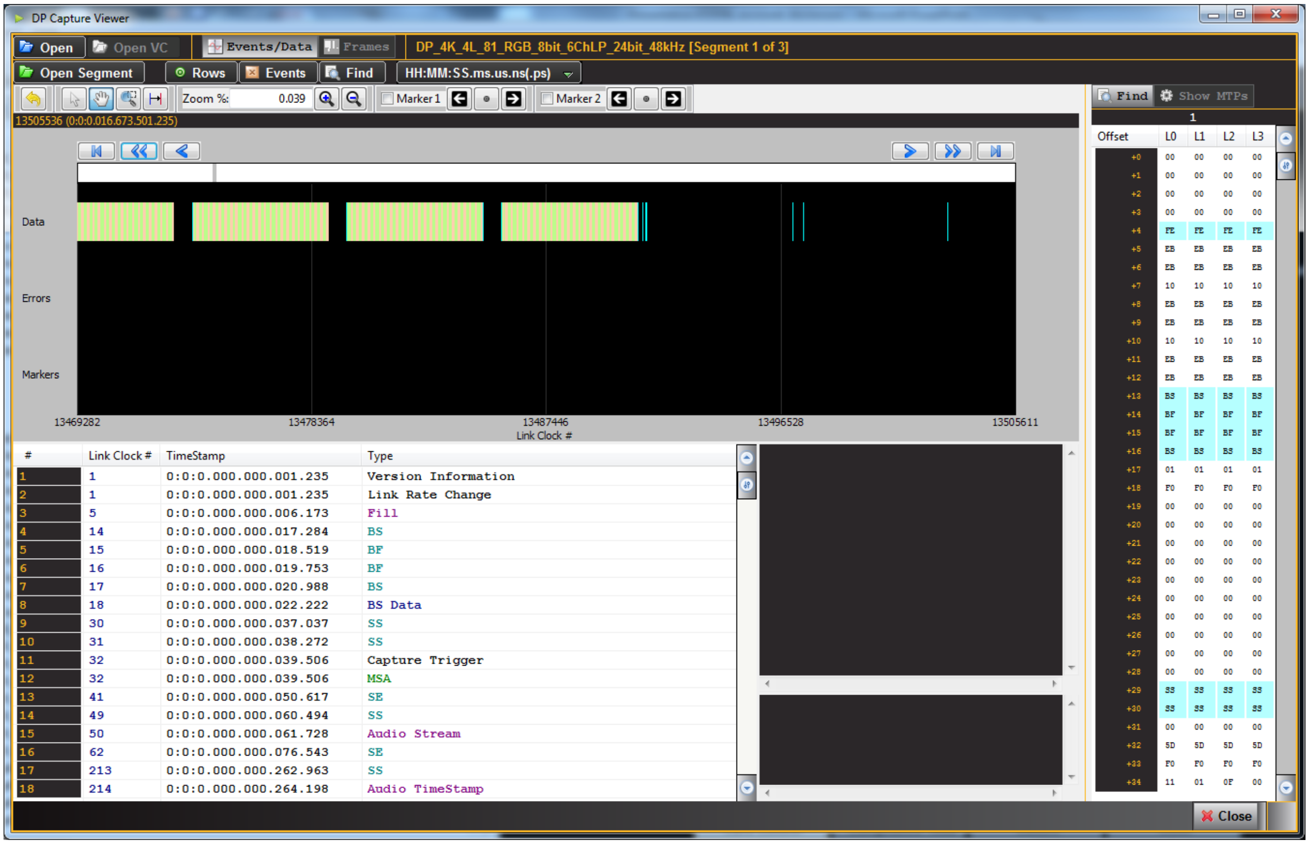


Enter a name for the capture:

DpCapture1

6. Enter a name in the space provided in the **New Capture** dialog box.

   The capture begins. When the capture is complete, the data is presented. An example of the captured data is shown in the screen shot examples below. Note that there is an **Event Plot** which is a graphical timeline depiction of the data. Alternatively you can view the data as a table in the **Event Table**. You can zoom in and out using the hour glass widgets.



#	Link Clock #	TimeStamp	Type
1	1	0:0:0.000.000.001.235	Version Information
2	1	0:0:0.000.000.001.235	Link Rate Change
3	5	0:0:0.000.000.006.173	Fill
4	14	0:0:0.000.000.017.284	BS
5	15	0:0:0.000.000.018.519	BF
6	16	0:0:0.000.000.019.753	BF
7	17	0:0:0.000.000.020.988	BS
8	18	0:0:0.000.000.022.222	BS Data
9	30	0:0:0.000.000.037.037	SS
10	31	0:0:0.000.000.038.272	SS
11	32	0:0:0.000.000.039.506	Capture Trigger
12	32	0:0:0.000.000.039.506	MSA
13	41	0:0:0.000.000.050.617	SE
14	49	0:0:0.000.000.060.494	SS
15	50	0:0:0.000.000.061.728	Audio Stream
16	62	0:0:0.000.000.076.543	SE
17	213	0:0:0.000.000.262.963	SS
18	214	0:0:0.000.000.264.198	Audio TimeStamp

1

Offset	L0	L1	L2	L3
+0	00	00	00	00
+1	00	00	00	00
+2	00	00	00	00
+3	00	00	00	00
+4	FE	FE	FE	FE
+5	EB	EB	EB	EB
+6	EB	EB	EB	EB
+7	10	10	10	10
+8	EB	EB	EB	EB
+9	EB	EB	EB	EB
+10	10	10	10	10
+11	EB	EB	EB	EB
+12	EB	EB	EB	EB
+13	BS	BS	BS	BS
+14	BF	BF	BF	BF
+15	BF	BF	BF	BF
+16	BS	BS	BS	BS
+17	01	01	01	01
+18	F0	F0	F0	F0
+19	00	00	00	00
+20	00	00	00	00
+21	00	00	00	00
+22	00	00	00	00
+23	00	00	00	00
+24	00	00	00	00
+25	00	00	00	00
+26	00	00	00	00
+27	00	00	00	00
+28	00	00	00	00
+29	SS	SS	SS	SS
+30	SS	SS	SS	SS
+31	00	00	00	00
+32	5D	5D	5D	5D
+33	F0	F0	F0	F0
+34	11	01	0F	00

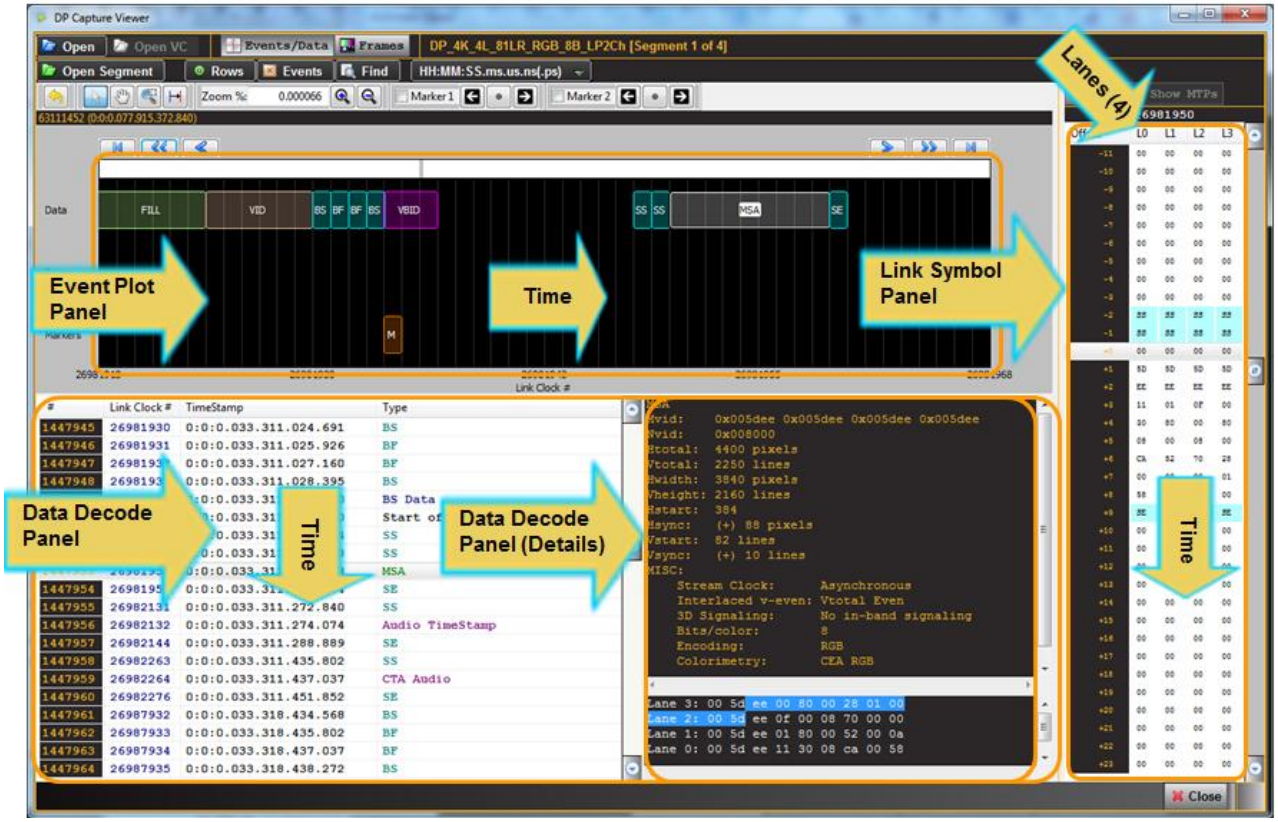
12.8 Capture Viewer Panels

The **Capture Viewer** enables you to locate data by searching for specific data types, panning, scrolling and zooming using various techniques. You can filter the data by type to limit the amount of data to sift through.

There are three (3) panels in the Capture Viewer:

- **Event Plot Panel** – Visual presentation of the audio, video, metadata, protocol and control elements.
- **Data Decode** (Transactions panel and Details panel) – Tabular chronology of audio, video, metadata, protocol and control elements with precise timestamps assigned. Enable serching and filtering.
- **Link Symbol Panel** – Table of link symbol values in hex for all lanes.

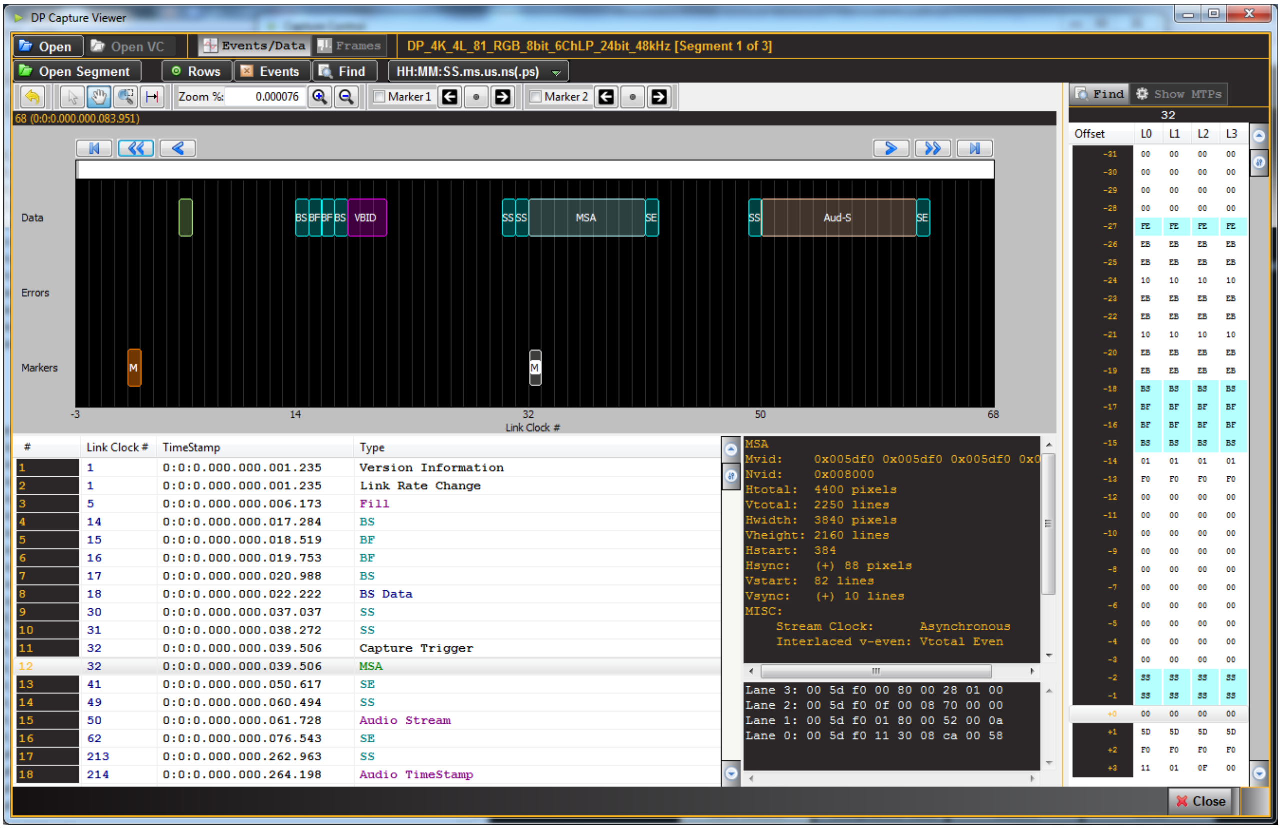
The panels are synchronized with one another. Refer to the screen capture and information below.



#	Link Clock #	TimeStamp	Type
1447945	26981930	0:0:0.033.311.024.691	BS
1447946	26981931	0:0:0.033.311.025.926	BF
1447947	269819[illegible]	0:0:0.033.311.027.160	BF
1447948	269819[illegible]	0:0:0.033.311.028.395	BS
[illegible]	[illegible]	[illegible]	BS Data
[illegible]	[illegible]	[illegible]	Start of
[illegible]	[illegible]	[illegible]	SS
[illegible]	[illegible]	[illegible]	SS
[illegible]	[illegible]	[illegible]	MSA
1447954	269819[illegible]	[illegible]	SE
1447955	26982131	0:0:0.033.311.272.840	SS
1447956	26982132	0:0:0.033.311.274.074	Audio TimeStamp
1447957	26982144	0:0:0.033.311.288.889	SE
1447958	26982263	0:0:0.033.311.435.802	SS
1447959	26982264	0:0:0.033.311.437.037	CTA Audio
1447960	26982276	0:0:0.033.311.451.852	SE
1447961	26987932	0:0:0.033.318.434.568	BS
1447962	26987933	0:0:0.033.318.435.802	BF
1447963	26987934	0:0:0.033.318.437.037	BF
1447964	26987935	0:0:0.033.318.438.272	BS

```
MSA
Mvid:    0x005dee 0x005dee 0x005dee 0x005dee
Nvid:    0x008000
Htotal:  4400 pixels
Vtotal:  2250 lines
Hwidth:  3840 pixels
Vheight: 2160 lines
Hstart:  384
Hsync:   (+) 88 pixels
Vstart:  82 lines
Vsync:   (+) 10 lines
MISC:
    Stream Clock:       Asynchronous
    Interlaced v-even: Vtotal Even
    3D Signaling:       No in-band signaling
    Bits/color:         8
    Encoding:           RGB
    Colorimetry:        CEA RGB
```

```
Lane 3: 00 5d ee 00 80 00 28 01 00
Lane 2: 00 5d ee 0f 00 08 70 00 00
Lane 1: 00 5d ee 01 80 00 52 00 0a
Lane 0: 00 5d ee 11 30 08 ca 00 58
```



#	Link Clock #	TimeStamp	Type
1	1	0:0:0.000.000.001.235	Version Information
2	1	0:0:0.000.000.001.235	Link Rate Change
3	5	0:0:0.000.000.006.173	Fill
4	14	0:0:0.000.000.017.284	BS
5	15	0:0:0.000.000.018.519	BF
6	16	0:0:0.000.000.019.753	BF
7	17	0:0:0.000.000.020.988	BS
8	18	0:0:0.000.000.022.222	BS Data
9	30	0:0:0.000.000.037.037	SS
10	31	0:0:0.000.000.038.272	SS
11	32	0:0:0.000.000.039.506	Capture Trigger
12	32	0:0:0.000.000.039.506	MSA
13	41	0:0:0.000.000.050.617	SE
14	49	0:0:0.000.000.060.494	SS
15	50	0:0:0.000.000.061.728	Audio Stream
16	62	0:0:0.000.000.076.543	SE
17	213	0:0:0.000.000.262.963	SS
18	214	0:0:0.000.000.264.198	Audio TimeStamp

```
MSA
Mvid:    0x005df0 0x005df0 0x005df0 0x0
Nvid:    0x008000
Htotal:  4400 pixels
Vtotal:  2250 lines
Hwidth:  3840 pixels
Vheight: 2160 lines
Hstart:  384
Hsync:   (+) 88 pixels
Vstart:  82 lines
Vsync:   (+) 10 lines
MISC:
    Stream Clock:      Asynchronous
    Interlaced v-even: Vtotal Even
```

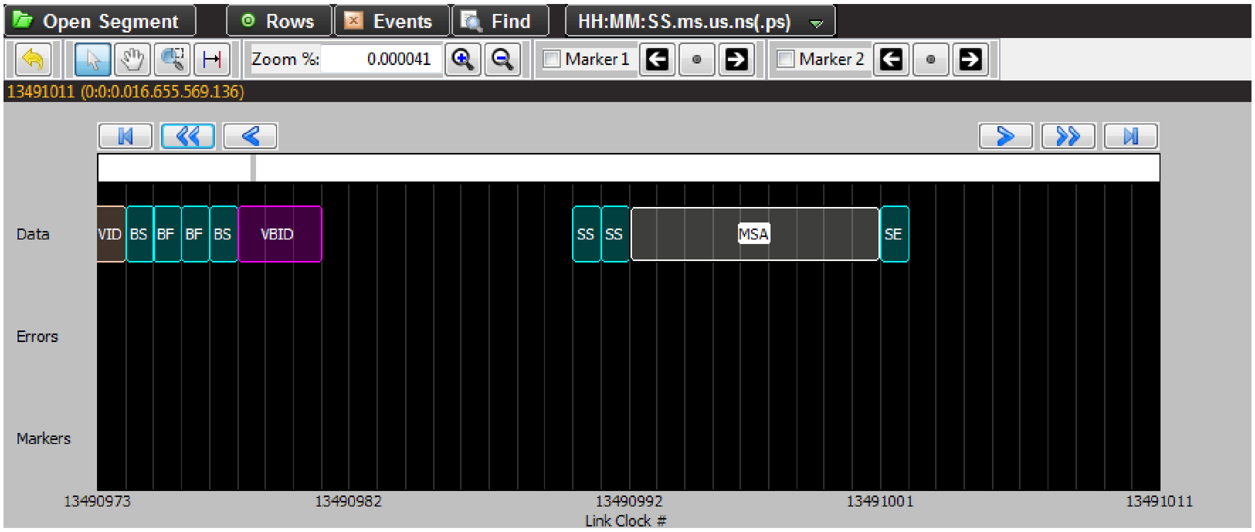
```
Lane 3: 00 5d f0 00 80 00 28 01 00
Lane 2: 00 5d f0 0f 00 08 70 00 00
Lane 1: 00 5d f0 01 80 00 52 00 0a
Lane 0: 00 5d f0 11 30 08 ca 00 58
```

32

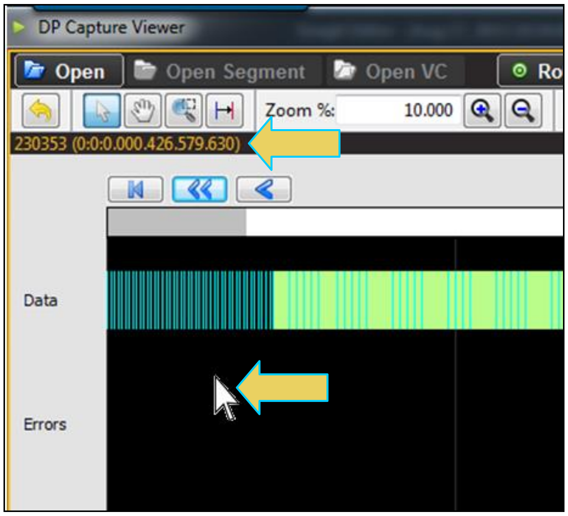
Offset	L0	L1	L2	L3
-31	00	00	00	00
-30	00	00	00	00
-29	00	00	00	00
-28	00	00	00	00
-27	FE	FE	FE	FE
-26	EB	EB	EB	EB
-25	EB	EB	EB	EB
-24	10	10	10	10
-23	EB	EB	EB	EB
-22	EB	EB	EB	EB
-21	10	10	10	10
-20	EB	EB	EB	EB
-19	EB	EB	EB	EB
-18	BS	BS	BS	BS
-17	BF	BF	BF	BF
-16	BF	BF	BF	BF
-15	BS	BS	BS	BS
-14	01	01	01	01
-13	F0	F0	F0	F0
-12	00	00	00	00
-11	00	00	00	00
-10	00	00	00	00
-9	00	00	00	00
-8	00	00	00	00
-7	00	00	00	00
-6	00	00	00	00
-5	00	00	00	00
-4	00	00	00	00
-3	00	00	00	00
-2	SS	SS	SS	SS
-1	SS	SS	SS	SS
+0	00	00	00	00
+1	5D	5D	5D	5D
+2	F0	F0	F0	F0
+3	11	01	0F	00

12.9 Event Plot Panel

The **Event Plot** is shown below. The **Event Plot** provides a graphical view of the captured data symbols. The vertical axis is the data types. The scale along the bottom shows the Link Clock number.



The timestamp of the cursor is shown near the top of the panel. As you move the pointer tool throughout the **Event Plot** panel the timestamp of the pointer's location is provided on the top of the panel as indicated below:



12.9.1 Scrolling in the Event Plot Panel

A scroll bar is provided to enable you to quickly browse through the data. The scroll bar is under the set of function icons just above the data panel where the data is displayed. You can also scroll to the end, scroll by page or scroll incrementally in either direction using the ⏮ ⏪ ◀ backward and forward activation ▶ ⏩ ⏭ buttons. See the screen shot below.

12.9.2 Zooming in the Event Plot Panel

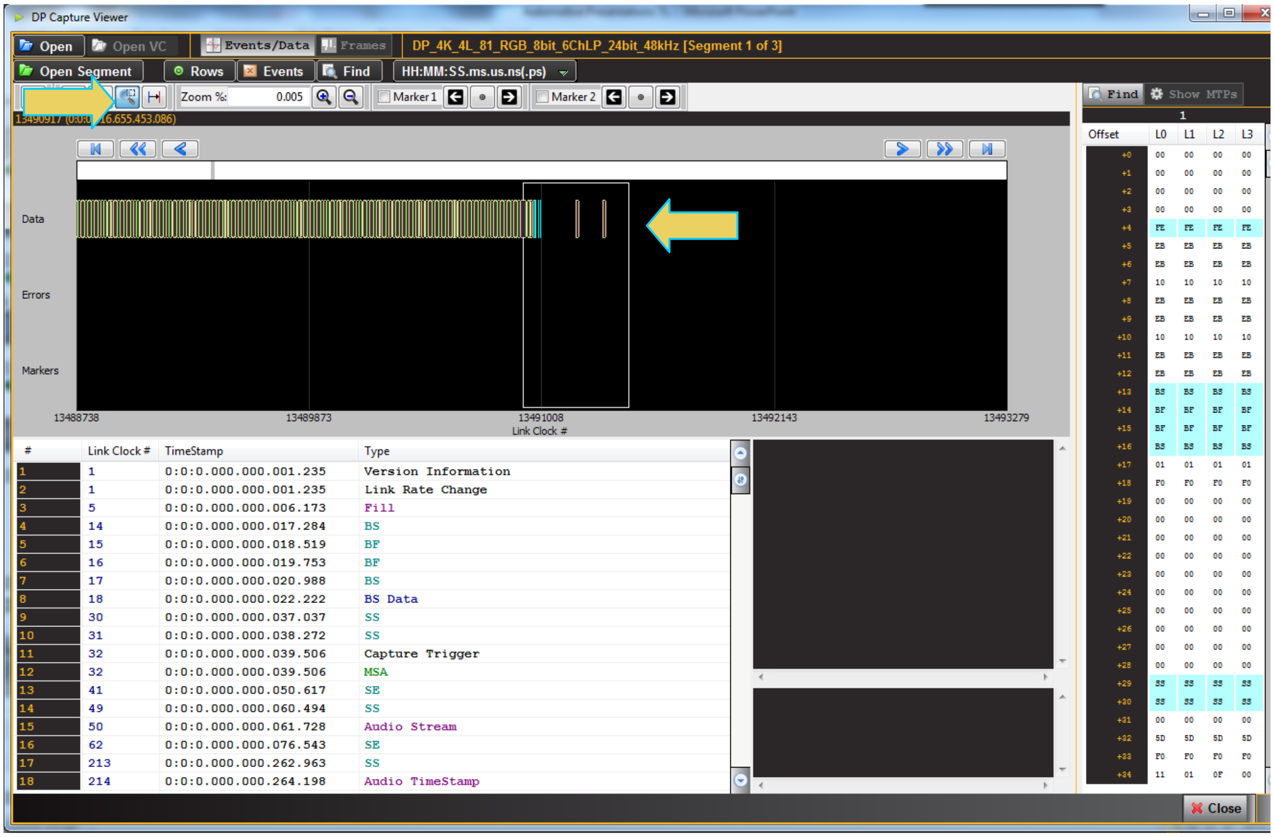
You can zoom in and zoom out and pan across the data using the slide bars provided. You can also zoom by surrounding a specific section of the captured data. These functions are described in the following table.

Even Plot Zoom & Panning Icons	Function
Icons – Zoom and Panning Zoom %: 2.500	▪ Back – The back icon enables you to return to the previous view. ▪ Pointer – The pointer icon enables you to click on any point and obtain information such as the data packet type and the timestamp, about that data packet. The information is displayed in a dark panel just above the scroll bar and below the icons. ▪ Panning – The panning function enables you scan across the data quickly by clicking and dragging. ▪ Surround activation button – You can select an area of the Event Plot by clicking and dragging across. When you do this the new view will be limited to the horizontal range that you selected. The midpoint of the selection will become the new center of the data displayed. ▪ Surround activation button – You can select an area of the Event Plot by clicking and dragging across. When you do this the

Even Plot Zoom & Panning Icons	Function
	new view will be limited to the horizontal range that you selected. The midpoint of the selection will become the new center of the data displayed. ▪ Zoom % – The Zoom % function enables you to enter a specific zoom amount in the associated field provided. ▪ Zoom In/Out icons 🔍 🔍 – The Zoom In/Out function buttons enables you to zoom in and zoom out by clicking on the activation button. The centered point will remain the same. ▪

12.9.3 Surrounding and Zooming

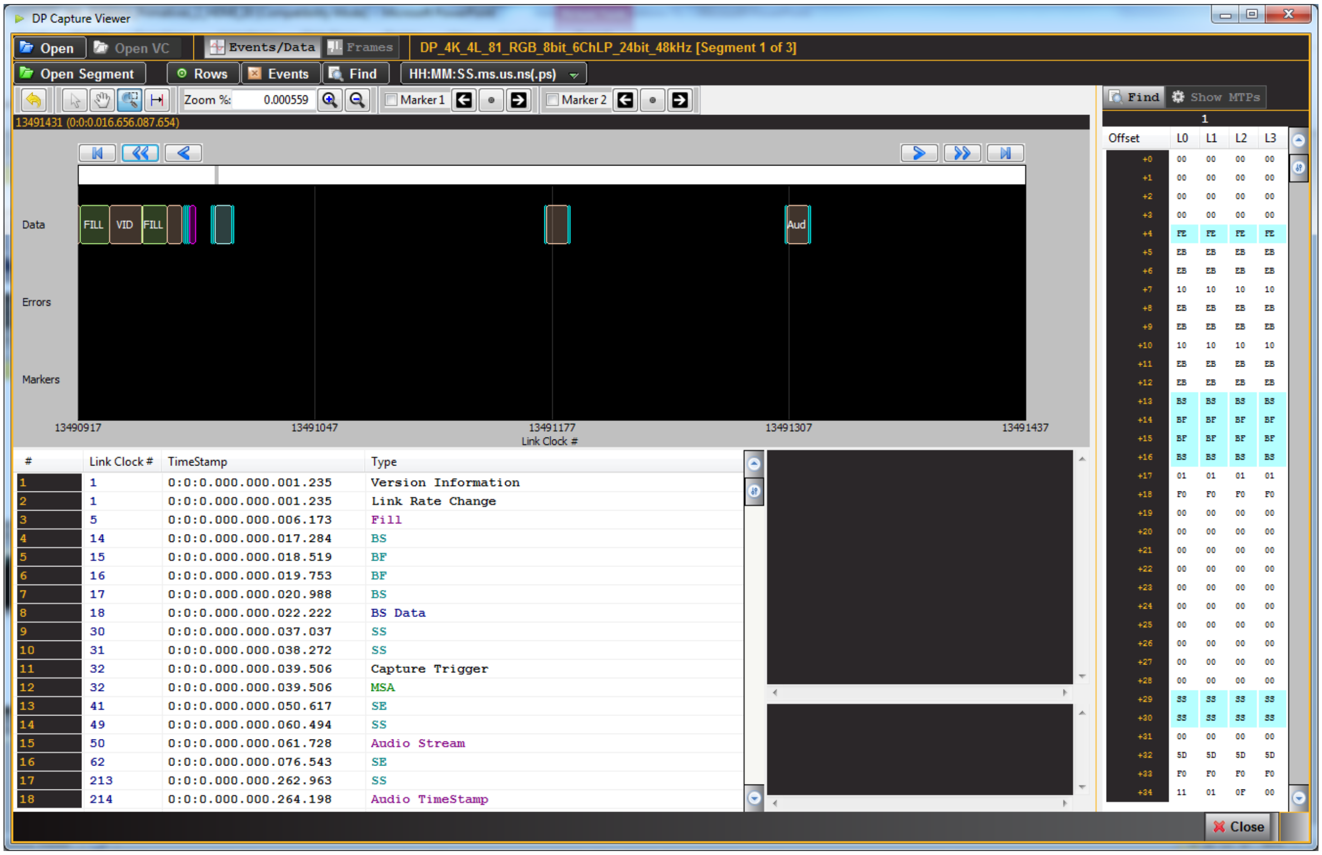
The **Event Plot** provides a Range Zoom tool 🔍. You can select an area of the **Event Plot** by clicking and dragging across. When you do this the new view will be limited to the horizontal range that you selected. The midpoint of the selection will become the new center of the data displayed. The two screens below show an example of surrounding a segment of data. The rectangle indicates the resultant section that is surrounded. The second view shows the resulting view.



#	Link Clock #	TimeStamp	Type
1	1	0:0:0.000.000.001.235	Version Information
2	1	0:0:0.000.000.001.235	Link Rate Change
3	5	0:0:0.000.000.006.173	Fill
4	14	0:0:0.000.000.017.284	BS
5	15	0:0:0.000.000.018.519	BF
6	16	0:0:0.000.000.019.753	BF
7	17	0:0:0.000.000.020.988	BS
8	18	0:0:0.000.000.022.222	BS Data
9	30	0:0:0.000.000.037.037	SS
10	31	0:0:0.000.000.038.272	SS
11	32	0:0:0.000.000.039.506	Capture Trigger
12	32	0:0:0.000.000.039.506	MSA
13	41	0:0:0.000.000.050.617	SE
14	49	0:0:0.000.000.060.494	SS
15	50	0:0:0.000.000.061.728	Audio Stream
16	62	0:0:0.000.000.076.543	SE
17	213	0:0:0.000.000.262.963	SS
18	214	0:0:0.000.000.264.198	Audio TimeStamp

	1			
Offset	L0	L1	L2	L3
+0	00	00	00	00
+1	00	00	00	00
+2	00	00	00	00
+3	00	00	00	00
+4	FE	FE	FE	FE
+5	EB	EB	EB	EB
+6	EB	EB	EB	EB
+7	10	10	10	10
+8	EB	EB	EB	EB
+9	EB	EB	EB	EB
+10	10	10	10	10
+11	EB	EB	EB	EB
+12	EB	EB	EB	EB
+13	BS	BS	BS	BS
+14	BF	BF	BF	BF
+15	BF	BF	BF	BF
+16	BS	BS	BS	BS
+17	01	01	01	01
+18	F0	F0	F0	F0
+19	00	00	00	00
+20	00	00	00	00
+21	00	00	00	00
+22	00	00	00	00
+23	00	00	00	00
+24	00	00	00	00
+25	00	00	00	00
+26	00	00	00	00
+27	00	00	00	00
+28	00	00	00	00
+29	SS	SS	SS	SS
+30	SS	SS	SS	SS
+31	00	00	00	00
+32	5D	5D	5D	5D
+33	F0	F0	F0	F0
+34	11	01	0F	00

The resulting screen is as follows:



#	Link Clock #	TimeStamp	Type
1	1	0:0:0.000.000.001.235	Version Information
2	1	0:0:0.000.000.001.235	Link Rate Change
3	5	0:0:0.000.000.006.173	Fill
4	14	0:0:0.000.000.017.284	BS
5	15	0:0:0.000.000.018.519	BF
6	16	0:0:0.000.000.019.753	BF
7	17	0:0:0.000.000.020.988	BS
8	18	0:0:0.000.000.022.222	BS Data
9	30	0:0:0.000.000.037.037	SS
10	31	0:0:0.000.000.038.272	SS
11	32	0:0:0.000.000.039.506	Capture Trigger
12	32	0:0:0.000.000.039.506	MSA
13	41	0:0:0.000.000.050.617	SE
14	49	0:0:0.000.000.060.494	SS
15	50	0:0:0.000.000.061.728	Audio Stream
16	62	0:0:0.000.000.076.543	SE
17	213	0:0:0.000.000.262.963	SS
18	214	0:0:0.000.000.264.198	Audio TimeStamp

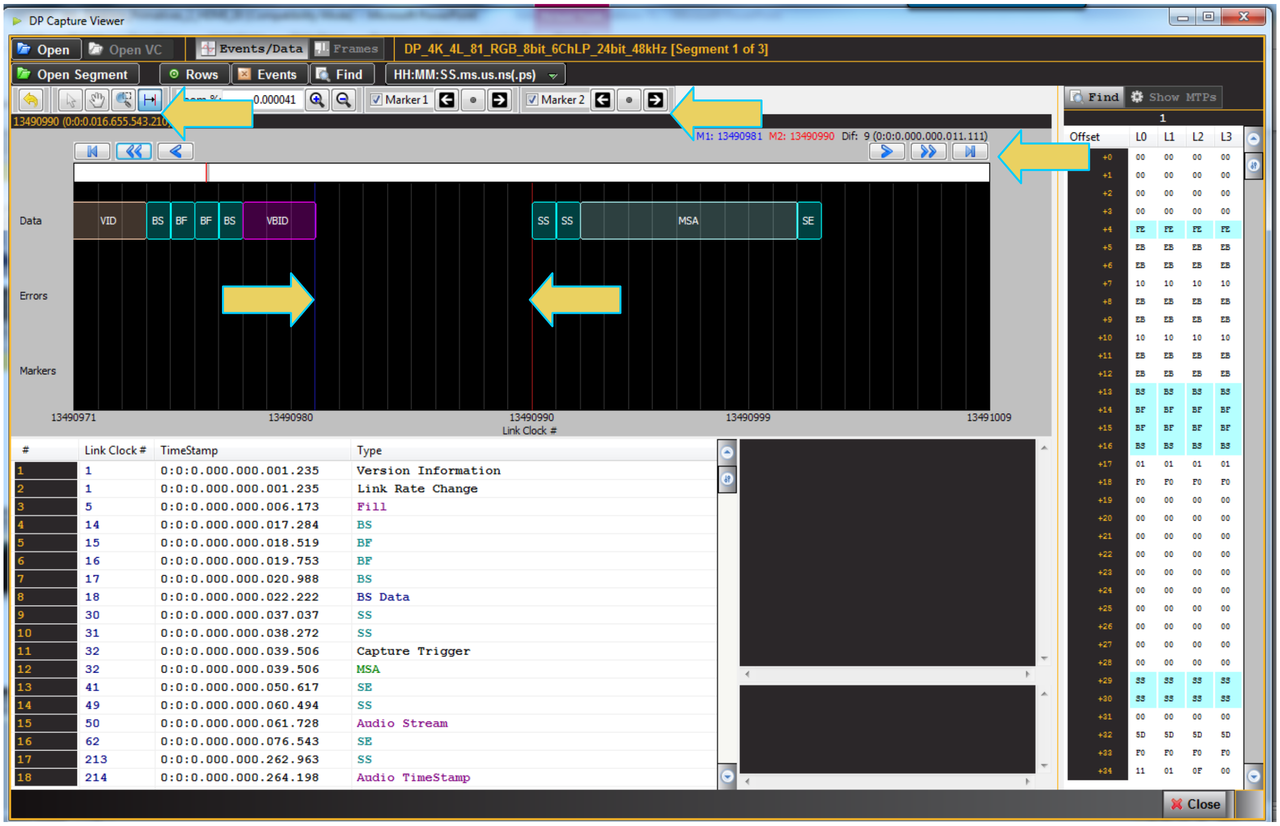
Offset	L0	L1	L2	L3
+0	00	00	00	00
+1	00	00	00	00
+2	00	00	00	00
+3	00	00	00	00
+4	FE	FE	FE	FE
+5	EB	EB	EB	EB
+6	EB	EB	EB	EB
+7	10	10	10	10
+8	EB	EB	EB	EB
+9	EB	EB	EB	EB
+10	10	10	10	10
+11	EB	EB	EB	EB
+12	EB	EB	EB	EB
+13	BS	BS	BS	BS
+14	BF	BF	BF	BF
+15	BF	BF	BF	BF
+16	BS	BS	BS	BS
+17	01	01	01	01
+18	F0	F0	F0	F0
+19	00	00	00	00
+20	00	00	00	00
+21	00	00	00	00
+22	00	00	00	00
+23	00	00	00	00
+24	00	00	00	00
+25	00	00	00	00
+26	00	00	00	00
+27	00	00	00	00
+28	00	00	00	00
+29	SS	SS	SS	SS
+30	SS	SS	SS	SS
+31	00	00	00	00
+32	5D	5D	5D	5D
+33	F0	F0	F0	F0
+34	11	01	0F	00

12.9.4 Working with Markers

The **Event Plot** panel enables you to view the data at a high level and identify points of interest for further analysis.

You can set two cursors or "markers" at particular points of interest using the Markers activation button ⊢. The **Event Plot** will show you the time difference between the two cursors. You can fine tune the position of the cursors with the left and right arrows associated with each marker ☐ Marker 1 ← ● →. The ● center icon allows you to center the particular marker on the center of the **Event Plot** window. The screens below show the markers being set and the resulting markers placed in the **Event Plot** panel.

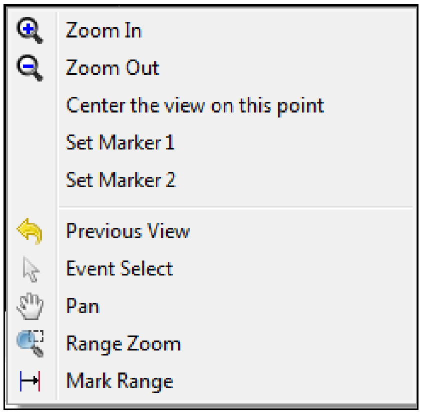
You can see the timestamp associated with each marker which are color coded (blue and red) just above the area where the data is shown. The dark text to the right shows the difference in microseconds and pixels between the two markers.



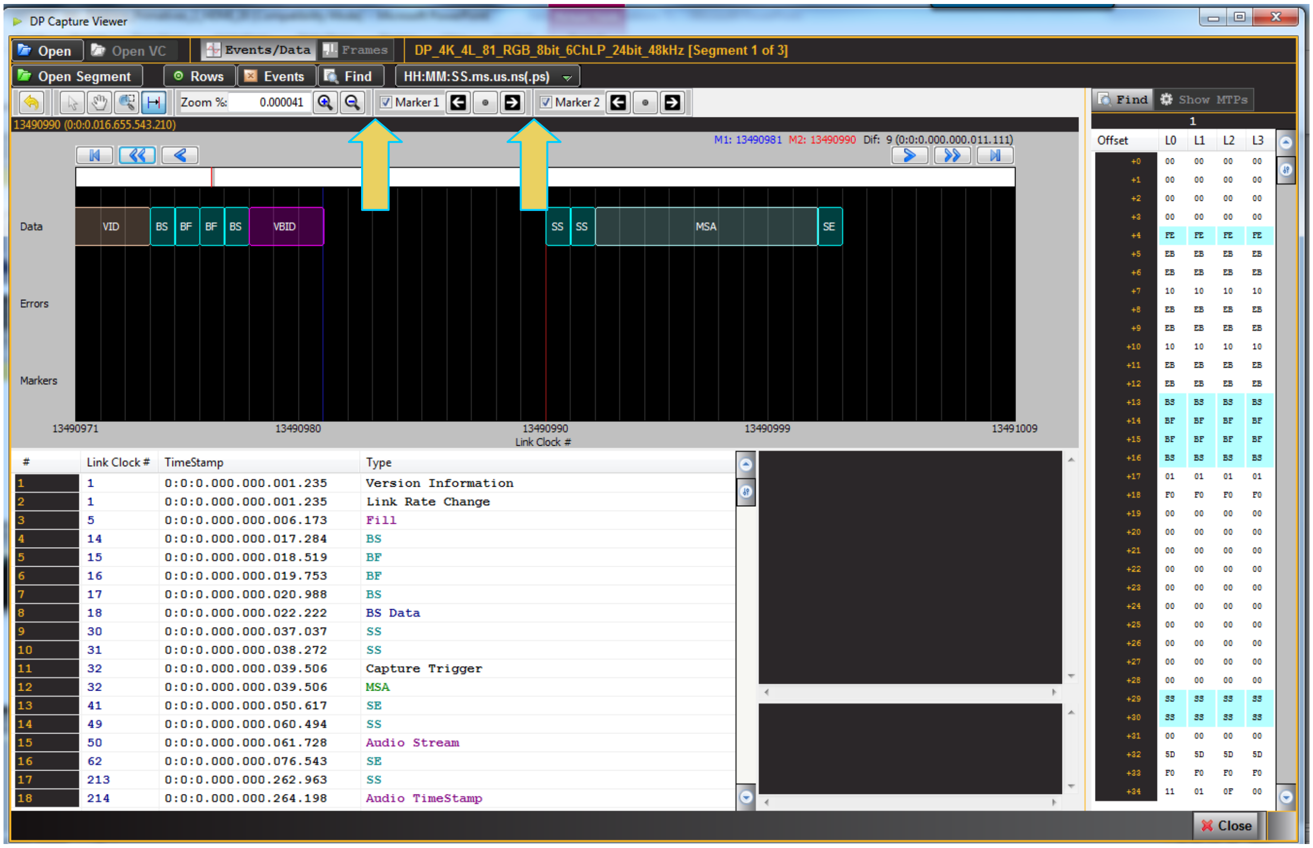
#	Link Clock #	TimeStamp	Type
1	1	0:0:0.000.000.001.235	Version Information
2	1	0:0:0.000.000.001.235	Link Rate Change
3	5	0:0:0.000.000.006.173	Fill
4	14	0:0:0.000.000.017.284	BS
5	15	0:0:0.000.000.018.519	BF
6	16	0:0:0.000.000.019.753	BF
7	17	0:0:0.000.000.020.988	BS
8	18	0:0:0.000.000.022.222	BS Data
9	30	0:0:0.000.000.037.037	SS
10	31	0:0:0.000.000.038.272	SS
11	32	0:0:0.000.000.039.506	Capture Trigger
12	32	0:0:0.000.000.039.506	MSA
13	41	0:0:0.000.000.050.617	SE
14	49	0:0:0.000.000.060.494	SS
15	50	0:0:0.000.000.061.728	Audio Stream
16	62	0:0:0.000.000.076.543	SE
17	213	0:0:0.000.000.262.963	SS
18	214	0:0:0.000.000.264.198	Audio TimeStamp

Offset	L0	L1	L2	L3
+0	00	00	00	00
+1	00	00	00	00
+2	00	00	00	00
+3	00	00	00	00
+4	FE	FE	FE	FE
+5	EB	EB	EB	EB
+6	EB	EB	EB	EB
+7	10	10	10	10
+8	EB	EB	EB	EB
+9	EB	EB	EB	EB
+10	10	10	10	10
+11	EB	EB	EB	EB
+12	EB	EB	EB	EB
+13	BS	BS	BS	BS
+14	BF	BF	BF	BF
+15	BF	BF	BF	BF
+16	BS	BS	BS	BS
+17	01	01	01	01
+18	F0	F0	F0	F0
+19	00	00	00	00
+20	00	00	00	00
+21	00	00	00	00
+22	00	00	00	00
+23	00	00	00	00
+24	00	00	00	00
+25	00	00	00	00
+26	00	00	00	00
+27	00	00	00	00
+28	00	00	00	00
+29	SS	SS	SS	SS
+30	SS	SS	SS	SS
+31	00	00	00	00
+32	5D	5D	5D	5D
+33	F0	F0	F0	F0
+34	11	01	0F	00

Note that you can also set the markers using the right click menu shown below:



You can remove the markers using the checkboxes associated with each **Marker** on the top menu bar. Refer to the screen example below.



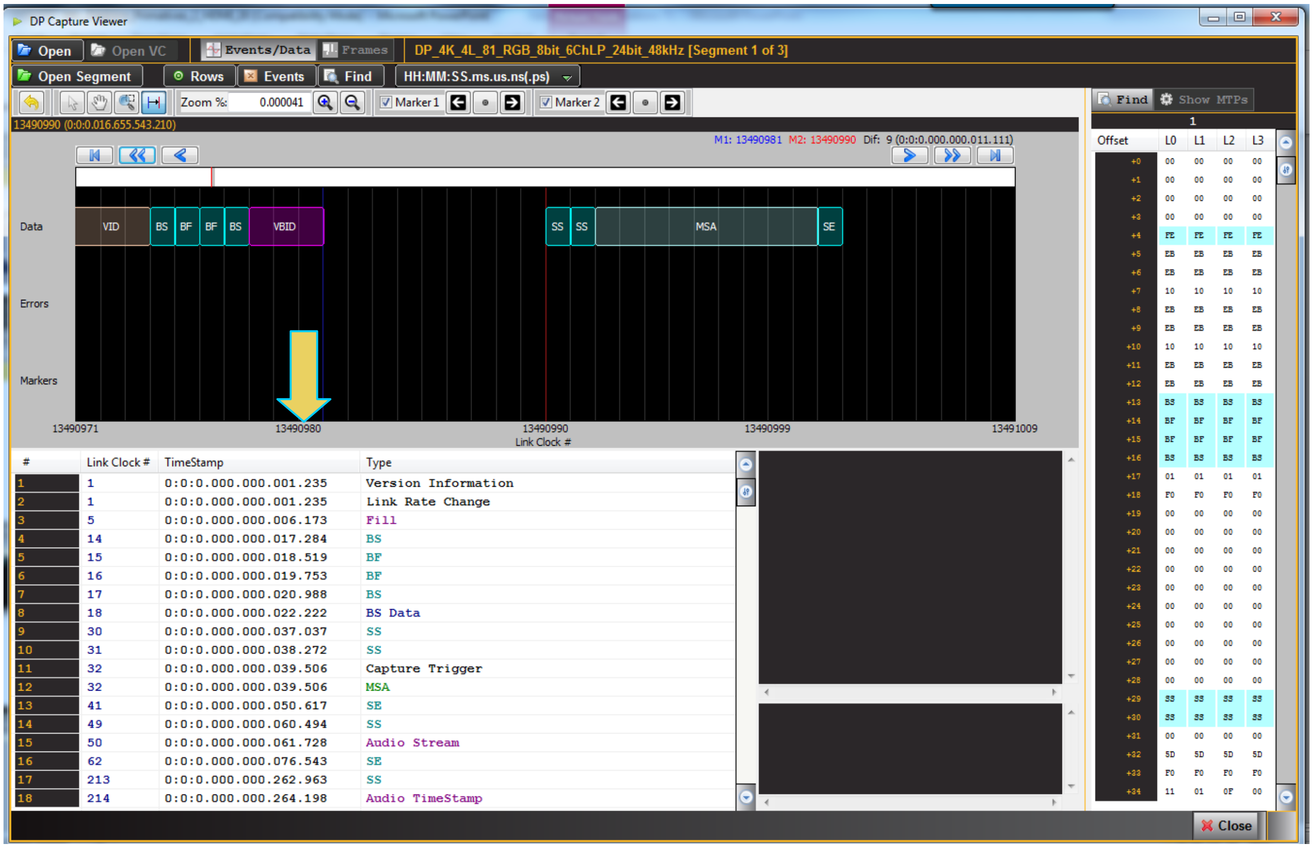
#	Link Clock #	TimeStamp	Type
1	1	0:0:0.000.000.001.235	Version Information
2	1	0:0:0.000.000.001.235	Link Rate Change
3	5	0:0:0.000.000.006.173	Fill
4	14	0:0:0.000.000.017.284	BS
5	15	0:0:0.000.000.018.519	BF
6	16	0:0:0.000.000.019.753	BF
7	17	0:0:0.000.000.020.988	BS
8	18	0:0:0.000.000.022.222	BS Data
9	30	0:0:0.000.000.037.037	SS
10	31	0:0:0.000.000.038.272	SS
11	32	0:0:0.000.000.039.506	Capture Trigger
12	32	0:0:0.000.000.039.506	MSA
13	41	0:0:0.000.000.050.617	SE
14	49	0:0:0.000.000.060.494	SS
15	50	0:0:0.000.000.061.728	Audio Stream
16	62	0:0:0.000.000.076.543	SE
17	213	0:0:0.000.000.262.963	SS
18	214	0:0:0.000.000.264.198	Audio TimeStamp

1

Offset	L0	L1	L2	L3
+0	00	00	00	00
+1	00	00	00	00
+2	00	00	00	00
+3	00	00	00	00
+4	FE	FE	FE	FE
+5	EB	EB	EB	EB
+6	EB	EB	EB	EB
+7	10	10	10	10
+8	EB	EB	EB	EB
+9	EB	EB	EB	EB
+10	10	10	10	10
+11	EB	EB	EB	EB
+12	EB	EB	EB	EB
+13	BS	BS	BS	BS
+14	BF	BF	BF	BF
+15	BF	BF	BF	BF
+16	BS	BS	BS	BS
+17	01	01	01	01
+18	F0	F0	F0	F0
+19	00	00	00	00
+20	00	00	00	00
+21	00	00	00	00
+22	00	00	00	00
+23	00	00	00	00
+24	00	00	00	00
+25	00	00	00	00
+26	00	00	00	00
+27	00	00	00	00
+28	00	00	00	00
+29	SS	SS	SS	SS
+30	SS	SS	SS	SS
+31	00	00	00	00
+32	5D	5D	5D	5D
+33	F0	F0	F0	F0
+34	11	01	0F	00

12.9.5 Link Clock timeline.

The Link clock symbol times are shown at the bottom of the **Event Plot** panel as indicated below.



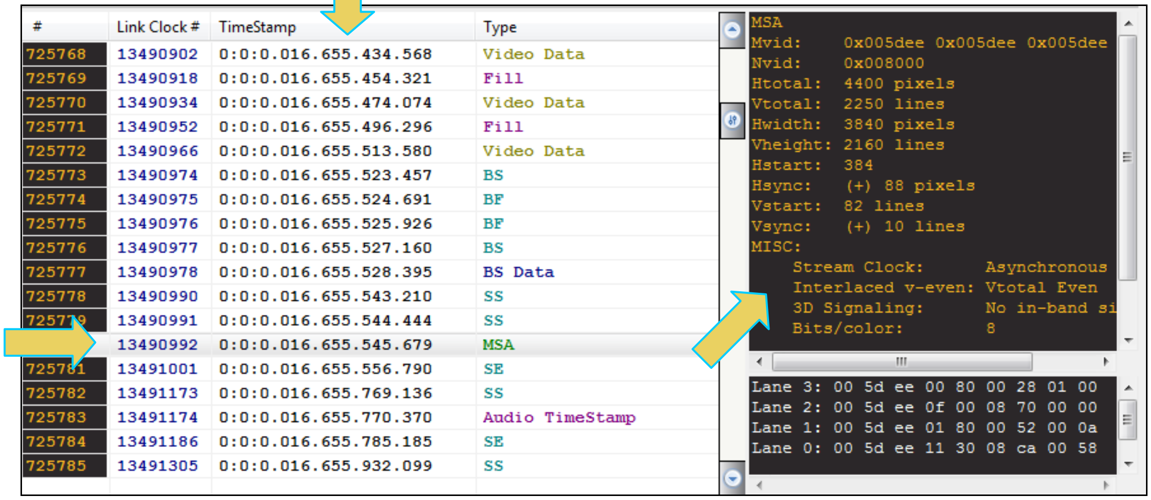
#	Link Clock #	TimeStamp	Type
1	1	0:0:0.000.000.001.235	Version Information
2	1	0:0:0.000.000.001.235	Link Rate Change
3	5	0:0:0.000.000.006.173	Fill
4	14	0:0:0.000.000.017.284	BS
5	15	0:0:0.000.000.018.519	BF
6	16	0:0:0.000.000.019.753	BF
7	17	0:0:0.000.000.020.988	BS
8	18	0:0:0.000.000.022.222	BS Data
9	30	0:0:0.000.000.037.037	SS
10	31	0:0:0.000.000.038.272	SS
11	32	0:0:0.000.000.039.506	Capture Trigger
12	32	0:0:0.000.000.039.506	MSA
13	41	0:0:0.000.000.050.617	SE
14	49	0:0:0.000.000.060.494	SS
15	50	0:0:0.000.000.061.728	Audio Stream
16	62	0:0:0.000.000.076.543	SE
17	213	0:0:0.000.000.262.963	SS
18	214	0:0:0.000.000.264.198	Audio TimeStamp

1

Offset	L0	L1	L2	L3
+0	00	00	00	00
+1	00	00	00	00
+2	00	00	00	00
+3	00	00	00	00
+4	FE	FE	FE	FE
+5	EB	EB	EB	EB
+6	EB	EB	EB	EB
+7	10	10	10	10
+8	EB	EB	EB	EB
+9	EB	EB	EB	EB
+10	10	10	10	10
+11	EB	EB	EB	EB
+12	EB	EB	EB	EB
+13	BS	BS	BS	BS
+14	BF	BF	BF	BF
+15	BF	BF	BF	BF
+16	BS	BS	BS	BS
+17	01	01	01	01
+18	F0	F0	F0	F0
+19	00	00	00	00
+20	00	00	00	00
+21	00	00	00	00
+22	00	00	00	00
+23	00	00	00	00
+24	00	00	00	00
+25	00	00	00	00
+26	00	00	00	00
+27	00	00	00	00
+28	00	00	00	00
+29	SS	SS	SS	SS
+30	SS	SS	SS	SS
+31	00	00	00	00
+32	5D	5D	5D	5D
+33	F0	F0	F0	F0
+34	11	01	0F	00

12.10 Data Decode Panel

The **Data Decode Panel** is shown below. The **Data Decode panel** provides a tabular or transactional view of the captured data symbols. When you highlight a transaction the information in the transaction appear in the Details panel to the right. The information in the Details panel is decoded in human readable text.



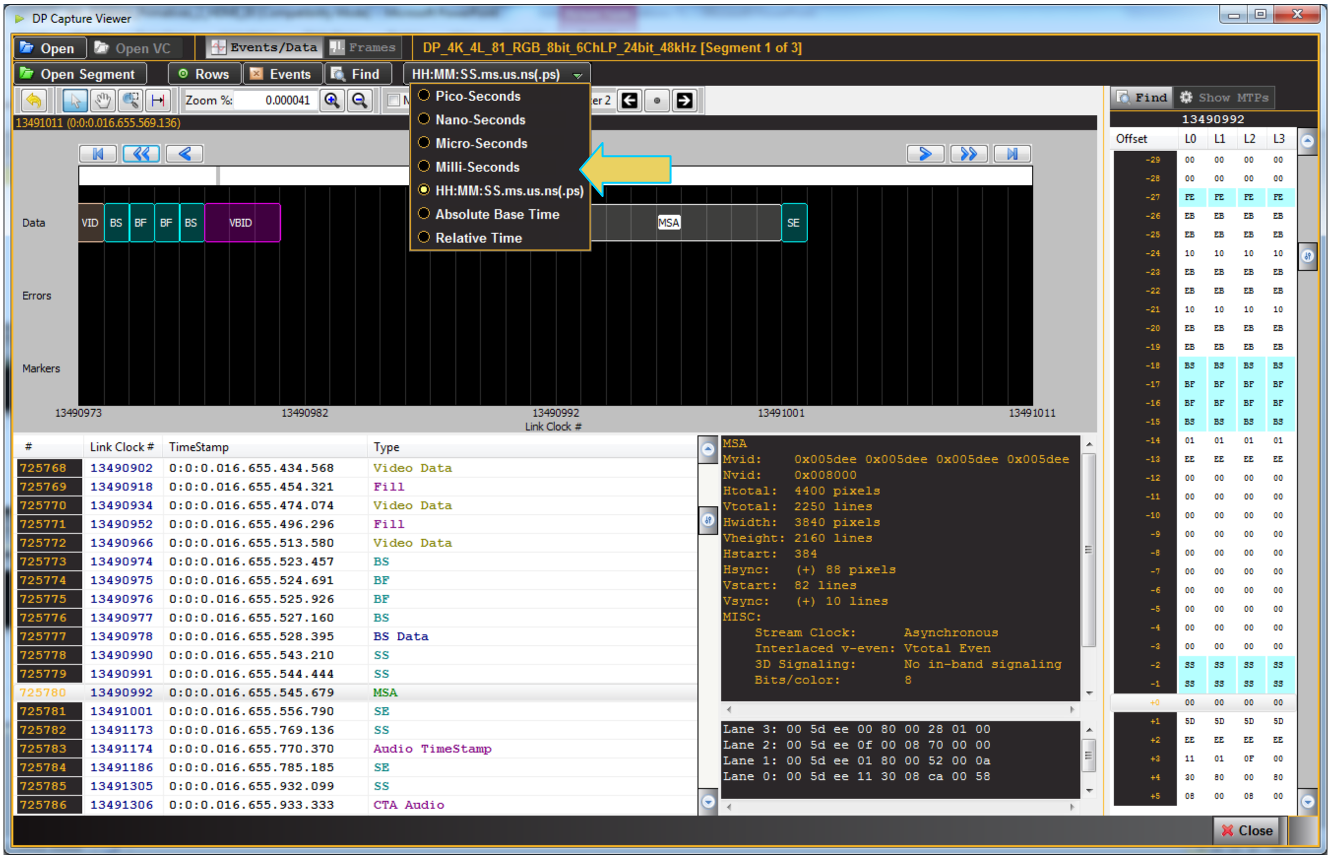
#	Link Clock #	TimeStamp	Type
725768	13490902	0:0:0.016.655.434.568	Video Data
725769	13490918	0:0:0.016.655.454.321	Fill
725770	13490934	0:0:0.016.655.474.074	Video Data
725771	13490952	0:0:0.016.655.496.296	Fill
725772	13490966	0:0:0.016.655.513.580	Video Data
725773	13490974	0:0:0.016.655.523.457	BS
725774	13490975	0:0:0.016.655.524.691	BF
725775	13490976	0:0:0.016.655.525.926	BF
725776	13490977	0:0:0.016.655.527.160	BS
725777	13490978	0:0:0.016.655.528.395	BS Data
725778	13490990	0:0:0.016.655.543.210	SS
725779	13490991	0:0:0.016.655.544.444	SS
	13490992	0:0:0.016.655.545.679	MSA
725781	13491001	0:0:0.016.655.556.790	SE
725782	13491173	0:0:0.016.655.769.136	SS
725783	13491174	0:0:0.016.655.770.370	Audio TimeStamp
725784	13491186	0:0:0.016.655.785.185	SE
725785	13491305	0:0:0.016.655.932.099	SS

```
MSA
Mvid:    0x005dee 0x005dee 0x005dee
Nvid:    0x008000
Htotal:  4400 pixels
Vtotal:  2250 lines
Hwidth:  3840 pixels
Vheight: 2160 lines
Hstart:  384
Hsync:   (+) 88 pixels
Vstart:  82 lines
Vsync:   (+) 10 lines
MISC:
    Stream Clock:       Asynchronous
    Interlaced v-even: Vtotal Even
    3D Signaling:       No in-band si
    Bits/color:         8
```

```
Lane 3: 00 5d ee 00 80 00 28 01 00
Lane 2: 00 5d ee 0f 00 08 70 00 00
Lane 1: 00 5d ee 01 80 00 52 00 0a
Lane 0: 00 5d ee 11 30 08 ca 00 58
```

12.10.1 Viewing and Setting the Timestamps of the Data Decode panel

You can set the timestamp values for pico, nano, micro or milliseconds using the pull-down menu at the top of the **Capture Viewer**. This pull-down menu is shown below. The default is to show times as hour, minutes, seconds and so on as in the examples. The Absolute Base Time will display a running time.



#	Link Clock #	TimeStamp	Type
725768	13490902	0:0:0.016.655.434.568	Video Data
725769	13490918	0:0:0.016.655.454.321	Fill
725770	13490934	0:0:0.016.655.474.074	Video Data
725771	13490952	0:0:0.016.655.496.296	Fill
725772	13490966	0:0:0.016.655.513.580	Video Data
725773	13490974	0:0:0.016.655.523.457	BS
725774	13490975	0:0:0.016.655.524.691	BF
725775	13490976	0:0:0.016.655.525.926	BF
725776	13490977	0:0:0.016.655.527.160	BS
725777	13490978	0:0:0.016.655.528.395	BS Data
725778	13490990	0:0:0.016.655.543.210	SS
725779	13490991	0:0:0.016.655.544.444	SS
725780	13490992	0:0:0.016.655.545.679	MSA
725781	13491001	0:0:0.016.655.556.790	SE
725782	13491173	0:0:0.016.655.769.136	SS
725783	13491174	0:0:0.016.655.770.370	Audio TimeStamp
725784	13491186	0:0:0.016.655.785.185	SE
725785	13491305	0:0:0.016.655.932.099	SS
725786	13491306	0:0:0.016.655.933.333	CTA Audio

```
MSA
Mvid:    0x005dee 0x005dee 0x005dee 0x005dee
Nvid:    0x008000
Htotal:  4400 pixels
Vtotal:  2250 lines
Hwidth:  3840 pixels
Vheight: 2160 lines
Hstart:  384
Hsync:   (+) 88 pixels
Vstart:  82 lines
Vsync:   (+) 10 lines
MISC:
    Stream Clock:       Asynchronous
    Interlaced v-even:  Vtotal Even
    3D Signaling:       No in-band signaling
    Bits/color:         8
```

```
Lane 3: 00 5d ee 00 80 00 28 01 00
Lane 2: 00 5d ee 0f 00 08 70 00 00
Lane 1: 00 5d ee 01 80 00 52 00 0a
Lane 0: 00 5d ee 11 30 08 ca 00 58
```

13490992

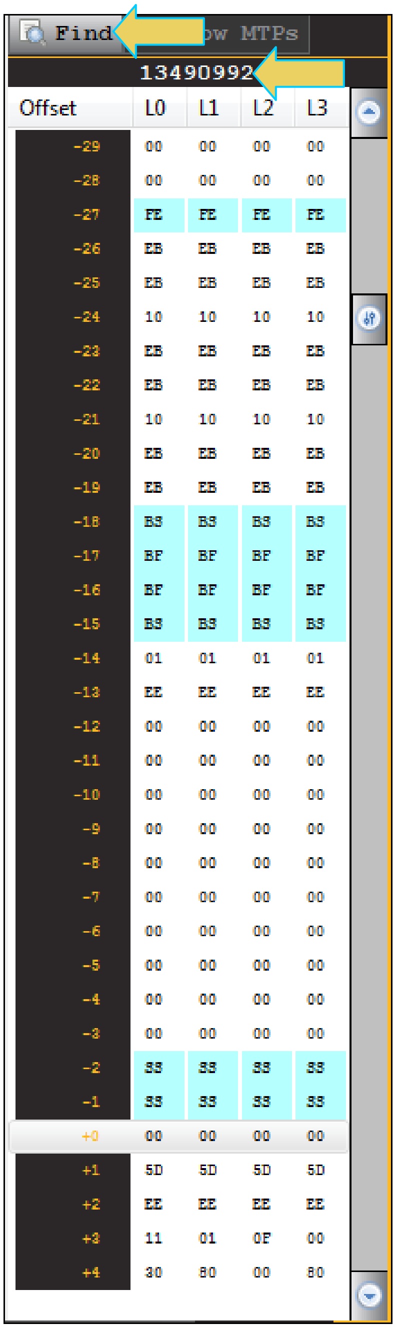
Offset	L0	L1	L2	L3
-29	00	00	00	00
-28	00	00	00	00
-27	FE	FE	FE	FE
-26	EB	EB	EB	EB
-25	EB	EB	EB	EB
-24	10	10	10	10
-23	EB	EB	EB	EB
-22	EB	EB	EB	EB
-21	10	10	10	10
-20	EB	EB	EB	EB
-19	EB	EB	EB	EB
-18	BS	BS	BS	BS
-17	BF	BF	BF	BF
-16	BF	BF	BF	BF
-15	BS	BS	BS	BS
-14	01	01	01	01
-13	EE	EE	EE	EE
-12	00	00	00	00
-11	00	00	00	00
-10	00	00	00	00
-9	00	00	00	00
-8	00	00	00	00
-7	00	00	00	00
-6	00	00	00	00
-5	00	00	00	00
-4	00	00	00	00
-3	00	00	00	00
-2	SS	SS	SS	SS
-1	SS	SS	SS	SS
+0	00	00	00	00
+1	5D	5D	5D	5D
+2	EE	EE	EE	EE
+3	11	01	0F	00
+4	30	80	00	80
+5	08	00	08	00

12.11 Link Symbol Panel

The **Link Symbol Panel** is shown below. The **Link Symbol Panel** provides an event list of all the raw link symbols in the capture for each lane. The data for each lane is presented in a separate column.

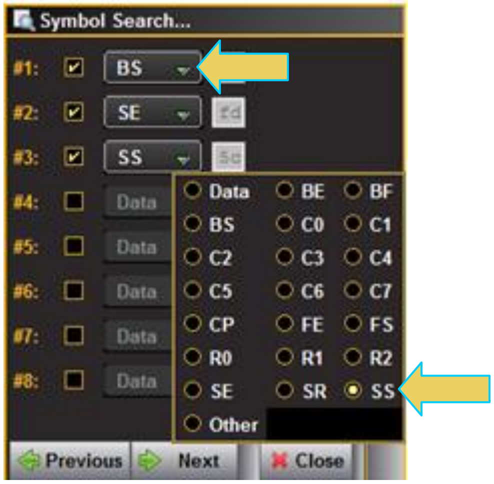
When you double click on a link symbol, the offset is reset to zero at that link symbol and the other two panels are then synchronized to that that point in the capture. The Link Symbol that is synchronized to is presented at the top of the panel as indicated below.

The Find button enables you to search for any type of control element. The Find dialog box is shown below with the Blanking Start (BS) control element selected. You can then search through the Link Symbol panel for all occurrences of that symbol or any other. You can select multiple symbol types as indicated below



13490992

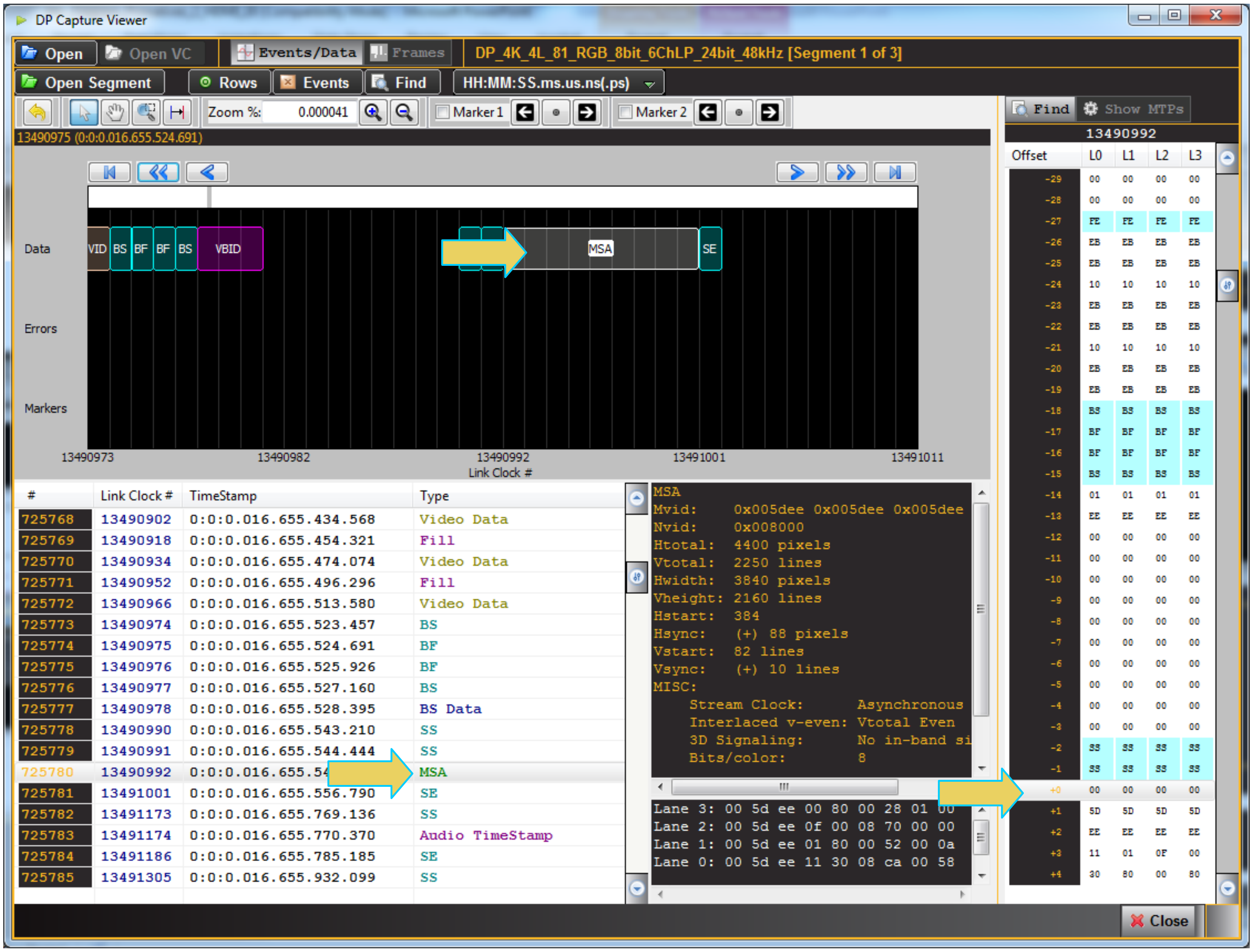
Offset	L0	L1	L2	L3
-29	00	00	00	00
-28	00	00	00	00
-27	FE	FE	FE	FE
-26	EB	EB	EB	EB
-25	EB	EB	EB	EB
-24	10	10	10	10
-23	EB	EB	EB	EB
-22	EB	EB	EB	EB
-21	10	10	10	10
-20	EB	EB	EB	EB
-19	EB	EB	EB	EB
-18	BS	BS	BS	BS
-17	BF	BF	BF	BF
-16	BF	BF	BF	BF
-15	BS	BS	BS	BS
-14	01	01	01	01
-13	EE	EE	EE	EE
-12	00	00	00	00
-11	00	00	00	00
-10	00	00	00	00
-9	00	00	00	00
-8	00	00	00	00
-7	00	00	00	00
-6	00	00	00	00
-5	00	00	00	00
-4	00	00	00	00
-3	00	00	00	00
-2	SS	SS	SS	SS
-1	SS	SS	SS	SS
+0	00	00	00	00
+1	5D	5D	5D	5D
+2	EE	EE	EE	EE
+3	11	01	0F	00
+4	30	80	00	80



#1: ☑ BS
#2: ☑ SE
#3: ☑ SS
#4: ☐ Data
#5: ☐ Data
#6: ☐ Data
#7: ☐ Data
#8: ☐ Data

12.11.1 Panel Synchronization

Each of the three panels are always automatically in sync with one another.



#	Link Clock #	TimeStamp	Type
725768	13490902	0:0:0.016.655.434.568	Video Data
725769	13490918	0:0:0.016.655.454.321	Fill
725770	13490934	0:0:0.016.655.474.074	Video Data
725771	13490952	0:0:0.016.655.496.296	Fill
725772	13490966	0:0:0.016.655.513.580	Video Data
725773	13490974	0:0:0.016.655.523.457	BS
725774	13490975	0:0:0.016.655.524.691	BF
725775	13490976	0:0:0.016.655.525.926	BF
725776	13490977	0:0:0.016.655.527.160	BS
725777	13490978	0:0:0.016.655.528.395	BS Data
725778	13490990	0:0:0.016.655.543.210	SS
725779	13490991	0:0:0.016.655.544.444	SS
725780	13490992	0:0:0.016.655.54	MSA
725781	13491001	0:0:0.016.655.556.790	SE
725782	13491173	0:0:0.016.655.769.136	SS
725783	13491174	0:0:0.016.655.770.370	Audio TimeStamp
725784	13491186	0:0:0.016.655.785.185	SE
725785	13491305	0:0:0.016.655.932.099	SS

```
MSA
Mvid:    0x005dee 0x005dee 0x005dee
Nvid:    0x008000
Htotal:  4400 pixels
Vtotal:  2250 lines
Hwidth:  3840 pixels
Vheight: 2160 lines
Hstart:  384
Hsync:   (+) 88 pixels
Vstart:  82 lines
Vsync:   (+) 10 lines
MISC:
    Stream Clock:        Asynchronous
    Interlaced v-even:  Vtotal Even
    3D Signaling:        No in-band si
    Bits/color:          8
```

```
Lane 3: 00 5d ee 00 80 00 28 01 00
Lane 2: 00 5d ee 0f 00 08 70 00 00
Lane 1: 00 5d ee 01 80 00 52 00 0a
Lane 0: 00 5d ee 11 30 08 ca 00 58
```

13490992

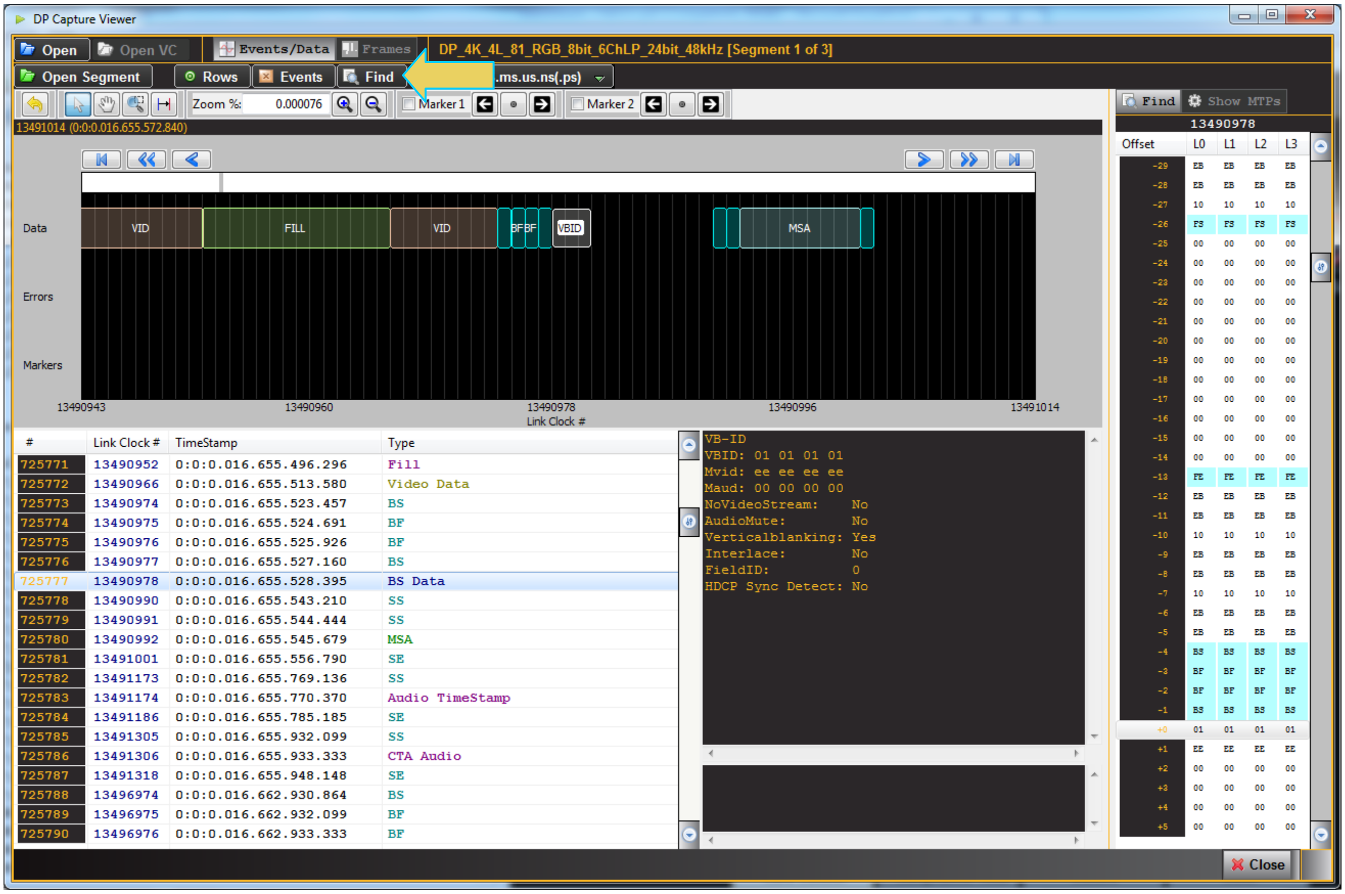
Offset	L0	L1	L2	L3
-29	00	00	00	00
-28	00	00	00	00
-27	FE	FE	FE	FE
-26	EB	EB	EB	EB
-25	EB	EB	EB	EB
-24	10	10	10	10
-23	EB	EB	EB	EB
-22	EB	EB	EB	EB
-21	10	10	10	10
-20	EB	EB	EB	EB
-19	EB	EB	EB	EB
-18	BS	BS	BS	BS
-17	BF	BF	BF	BF
-16	BF	BF	BF	BF
-15	BS	BS	BS	BS
-14	01	01	01	01
-13	EE	EE	EE	EE
-12	00	00	00	00
-11	00	00	00	00
-10	00	00	00	00
-9	00	00	00	00
-8	00	00	00	00
-7	00	00	00	00
-6	00	00	00	00
-5	00	00	00	00
-4	00	00	00	00
-3	00	00	00	00
-2	SS	SS	SS	SS
-1	SS	SS	SS	SS
+0	00	00	00	00
+1	5D	5D	5D	5D
+2	EE	EE	EE	EE
+3	11	01	0F	00
+4	30	80	00	80

12.12 Searching and Filtering for Specific Data Elements

You can locate data items by browsing either through the **Event Plot** view of the **Event Data** table. The two windows (**Event Plot** and **Event Table**) are in sync as you browse, search or select an item.

12.12.1 Event Search

You can locate specific data types using the **Event Search** feature in either the **Event Plot** or the **Event Table**. The following screen shot is a typical example of captured data. The **Event Search** dialog box is accessible from the **Find** Find activation button on the top of the **DP Capture Viewer** window as shown below.



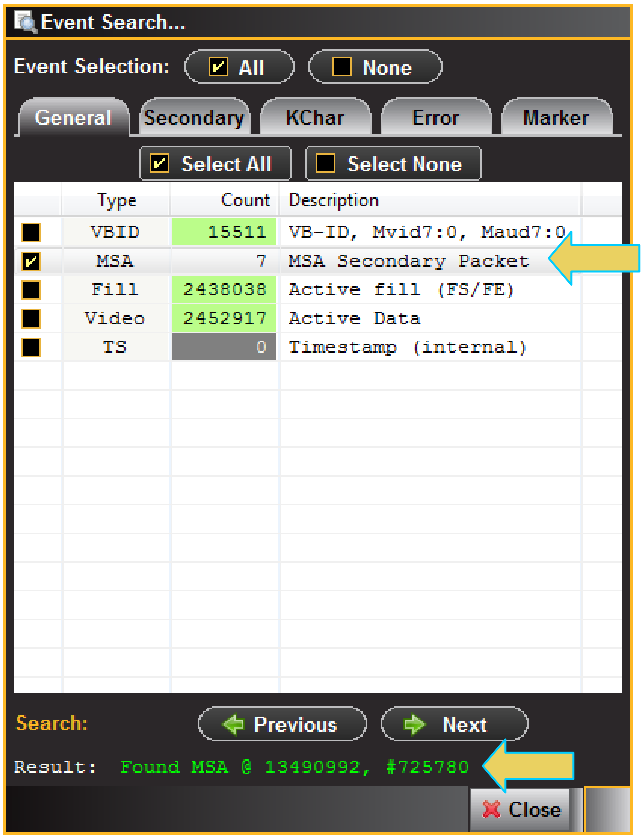
#	Link Clock #	TimeStamp	Type
725771	13490952	0:0:0.016.655.496.296	Fill
725772	13490966	0:0:0.016.655.513.580	Video Data
725773	13490974	0:0:0.016.655.523.457	BS
725774	13490975	0:0:0.016.655.524.691	BF
725775	13490976	0:0:0.016.655.525.926	BF
725776	13490977	0:0:0.016.655.527.160	BS
725777	13490978	0:0:0.016.655.528.395	BS Data
725778	13490990	0:0:0.016.655.543.210	SS
725779	13490991	0:0:0.016.655.544.444	SS
725780	13490992	0:0:0.016.655.545.679	MSA
725781	13491001	0:0:0.016.655.556.790	SE
725782	13491173	0:0:0.016.655.769.136	SS
725783	13491174	0:0:0.016.655.770.370	Audio TimeStamp
725784	13491186	0:0:0.016.655.785.185	SE
725785	13491305	0:0:0.016.655.932.099	SS
725786	13491306	0:0:0.016.655.933.333	CTA Audio
725787	13491318	0:0:0.016.655.948.148	SE
725788	13496974	0:0:0.016.662.930.864	BS
725789	13496975	0:0:0.016.662.932.099	BF
725790	13496976	0:0:0.016.662.933.333	BF

```
VB-ID
VBID: 01 01 01 01
Mvid: ee ee ee ee
Maud: 00 00 00 00
NoVideoStream:    No
AudioMute:        No
Verticalblanking: Yes
Interlace:        No
FieldID:          0
HDCP Sync Detect: No
```

13490978

Offset	L0	L1	L2	L3
-29	EB	EB	EB	EB
-28	EB	EB	EB	EB
-27	10	10	10	10
-26	FS	FS	FS	FS
-25	00	00	00	00
-24	00	00	00	00
-23	00	00	00	00
-22	00	00	00	00
-21	00	00	00	00
-20	00	00	00	00
-19	00	00	00	00
-18	00	00	00	00
-17	00	00	00	00
-16	00	00	00	00
-15	00	00	00	00
-14	00	00	00	00
-13	FE	FE	FE	FE
-12	EB	EB	EB	EB
-11	EB	EB	EB	EB
-10	10	10	10	10
-9	EB	EB	EB	EB
-8	EB	EB	EB	EB
-7	10	10	10	10
-6	EB	EB	EB	EB
-5	EB	EB	EB	EB
-4	BS	BS	BS	BS
-3	BF	BF	BF	BF
-2	BF	BF	BF	BF
-1	BS	BS	BS	BS
+0	01	01	01	01
+1	EE	EE	EE	EE
+2	00	00	00	00
+3	00	00	00	00
+4	00	00	00	00
+5	00	00	00	00

12.12.2 The **Event Search** dialog box is shown below. You can search for specific data types using the tabs and the check boxes within each tab.



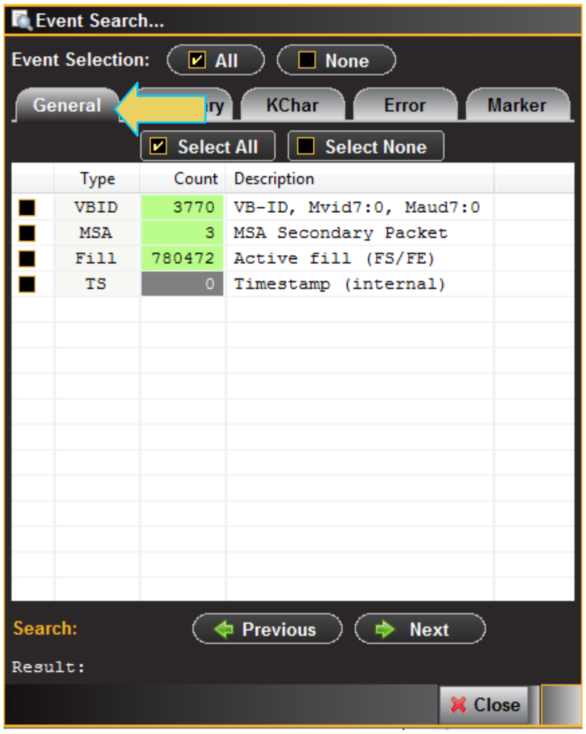
	Type	Count	Description
☐	VBID	15511	VB-ID, Mvid7:0, Maud7:0
☑	MSA	7	MSA Secondary Packet
☐	Fill	2438038	Active fill (FS/FE)
☐	Video	2452917	Active Data
☐	TS	0	Timestamp (internal)

Result: Found MSA @ 13490992, #725780

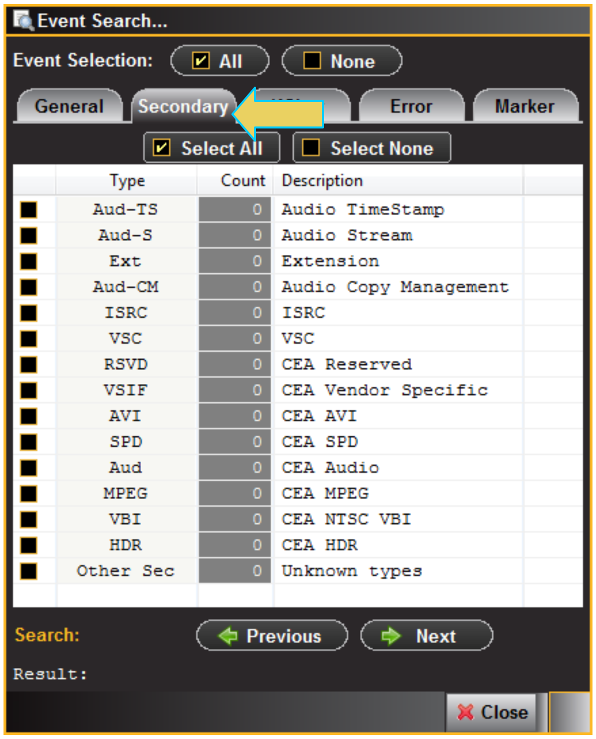
The dialog box enables you to select all or none of the data element types either per tab using the **Event Selection** buttons on the top of the dialog box Event Selection: ☑ All ☐ None, or all or none of the data elements of a particular tab ☑ Select All ☐ Select None. You can navigate through the data elements that you have indicated in the search using the Previous and Next buttons Previous Next.

The results of a search are shown below under **Results** indicated above.

Several example screen shots of the **Event Search** dialog box are shown below. There are several tabs at the top. Each tab enables you to select from a category of data types. The examples show all the data elements that can be specified for a search. Note that the **Count** is an indication of the number of that data element that appears in the captured data.

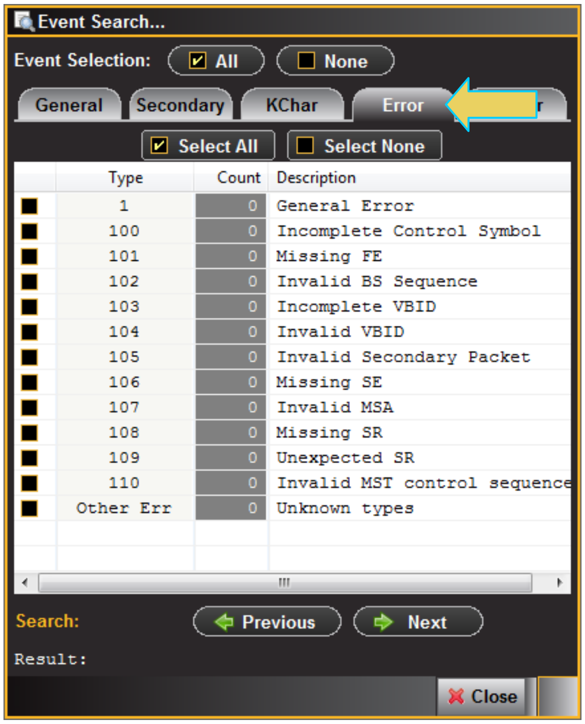


	Type	Count	Description
■	VBID	3770	VB-ID, Mvid7:0, Maud7:0
■	MSA	3	MSA Secondary Packet
■	Fill	780472	Active fill (FS/FE)
■	TS	0	Timestamp (internal)



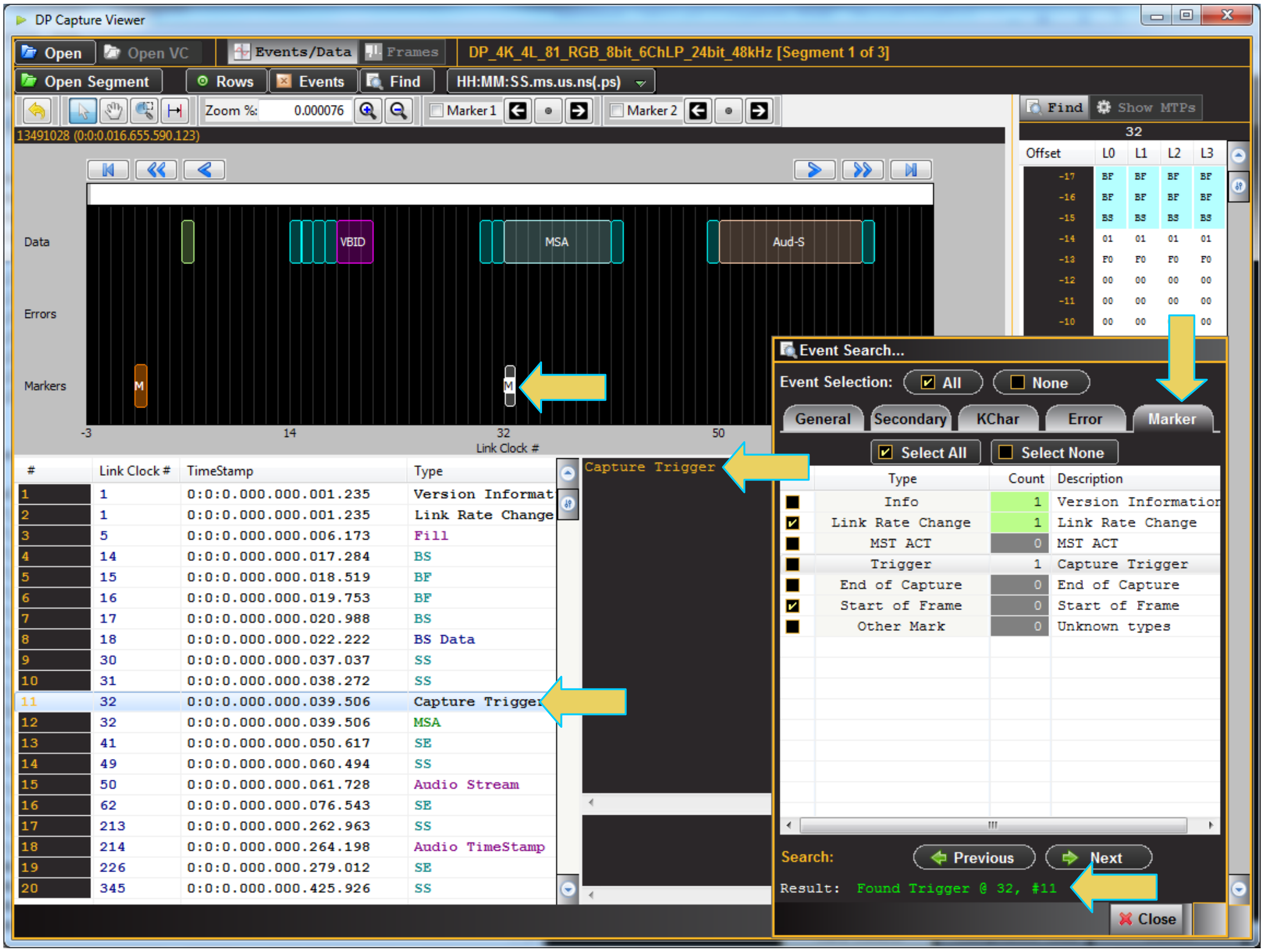
	Type	Count	Description
■	Aud-TS	0	Audio TimeStamp
■	Aud-S	0	Audio Stream
■	Ext	0	Extension
■	Aud-CM	0	Audio Copy Management
■	ISRC	0	ISRC
■	VSC	0	VSC
■	RSVD	0	CEA Reserved
■	VSIF	0	CEA Vendor Specific
■	AVI	0	CEA AVI
■	SPD	0	CEA SPD
■	Aud	0	CEA Audio
■	MPEG	0	CEA MPEG
■	VBI	0	CEA NTSC VBI
■	HDR	0	CEA HDR
■	Other Sec	0	Unknown types

	Type	Count	Description
■	SR	16	Scrambler Reset
■	SS	6	Secondary-data Start
■	R0	0	Reserved 0
■	BS	7524	Blanking Start
■	R1	0	Reserved 1
■	R2	0	Reserved 2
■	BE	3591	Blanking End
■	SE	4	Secondary-data End
■	CP	0	CP Symbol
☑	BF	7540	BF Symbol
■	Other KChar	0	Unknown types



	Type	Count	Description
■	1	0	General Error
■	100	0	Incomplete Control Symbol
■	101	0	Missing FE
■	102	0	Invalid BS Sequence
■	103	0	Incomplete VBID
■	104	0	Invalid VBID
■	105	0	Invalid Secondary Packet
■	106	0	Missing SE
■	107	0	Invalid MSA
■	108	0	Missing SR
■	109	0	Unexpected SR
■	110	0	Invalid MST control sequence
■	Other Err	0	Unknown types

In the following example, the **Trigger** condition **Marker** is searched for. Note that the status of the search is shown on the bottom of the dialog box. The search function centered the trigger condition marker on the Event Plot which you can partially see behind the dialog box.



#	Link Clock #	TimeStamp	Type
1	1	0:0:0.000.000.001.235	Version Informat
2	1	0:0:0.000.000.001.235	Link Rate Change
3	5	0:0:0.000.000.006.173	Fill
4	14	0:0:0.000.000.017.284	BS
5	15	0:0:0.000.000.018.519	BF
6	16	0:0:0.000.000.019.753	BF
7	17	0:0:0.000.000.020.988	BS
8	18	0:0:0.000.000.022.222	BS Data
9	30	0:0:0.000.000.037.037	SS
10	31	0:0:0.000.000.038.272	SS
11	32	0:0:0.000.000.039.506	Capture Trigger
12	32	0:0:0.000.000.039.506	MSA
13	41	0:0:0.000.000.050.617	SE
14	49	0:0:0.000.000.060.494	SS
15	50	0:0:0.000.000.061.728	Audio Stream
16	62	0:0:0.000.000.076.543	SE
17	213	0:0:0.000.000.262.963	SS
18	214	0:0:0.000.000.264.198	Audio TimeStamp
19	226	0:0:0.000.000.279.012	SE
20	345	0:0:0.000.000.425.926	SS

Offset	L0	L1	L2	L3
-17	BF	BF	BF	BF
-16	BF	BF	BF	BF
-15	BS	BS	BS	BS
-14	01	01	01	01
-13	F0	F0	F0	F0
-12	00	00	00	00
-11	00	00	00	00
-10	00	00	[illegible]	00

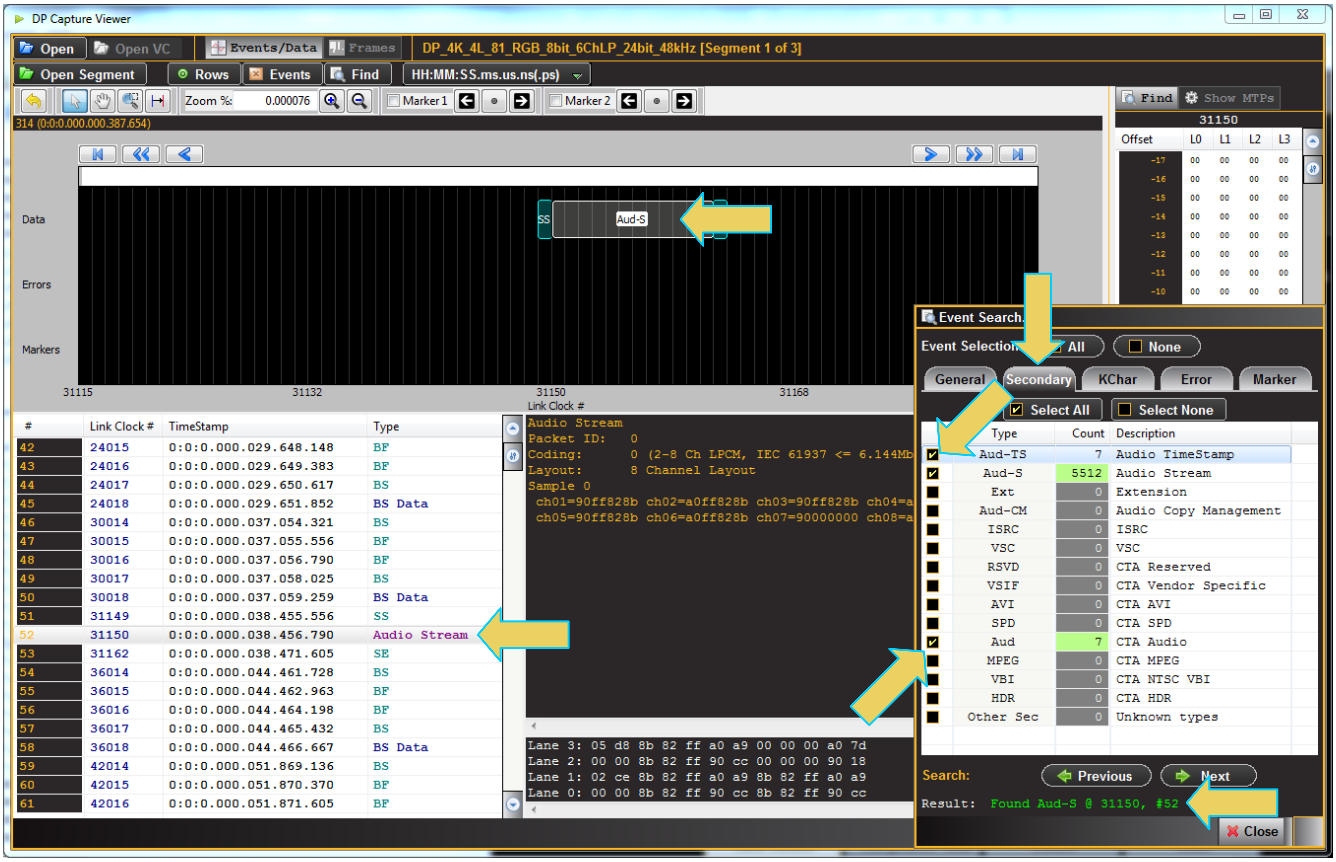
Event Selection: ☑ All ☐ None

☑ Select All ☐ Select None

	Type	Count	Description
☐	Info	1	Version Informatio
☑	Link Rate Change	1	Link Rate Change
☐	MST ACT	0	MST ACT
☐	Trigger	1	Capture Trigger
☐	End of Capture	0	End of Capture
☑	Start of Frame	0	Start of Frame
☐	Other Mark	0	Unknown types

Result: Found Trigger @ 32, #11

The following example shows a search of audio packets.



31150

Offset	L0	L1	L2	L3
-17	00	00	00	00
-16	00	00	00	00
-15	00	00	00	00
-14	00	00	00	00
-13	00	00	00	00
-12	00	00	00	00
-11	00	00	00	00
-10	00	00	00	00

#	Link Clock #	TimeStamp	Type
42	24015	0:0:0.000.029.648.148	BF
43	24016	0:0:0.000.029.649.383	BF
44	24017	0:0:0.000.029.650.617	BS
45	24018	0:0:0.000.029.651.852	BS Data
46	30014	0:0:0.000.037.054.321	BS
47	30015	0:0:0.000.037.055.556	BF
48	30016	0:0:0.000.037.056.790	BF
49	30017	0:0:0.000.037.058.025	BS
50	30018	0:0:0.000.037.059.259	BS Data
51	31149	0:0:0.000.038.455.556	SS
52	31150	0:0:0.000.038.456.790	Audio Stream
53	31162	0:0:0.000.038.471.605	SE
54	36014	0:0:0.000.044.461.728	BS
55	36015	0:0:0.000.044.462.963	BF
56	36016	0:0:0.000.044.464.198	BF
57	36017	0:0:0.000.044.465.432	BS
58	36018	0:0:0.000.044.466.667	BS Data
59	42014	0:0:0.000.051.869.136	BS
60	42015	0:0:0.000.051.870.370	BF
61	42016	0:0:0.000.051.871.605	BF

```
Audio Stream
Packet ID:   0
Coding:      0 (2-8 Ch LPCM, IEC 61937 <= 6.144Mb
Layout:      8 Channel Layout
Sample 0
 ch01=90ff828b ch02=a0ff828b ch03=90ff828b ch04=a
 ch05=90ff828b ch06=a0ff828b ch07=90000000 ch08=a
```

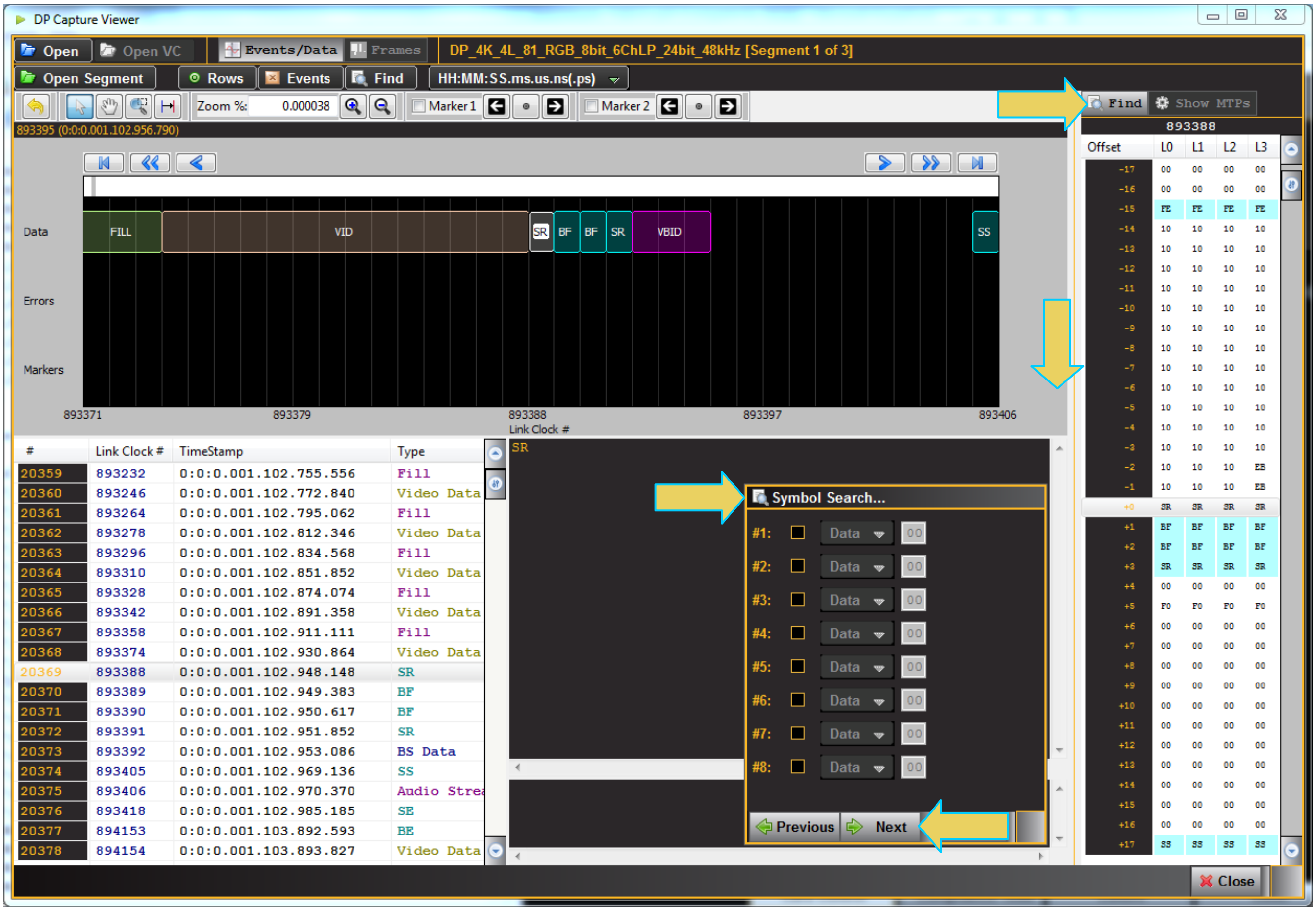
```
Lane 3: 05 d8 8b 82 ff a0 a9 00 00 00 a0 7d
Lane 2: 00 00 8b 82 ff 90 cc 00 00 00 90 18
Lane 1: 02 ce 8b 82 ff a0 a9 8b 82 ff a0 a9
Lane 0: 00 00 8b 82 ff 90 cc 8b 82 ff 90 cc
```

	Type	Count	Description
☑	Aud-TS	7	Audio TimeStamp
☑	Aud-S	5512	Audio Stream
☐	Ext	0	Extension
☐	Aud-CM	0	Audio Copy Management
☐	ISRC	0	ISRC
☐	VSC	0	VSC
☐	RSVD	0	CTA Reserved
☐	VSIF	0	CTA Vendor Specific
☐	AVI	0	CTA AVI
☐	SPD	0	CTA SPD
☑	Aud	7	CTA Audio
☐	MPEG	0	CTA MPEG
☐	VBI	0	CTA NTSC VBI
☐	HDR	0	CTA HDR
☐	Other Sec	0	Unknown types

```
Result:  Found Aud-S @ 31150, #52
```

12.12.3 Symbol Search

You can also initiate a symbol search on the **Raw Data** panel by clicking on the **Find** button near the top left of the panel. When you initiate a symbol search, the **Symbol Search** dialog box appears as shown below which indicates a search for Scrambler Reset.



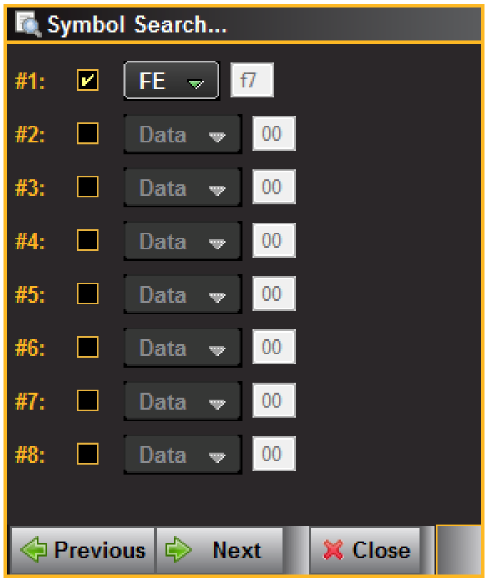
#	Link Clock #	TimeStamp	Type
20359	893232	0:0:0.001.102.755.556	Fill
20360	893246	0:0:0.001.102.772.840	Video Data
20361	893264	0:0:0.001.102.795.062	Fill
20362	893278	0:0:0.001.102.812.346	Video Data
20363	893296	0:0:0.001.102.834.568	Fill
20364	893310	0:0:0.001.102.851.852	Video Data
20365	893328	0:0:0.001.102.874.074	Fill
20366	893342	0:0:0.001.102.891.358	Video Data
20367	893358	0:0:0.001.102.911.111	Fill
20368	893374	0:0:0.001.102.930.864	Video Data
20369	893388	0:0:0.001.102.948.148	SR
20370	893389	0:0:0.001.102.949.383	BF
20371	893390	0:0:0.001.102.950.617	BF
20372	893391	0:0:0.001.102.951.852	SR
20373	893392	0:0:0.001.102.953.086	BS Data
20374	893405	0:0:0.001.102.969.136	SS
20375	893406	0:0:0.001.102.970.370	Audio Strea
20376	893418	0:0:0.001.102.985.185	SE
20377	894153	0:0:0.001.103.892.593	BE
20378	894154	0:0:0.001.103.893.827	Video Data

893388

Offset	L0	L1	L2	L3
-17	00	00	00	00
-16	00	00	00	00
-15	FE	FE	FE	FE
-14	10	10	10	10
-13	10	10	10	10
-12	10	10	10	10
-11	10	10	10	10
-10	10	10	10	10
-9	10	10	10	10
-8	10	10	10	10
-7	10	10	10	10
-6	10	10	10	10
-5	10	10	10	10
-4	10	10	10	10
-3	10	10	10	10
-2	10	10	10	EB
-1	10	10	10	EB
+0	SR	SR	SR	SR
+1	BF	BF	BF	BF
+2	BF	BF	BF	BF
+3	SR	SR	SR	SR
+4	00	00	00	00
+5	F0	F0	F0	F0
+6	00	00	00	00
+7	00	00	00	00
+8	00	00	00	00
+9	00	00	00	00
+10	00	00	00	00
+11	00	00	00	00
+12	00	00	00	00
+13	00	00	00	00
+14	00	00	00	00
+15	00	00	00	00
+16	00	00	00	00
+17	SS	SS	SS	SS

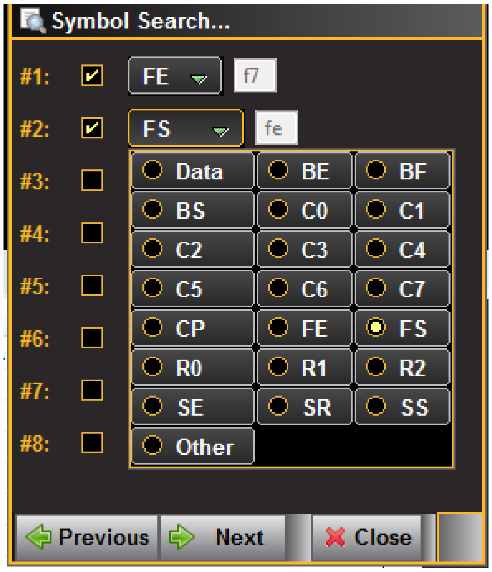
#1:	☐	Data	00
#2:	☐	Data	00
#3:	☐	Data	00
#4:	☐	Data	00
#5:	☐	Data	00
#6:	☐	Data	00
#7:	☐	Data	00
#8:	☐	Data	00

The Symbol Search dialog box is shown below.



#1:	☑	FE	f7
#2:	☐	Data	00
#3:	☐	Data	00
#4:	☐	Data	00
#5:	☐	Data	00
#6:	☐	Data	00
#7:	☐	Data	00
#8:	☐	Data	00

To search for a symbol, click on a checkbox and select the symbol type from the pop-up menu a shown below.



Symbol Search...

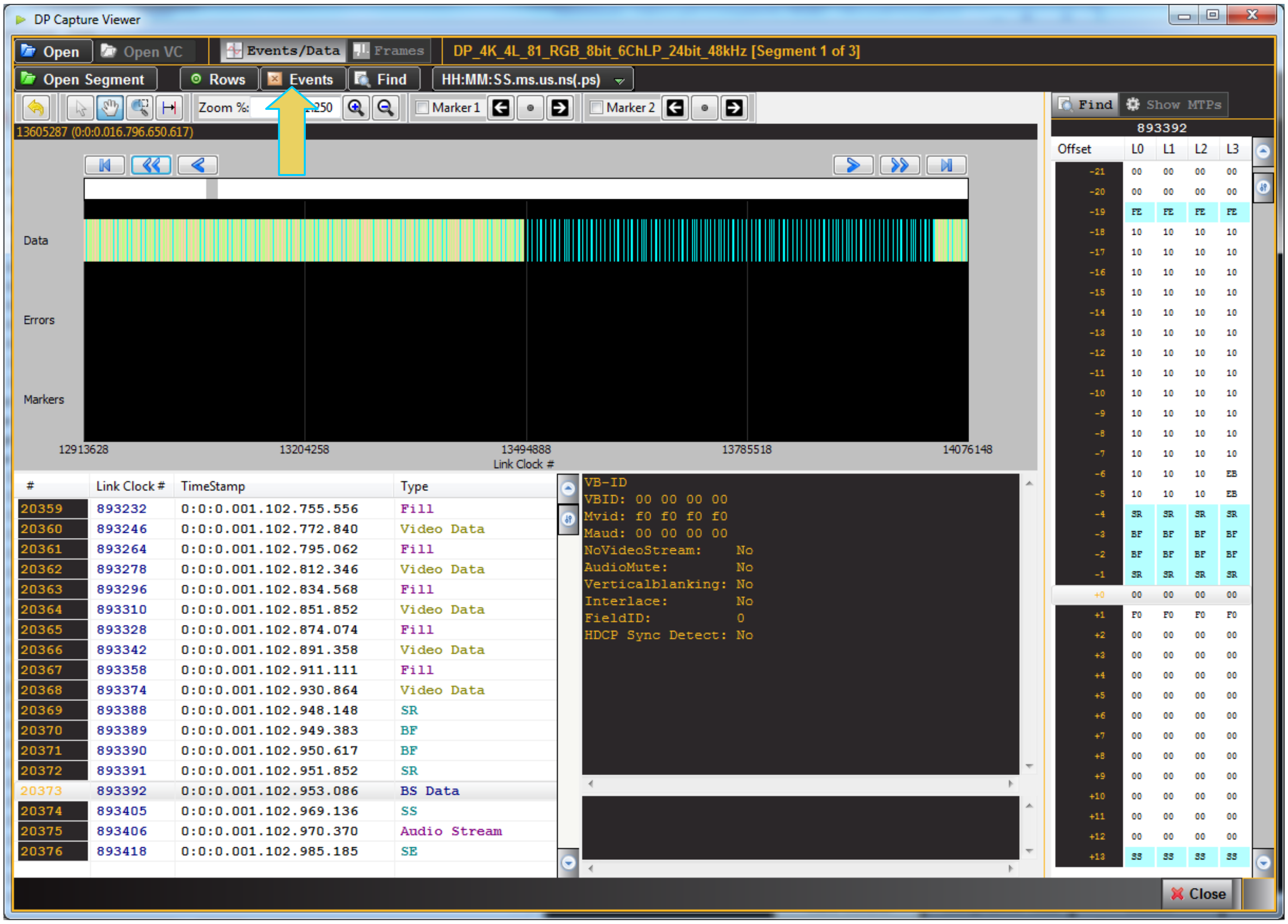
#1: ☑ FE f7
#2: ☑ FS fe
#3: ☐
#4: ☐
#5: ☐
#6: ☐
#7: ☐
#8: ☐

○ Data ○ BE ○ BF
○ BS ○ C0 ○ C1
○ C2 ○ C3 ○ C4
○ C5 ○ C6 ○ C7
○ CP ○ FE ● FS
○ R0 ○ R1 ○ R2
○ SE ○ SR ○ SS
○ Other

When you click **Next** the application will search for the symbols.

12.13 Filtering Specific Data Elements

You can filter the captured data to show only specific data types using the **Event Selection** feature. The **Event Selection** dialog box is accessible from the **Events** activation button Events on the top of the **DP Capture Viewer** window as shown below. The results of the filter apply to both the **Event Plot** and the **Event Data** panels.



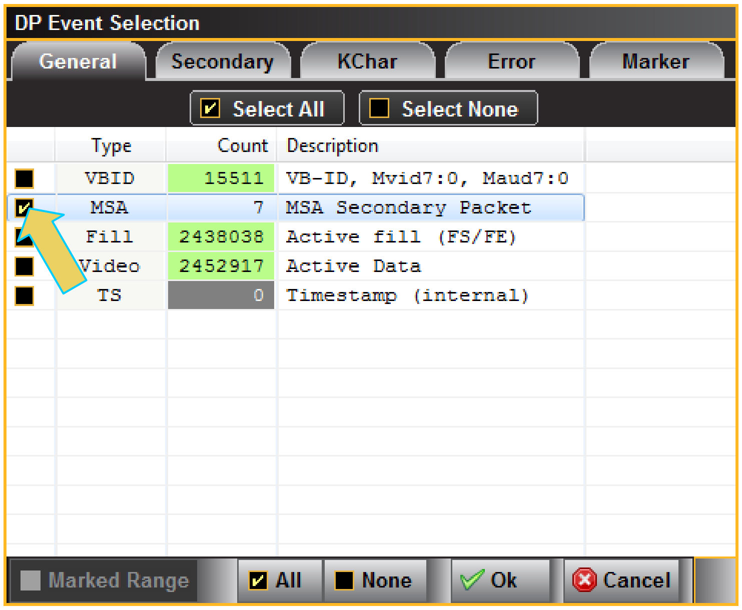
#	Link Clock #	TimeStamp	Type
20359	893232	0:0:0.001.102.755.556	Fill
20360	893246	0:0:0.001.102.772.840	Video Data
20361	893264	0:0:0.001.102.795.062	Fill
20362	893278	0:0:0.001.102.812.346	Video Data
20363	893296	0:0:0.001.102.834.568	Fill
20364	893310	0:0:0.001.102.851.852	Video Data
20365	893328	0:0:0.001.102.874.074	Fill
20366	893342	0:0:0.001.102.891.358	Video Data
20367	893358	0:0:0.001.102.911.111	Fill
20368	893374	0:0:0.001.102.930.864	Video Data
20369	893388	0:0:0.001.102.948.148	SR
20370	893389	0:0:0.001.102.949.383	BF
20371	893390	0:0:0.001.102.950.617	BF
20372	893391	0:0:0.001.102.951.852	SR
20373	893392	0:0:0.001.102.953.086	BS Data
20374	893405	0:0:0.001.102.969.136	SS
20375	893406	0:0:0.001.102.970.370	Audio Stream
20376	893418	0:0:0.001.102.985.185	SE

```
VB-ID
VBID: 00 00 00 00
Mvid: f0 f0 f0 f0
Maud: 00 00 00 00
NoVideoStream:    No
AudioMute:        No
Verticalblanking: No
Interlace:        No
FieldID:          0
HDCP Sync Detect: No
```

893392

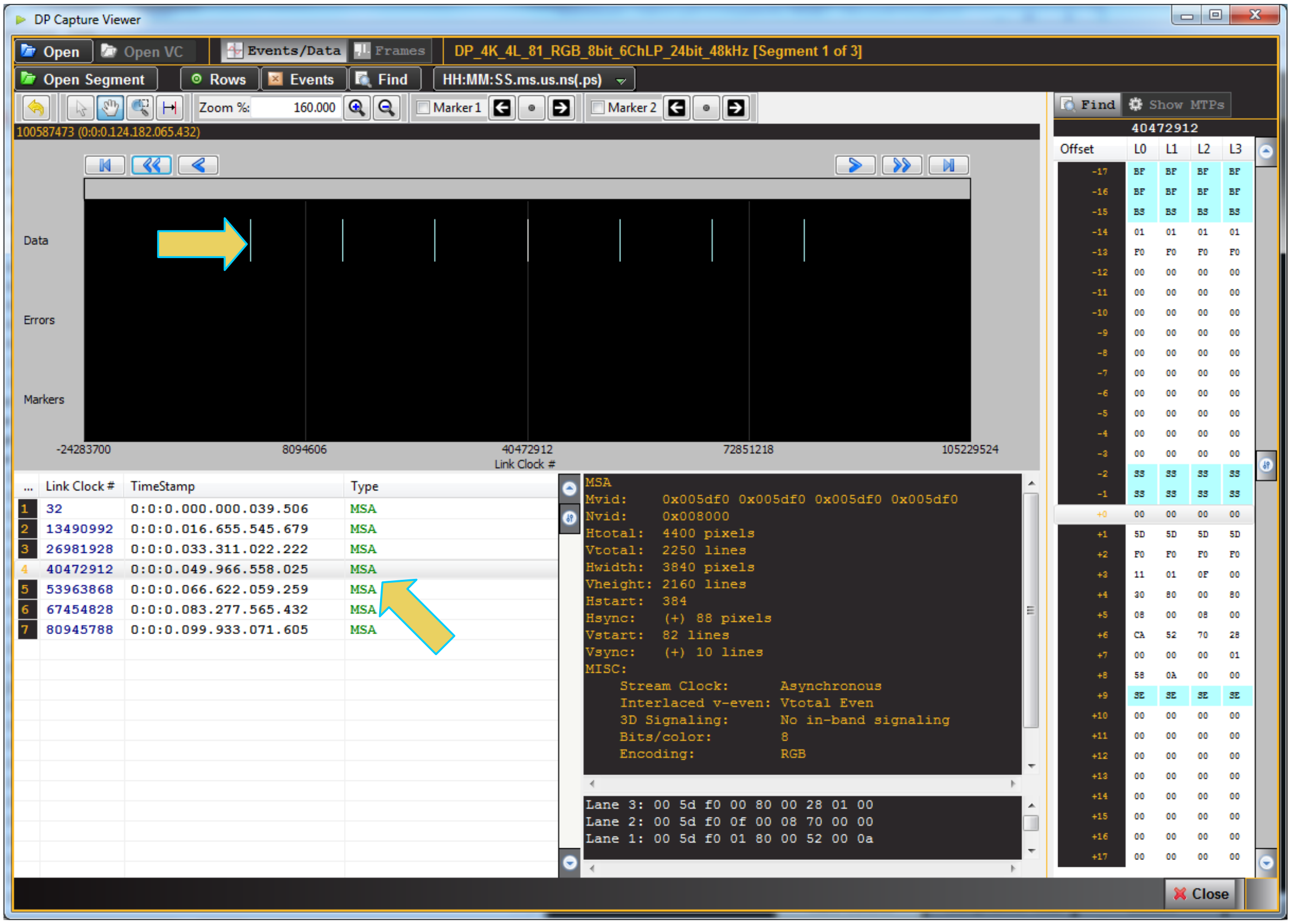
Offset	L0	L1	L2	L3
-21	00	00	00	00
-20	00	00	00	00
-19	FE	FE	FE	FE
-18	10	10	10	10
-17	10	10	10	10
-16	10	10	10	10
-15	10	10	10	10
-14	10	10	10	10
-13	10	10	10	10
-12	10	10	10	10
-11	10	10	10	10
-10	10	10	10	10
-9	10	10	10	10
-8	10	10	10	10
-7	10	10	10	10
-6	10	10	10	EB
-5	10	10	10	EB
-4	SR	SR	SR	SR
-3	BF	BF	BF	BF
-2	BF	BF	BF	BF
-1	SR	SR	SR	SR
+0	00	00	00	00
+1	F0	F0	F0	F0
+2	00	00	00	00
+3	00	00	00	00
+4	00	00	00	00
+5	00	00	00	00
+6	00	00	00	00
+7	00	00	00	00
+8	00	00	00	00
+9	00	00	00	00
+10	00	00	00	00
+11	00	00	00	00
+12	00	00	00	00
+13	SS	SS	SS	SS

The following screens show some examples of filtering scenarios.



	Type	Count	Description
■	VBID	15511	VB-ID, Mvid7:0, Maud7:0
☑	MSA	7	MSA Secondary Packet
■	Fill	2438038	Active fill (FS/FE)
■	Video	2452917	Active Data
■	TS	0	Timestamp (internal)

The results of the search of the MSA data elements on the **Event Table** are shown below.



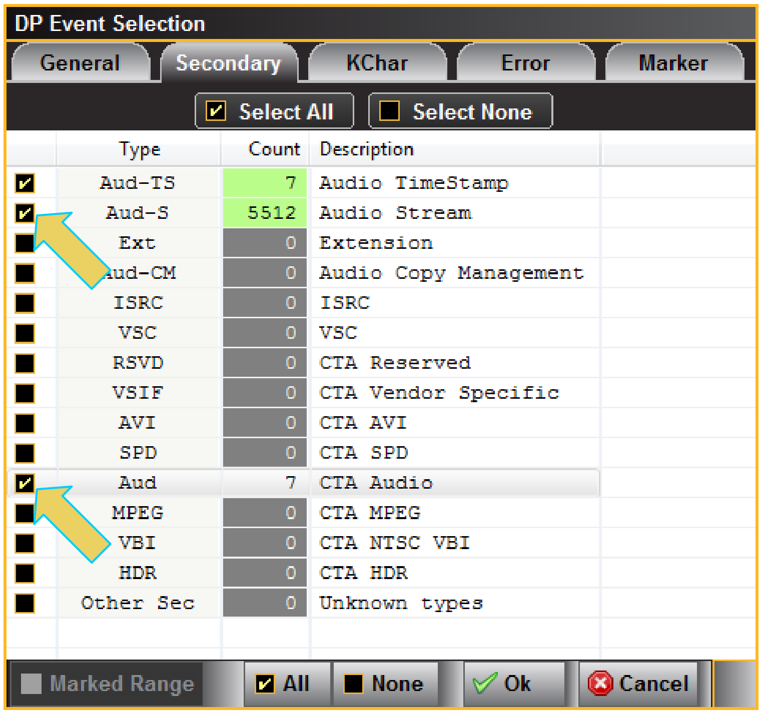
...	Link Clock #	TimeStamp	Type
1	32	0:0:0.000.000.039.506	MSA
2	13490992	0:0:0.016.655.545.679	MSA
3	26981928	0:0:0.033.311.022.222	MSA
4	40472912	0:0:0.049.966.558.025	MSA
5	53963868	0:0:0.066.622.059.259	MSA
6	67454828	0:0:0.083.277.565.432	MSA
7	80945788	0:0:0.099.933.071.605	MSA

```
MSA
Mvid:    0x005df0 0x005df0 0x005df0 0x005df0
Nvid:    0x008000
Htotal:  4400 pixels
Vtotal:  2250 lines
Hwidth:  3840 pixels
Vheight: 2160 lines
Hstart:  384
Hsync:   (+) 88 pixels
Vstart:  82 lines
Vsync:   (+) 10 lines
MISC:
    Stream Clock:       Asynchronous
    Interlaced v-even: Vtotal Even
    3D Signaling:       No in-band signaling
    Bits/color:         8
    Encoding:           RGB
```

```
Lane 3: 00 5d f0 00 80 00 28 01 00
Lane 2: 00 5d f0 0f 00 08 70 00 00
Lane 1: 00 5d f0 01 80 00 52 00 0a
```

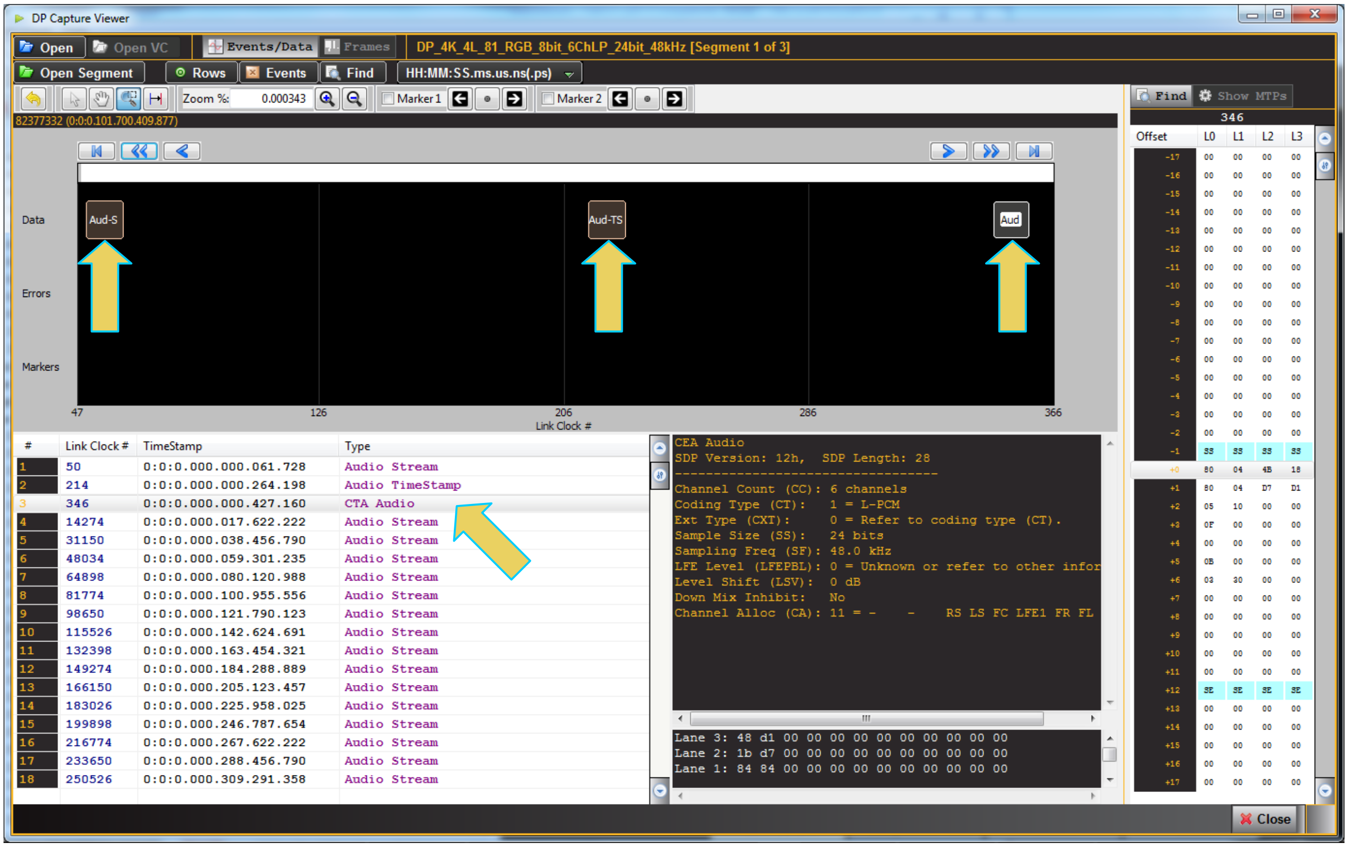
Offset	L0	L1	L2	L3
-17	BF	BF	BF	BF
-16	BF	BF	BF	BF
-15	BS	BS	BS	BS
-14	01	01	01	01
-13	F0	F0	F0	F0
-12	00	00	00	00
-11	00	00	00	00
-10	00	00	00	00
-9	00	00	00	00
-8	00	00	00	00
-7	00	00	00	00
-6	00	00	00	00
-5	00	00	00	00
-4	00	00	00	00
-3	00	00	00	00
-2	SS	SS	SS	SS
-1	SS	SS	SS	SS
+0	00	00	00	00
+1	5D	5D	5D	5D
+2	F0	F0	F0	F0
+3	11	01	0F	00
+4	30	80	00	80
+5	08	00	08	00
+6	CA	52	70	28
+7	00	00	00	01
+8	58	0A	00	00
+9	SE	SE	SE	SE
+10	00	00	00	00
+11	00	00	00	00
+12	00	00	00	00
+13	00	00	00	00
+14	00	00	00	00
+15	00	00	00	00
+16	00	00	00	00
+17	00	00	00	00

The following screen shows a second example with a successful search for audio data elements.



	Type	Count	Description
☑	Aud-TS	7	Audio TimeStamp
☑	Aud-S	5512	Audio Stream
☐	Ext	0	Extension
☐	Aud-CM	0	Audio Copy Management
☐	ISRC	0	ISRC
☐	VSC	0	VSC
☐	RSVD	0	CTA Reserved
☐	VSIF	0	CTA Vendor Specific
☐	AVI	0	CTA AVI
☐	SPD	0	CTA SPD
☑	Aud	7	CTA Audio
☐	MPEG	0	CTA MPEG
☐	VBI	0	CTA NTSC VBI
☐	HDR	0	CTA HDR
☐	Other Sec	0	Unknown types

The following screen example shows the results of the above search.

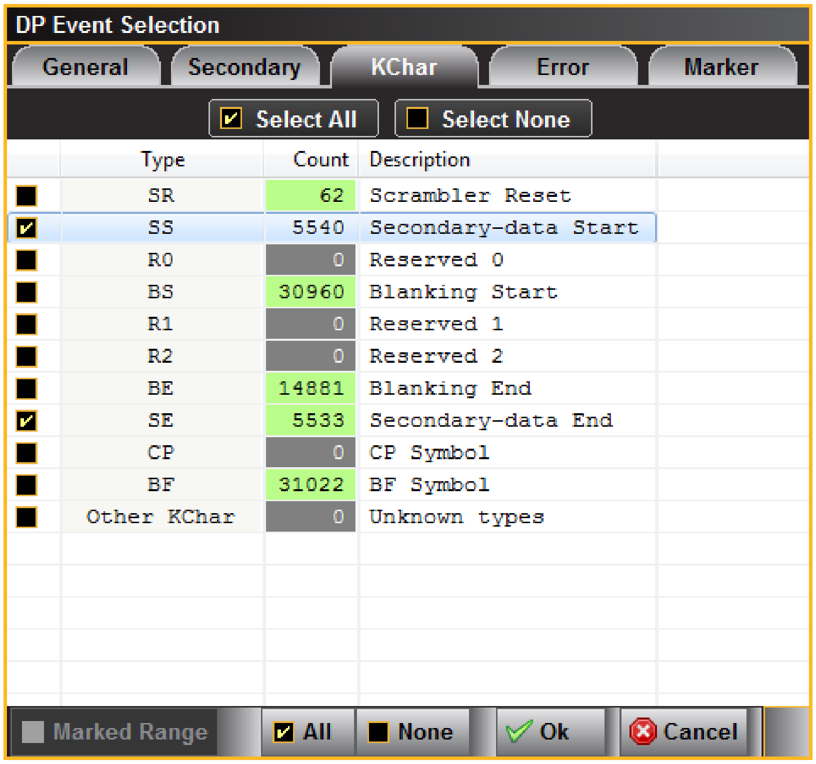


#	Link Clock #	TimeStamp	Type
1	50	0:0:0.000.000.061.728	Audio Stream
2	214	0:0:0.000.000.264.198	Audio TimeStamp
3	346	0:0:0.000.000.427.160	CTA Audio
4	14274	0:0:0.000.017.622.222	Audio Stream
5	31150	0:0:0.000.038.456.790	Audio Stream
6	48034	0:0:0.000.059.301.235	Audio Stream
7	64898	0:0:0.000.080.120.988	Audio Stream
8	81774	0:0:0.000.100.955.556	Audio Stream
9	98650	0:0:0.000.121.790.123	Audio Stream
10	115526	0:0:0.000.142.624.691	Audio Stream
11	132398	0:0:0.000.163.454.321	Audio Stream
12	149274	0:0:0.000.184.288.889	Audio Stream
13	166150	0:0:0.000.205.123.457	Audio Stream
14	183026	0:0:0.000.225.958.025	Audio Stream
15	199898	0:0:0.000.246.787.654	Audio Stream
16	216774	0:0:0.000.267.622.222	Audio Stream
17	233650	0:0:0.000.288.456.790	Audio Stream
18	250526	0:0:0.000.309.291.358	Audio Stream

```
CEA Audio
SDP Version: 12h,  SDP Length: 28
----------------------------------
Channel Count (CC): 6 channels
Coding Type (CT):   1 = L-PCM
Ext Type (CXT):     0 = Refer to coding type (CT).
Sample Size (SS):   24 bits
Sampling Freq (SF): 48.0 kHz
LFE Level (LFEPBL): 0 = Unknown or refer to other infor
Level Shift (LSV):  0 dB
Down Mix Inhibit:   No
Channel Alloc (CA): 11 = -    -    RS LS FC LFE1 FR FL
```

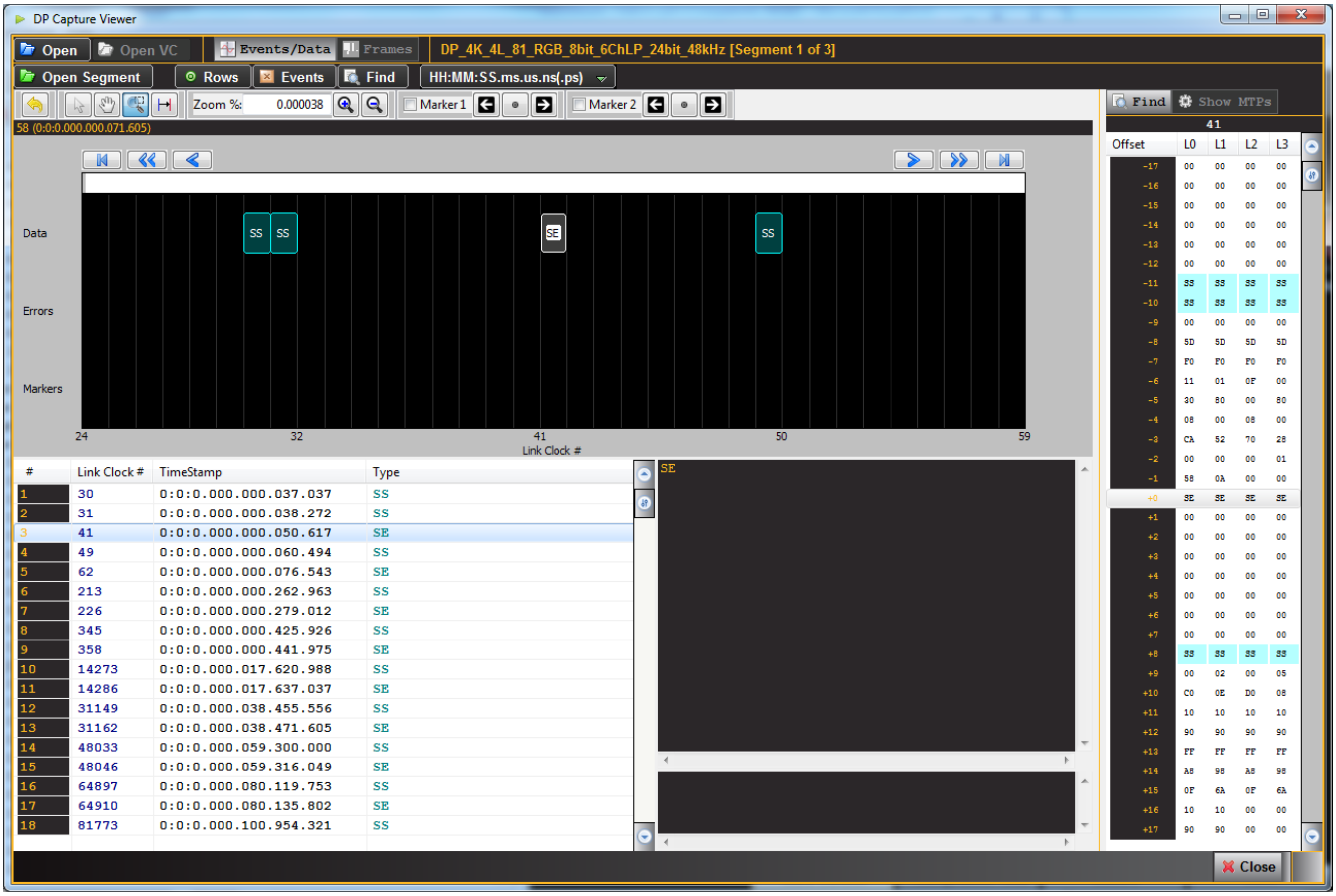
```
Lane 3: 48 d1 00 00 00 00 00 00 00 00 00 00
Lane 2: 1b d7 00 00 00 00 00 00 00 00 00 00
Lane 1: 84 84 00 00 00 00 00 00 00 00 00 00
```

In the next example below, the **K Character** tab is active and all the K Characters are selected in the search.



	Type	Count	Description
☐	SR	62	Scrambler Reset
☑	SS	5540	Secondary-data Start
☐	R0	0	Reserved 0
☐	BS	30960	Blanking Start
☐	R1	0	Reserved 1
☐	R2	0	Reserved 2
☐	BE	14881	Blanking End
☑	SE	5533	Secondary-data End
☐	CP	0	CP Symbol
☐	BF	31022	BF Symbol
☐	Other KChar	0	Unknown types

The results of the above search criteria are shown below.

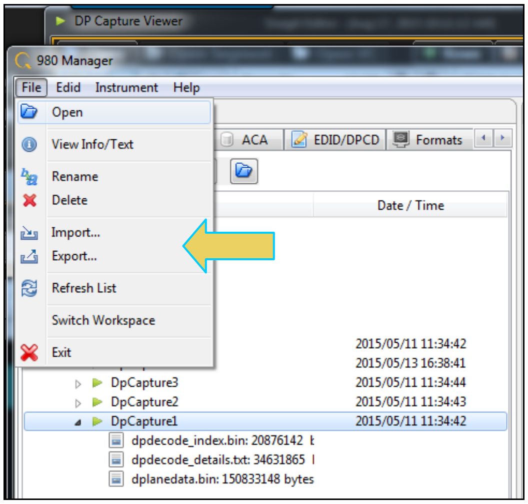


#	Link Clock #	TimeStamp	Type
1	30	0:0:0.000.000.037.037	SS
2	31	0:0:0.000.000.038.272	SS
3	41	0:0:0.000.000.050.617	SE
4	49	0:0:0.000.000.060.494	SS
5	62	0:0:0.000.000.076.543	SE
6	213	0:0:0.000.000.262.963	SS
7	226	0:0:0.000.000.279.012	SE
8	345	0:0:0.000.000.425.926	SS
9	358	0:0:0.000.000.441.975	SE
10	14273	0:0:0.000.017.620.988	SS
11	14286	0:0:0.000.017.637.037	SE
12	31149	0:0:0.000.038.455.556	SS
13	31162	0:0:0.000.038.471.605	SE
14	48033	0:0:0.000.059.300.000	SS
15	48046	0:0:0.000.059.316.049	SE
16	64897	0:0:0.000.080.119.753	SS
17	64910	0:0:0.000.080.135.802	SE
18	81773	0:0:0.000.100.954.321	SS

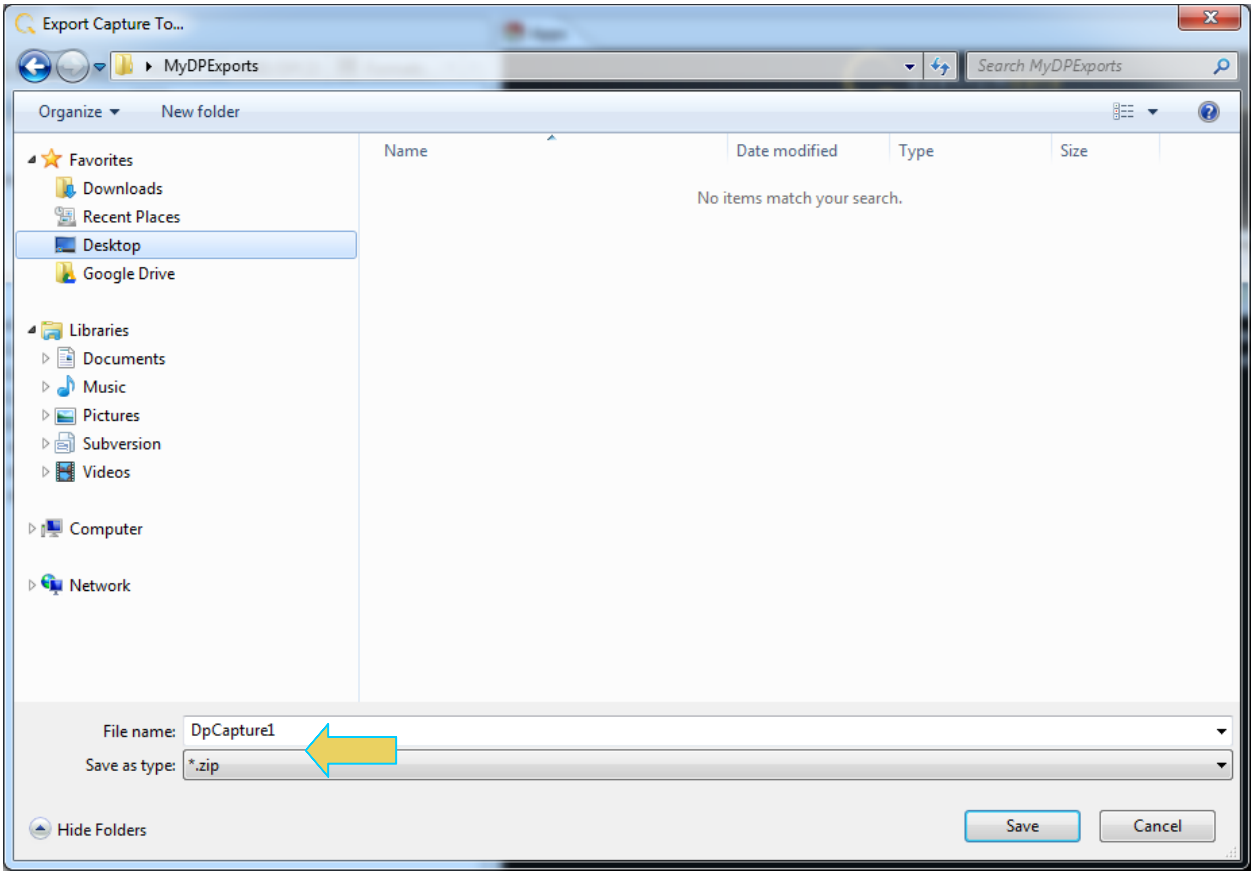
Offset	L0	L1	L2	L3
-17	00	00	00	00
-16	00	00	00	00
-15	00	00	00	00
-14	00	00	00	00
-13	00	00	00	00
-12	00	00	00	00
-11	SS	SS	SS	SS
-10	SS	SS	SS	SS
-9	00	00	00	00
-8	5D	5D	5D	5D
-7	F0	F0	F0	F0
-6	11	01	0F	00
-5	30	80	00	80
-4	08	00	08	00
-3	CA	52	70	28
-2	00	00	00	01
-1	58	0A	00	00
+0	SE	SE	SE	SE
+1	00	00	00	00
+2	00	00	00	00
+3	00	00	00	00
+4	00	00	00	00
+5	00	00	00	00
+6	00	00	00	00
+7	00	00	00	00
+8	SS	SS	SS	SS
+9	00	02	00	05
+10	C0	0E	D0	08
+11	10	10	10	10
+12	90	90	90	90
+13	FF	FF	FF	FF
+14	A8	98	A8	98
+15	0F	6A	0F	6A
+16	10	10	00	00
+17	90	90	00	00

12.14 Importing and Exporting Capture files

The **Import** and **Export** options on the right-click menu and the **File** pull-down menu allow you to exchange capture files between your PC and the 980 GUI Manager application. You Export a capture file to disseminate to colleagues or other subject matter experts. You import a file when you want to examine a capture file taken by a colleague. The **Export** and **Import** function zips or unzips a capture file to enable you to post it on an FTP server of disseminate through email of the file is not too large.



When you select **Export**, a Windows Explorer window will show up enabling you to save the capture as a zip file in a directory and name of your choosing. Refer to the screen examples below.



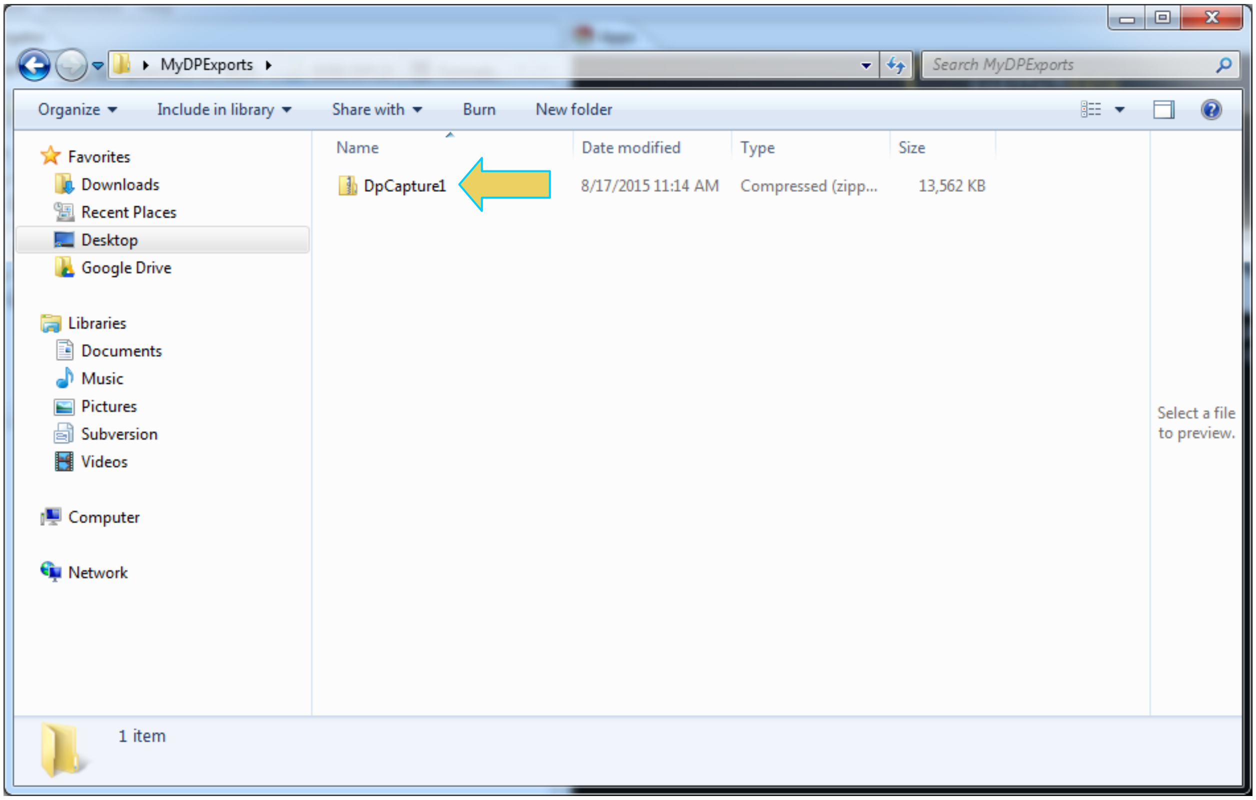
Export Capture To...

MyDPExports

No items match your search.

File name: DpCapture1

Save as type: *.zip



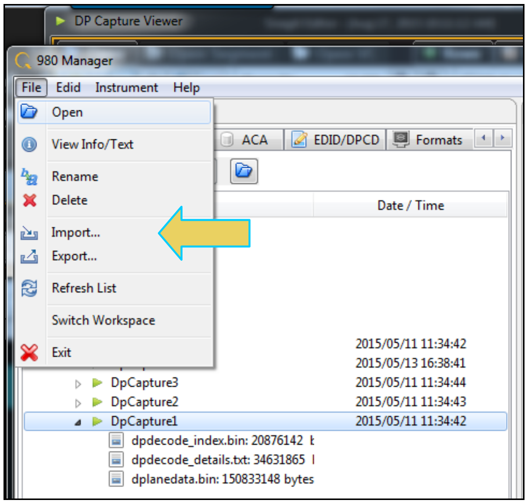
MyDPExports

Name	Date modified	Type	Size
DpCapture1	8/17/2015 11:14 AM	Compressed (zipp...	13,562 KB

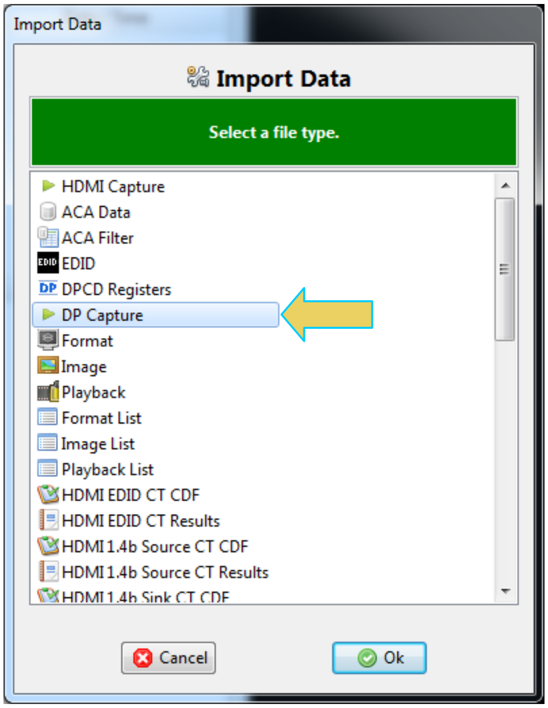
Select a file to preview.

1 item

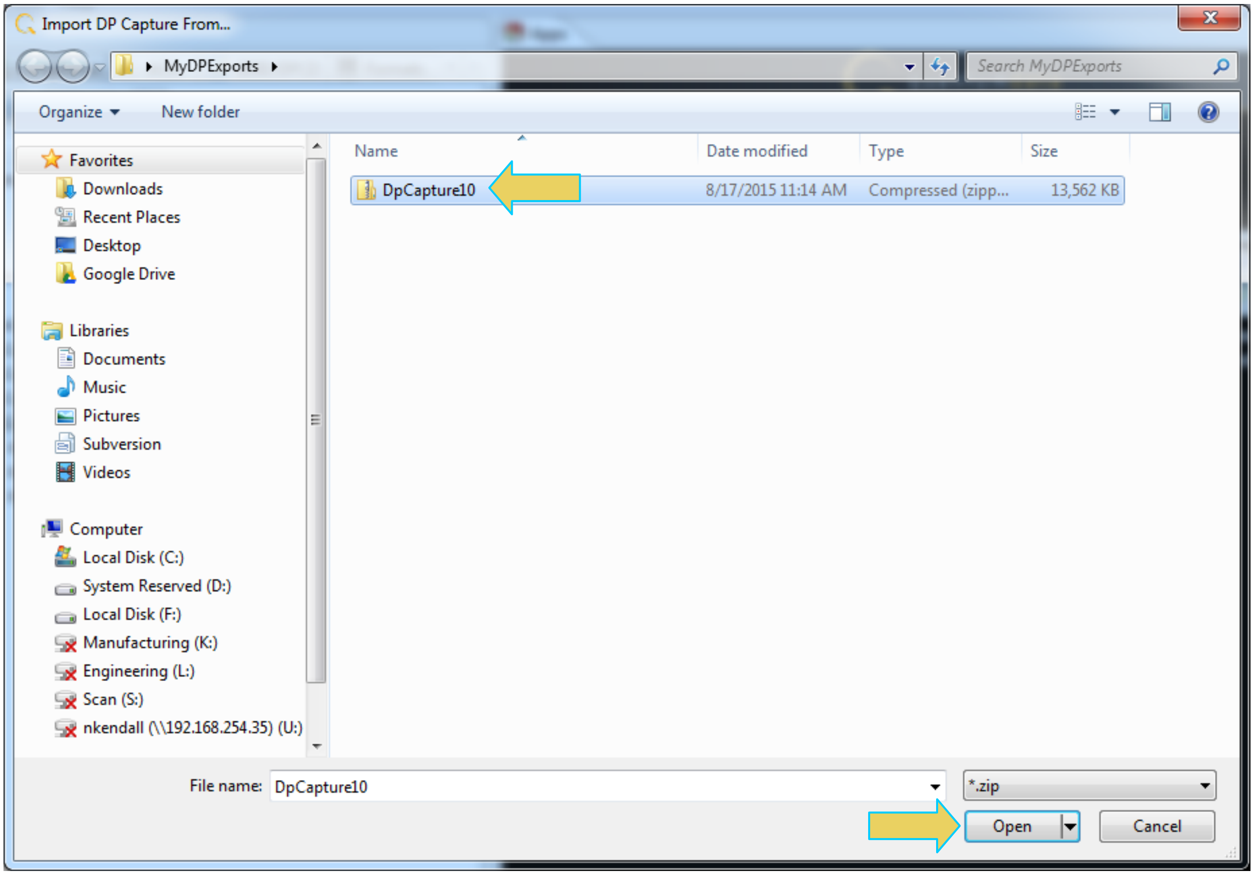
When you want to import a file, use the **File** pull-down menu and select **Import** as shown below.



The **Import Data** dialog box will appear as shown below. Select **DPCapture** and click **OK**.



A Windows Explorer window will appear enabling you to navigate to the directory where you have stored your zipped capture file. Select the file and click **Open** as shown below.

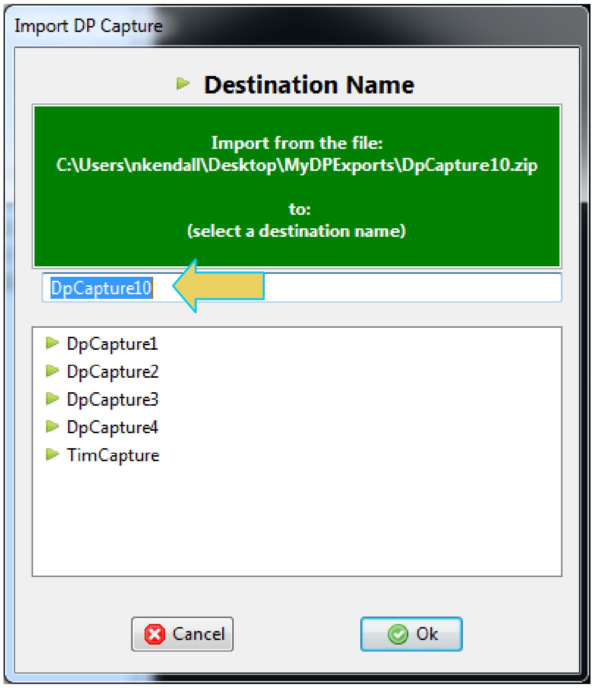


Name	Date modified	Type	Size
DpCapture10	8/17/2015 11:14 AM	Compressed (zipp...	13,562 KB

File name: DpCapture10

*.zip

You will then be given an opportunity to rename the file with the **Import DP Capture** dialog box as shown below.

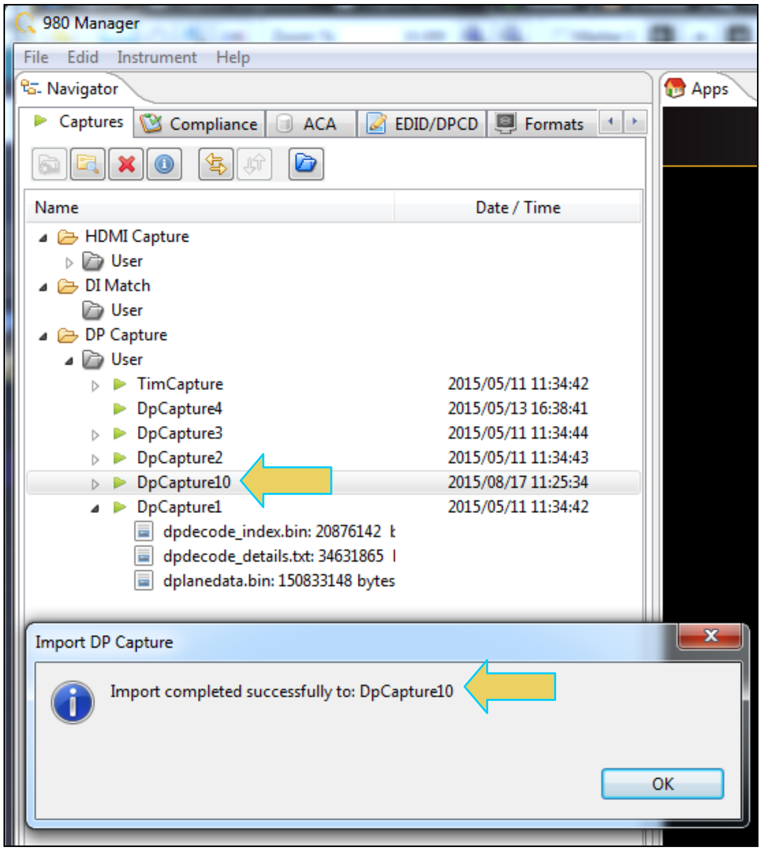


Import from the file:
C:\Users\nkendall\Desktop\MyDPExports\DpCapture10.zip

to:
(select a destination name)

DpCapture10

Click **Ok** and the import will begin. You will see a confirmation dialog box and you will see the new capture in the list of captures in the **Navigator** panel as shown below.



Import completed successfully to: DpCapture10

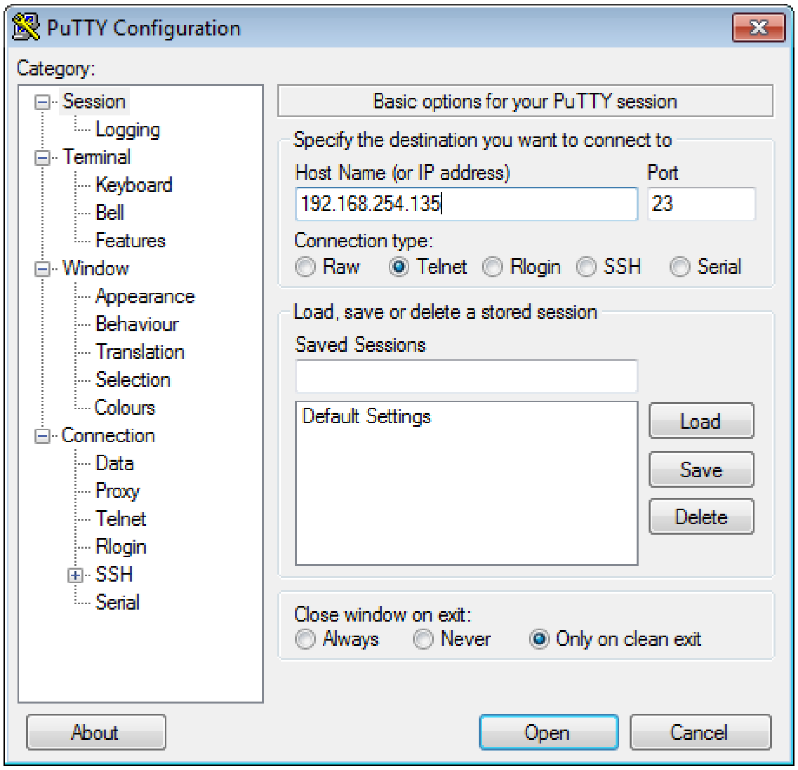
14 Command Reference

This section provides a list of commands available for use with the 980 HDMI Video Generator module. You can control the 980 and its modules through the command line via a telnet session or from the 980 Manager Console panel. Typically users will utilize a terminal program such as PuTTY.

15.1 Accessing the Command Line

To establish a command line session through a telnet session:

1. Launch the Command Prompt utility from the Windows Accessories such as PuTTY. Enter



Host Name (or IP address): 192.168.254.135

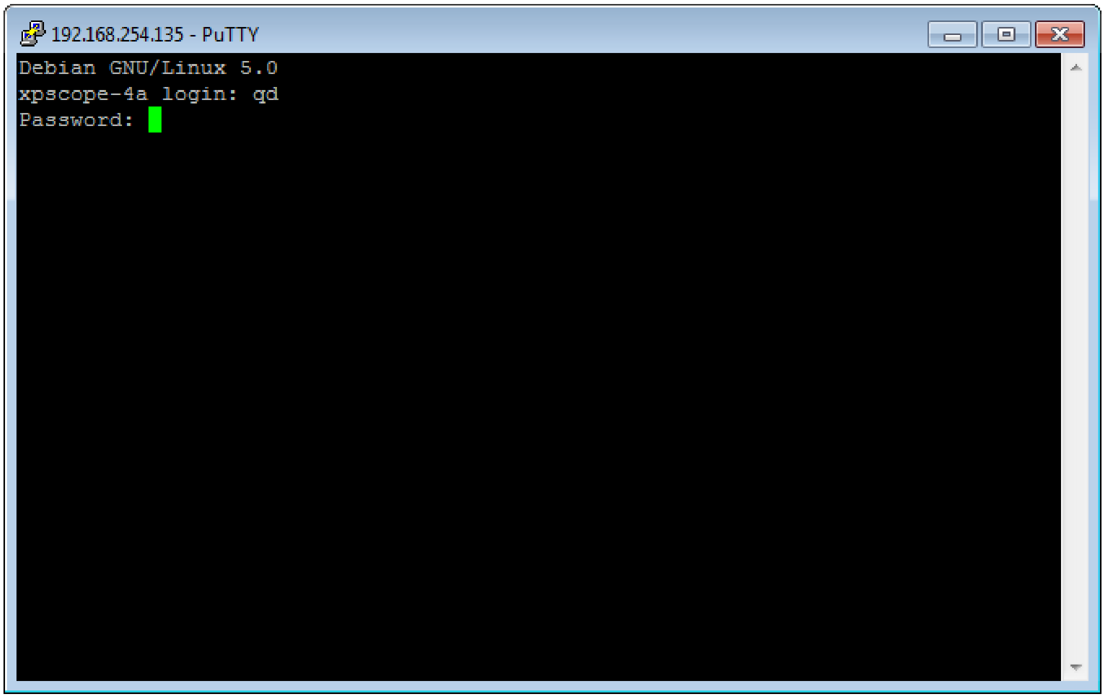
Port: 23

Connection type: ○ Raw ● Telnet ○ Rlogin ○ SSH ○ Serial

Close window on exit: ○ Always ○ Never ● Only on clean exit

2. Establish a telnet session with the 980 using the following command. Note you will enter in the IP address of the 980 (192.168.254.135 in example)

   The 980 login prompt will then appear as shown below.



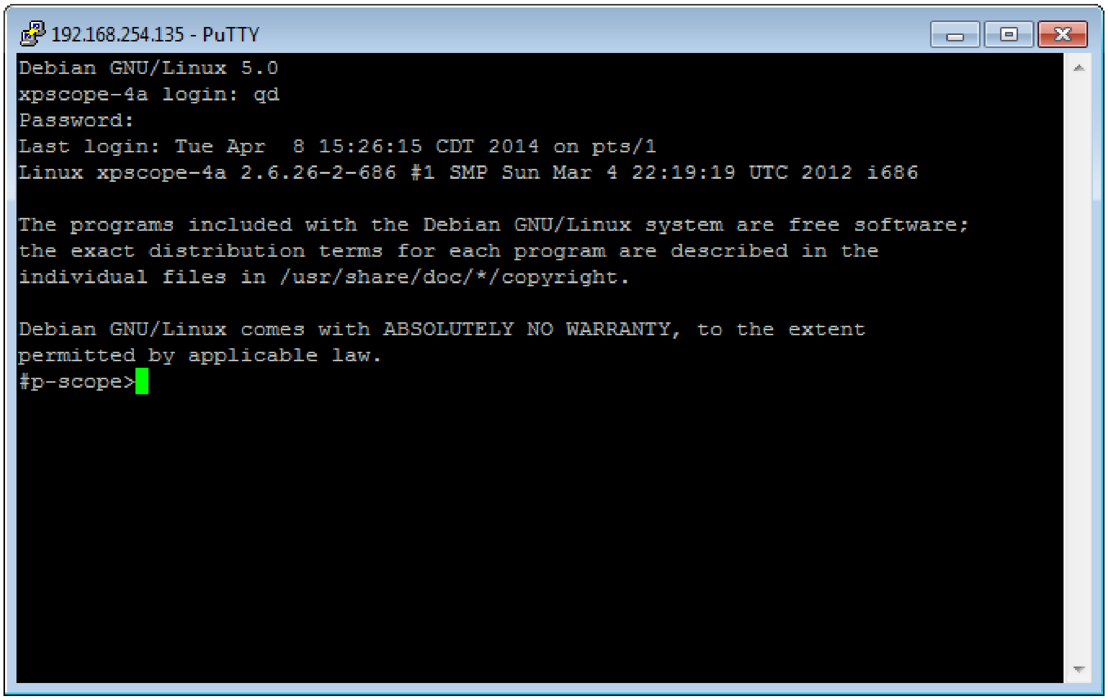
```
Debian GNU/Linux 5.0
xpscope-4a login: qd
Password:
```

3. Login at the prompt.

   Pscope login: `qd`

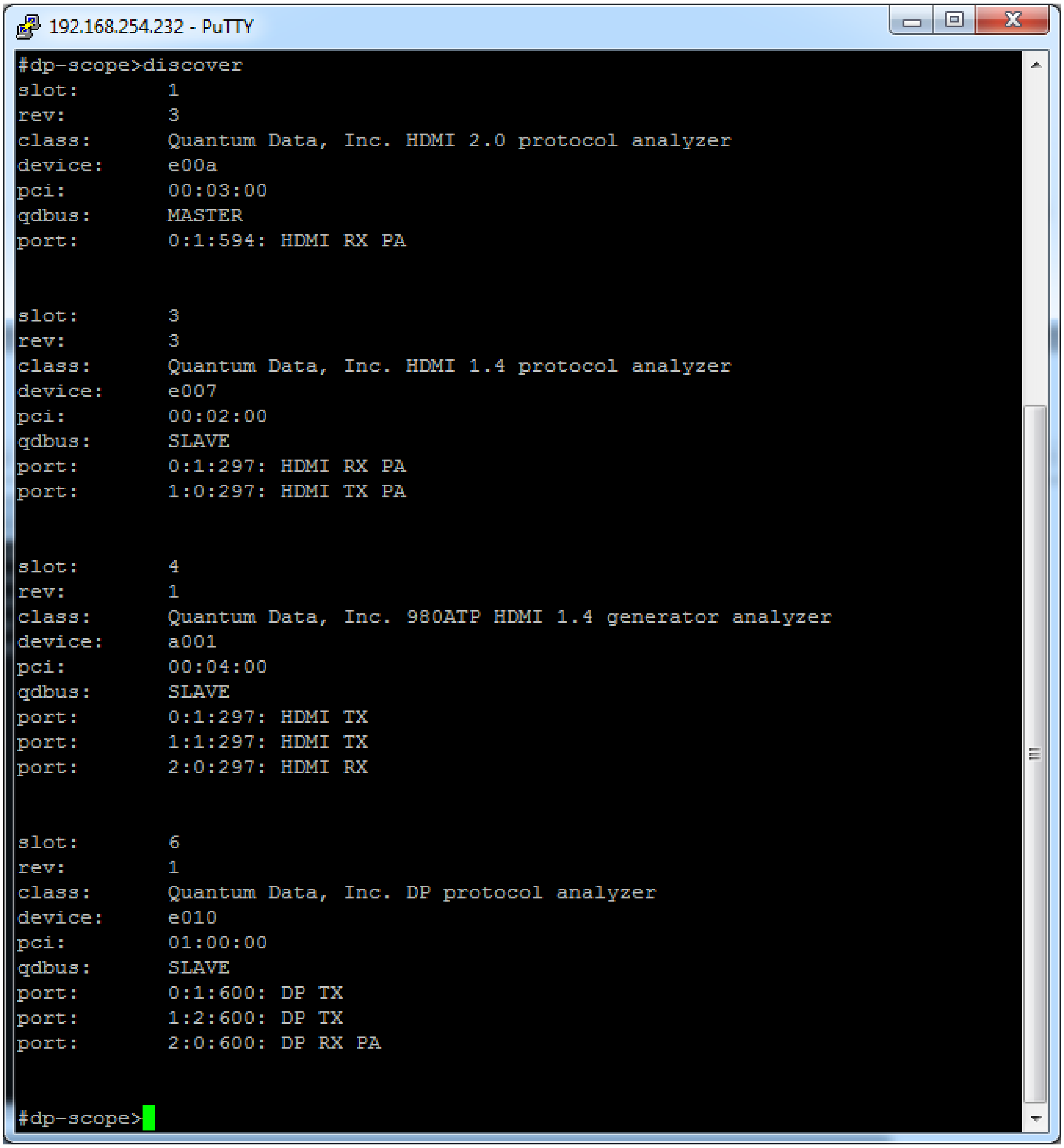
   Password: `qd // you will not be able to see the entry.`

4. The **`p-scope>`** prompt will appear allowing you to enter commands. Refer to the screen example below.



```
Debian GNU/Linux 5.0
xpscope-4a login: qd
Password:
Last login: Tue Apr  8 15:26:15 CDT 2014 on pts/1
Linux xpscope-4a 2.6.26-2-686 #1 SMP Sun Mar 4 22:19:19 UTC 2012 i686

The programs included with the Debian GNU/Linux system are free software;
the exact distribution terms for each program are described in the
individual files in /usr/share/doc/*/copyright.

Debian GNU/Linux comes with ABSOLUTELY NO WARRANTY, to the extent
permitted by applicable law.
#p-scope>
```

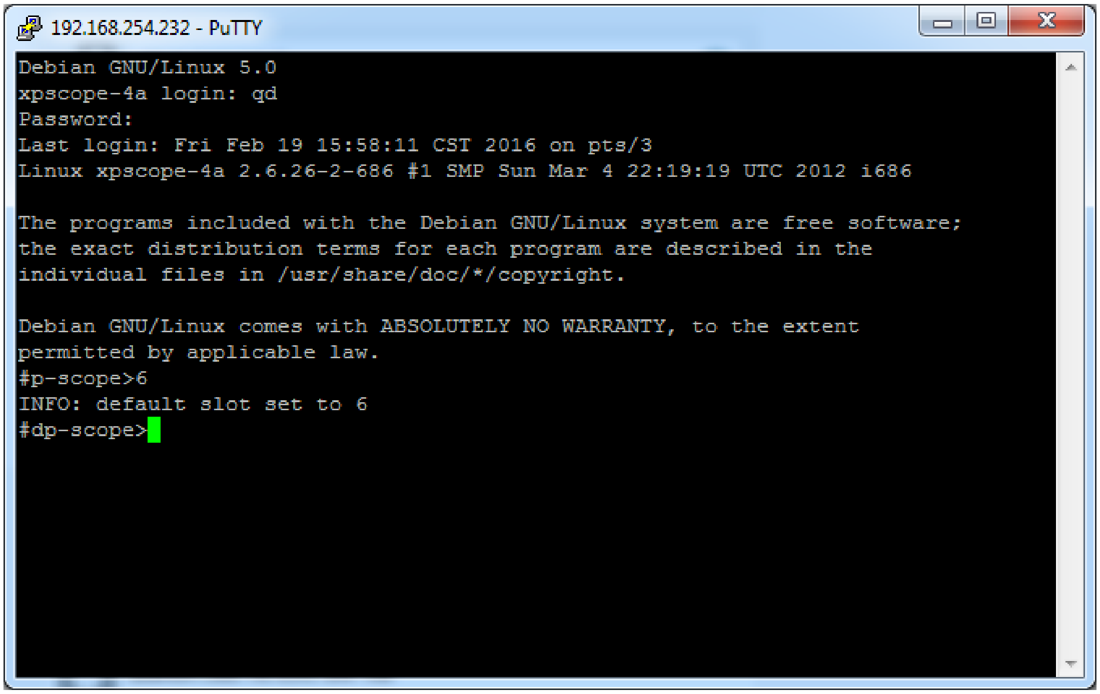
5. Determine the slot number using the `discover` command:



```
#dp-scope>discover
slot:       1
rev:        3
class:      Quantum Data, Inc. HDMI 2.0 protocol analyzer
device:     e00a
pci:        00:03:00
qdbus:      MASTER
port:       0:1:594: HDMI RX PA


slot:       3
rev:        3
class:      Quantum Data, Inc. HDMI 1.4 protocol analyzer
device:     e007
pci:        00:02:00
qdbus:      SLAVE
port:       0:1:297: HDMI RX PA
port:       1:0:297: HDMI TX PA


slot:       4
rev:        1
class:      Quantum Data, Inc. 980ATP HDMI 1.4 generator analyzer
device:     a001
pci:        00:04:00
qdbus:      SLAVE
port:       0:1:297: HDMI TX
port:       1:1:297: HDMI TX
port:       2:0:297: HDMI RX


slot:       6
rev:        1
class:      Quantum Data, Inc. DP protocol analyzer
device:     e010
pci:        01:00:00
qdbus:      SLAVE
port:       0:1:600: DP TX
port:       1:2:600: DP TX
port:       2:0:600: DP RX PA


#dp-scope>
```

In this example the DP module is in slot 6.

6. Access the DP Video Generator / Analyzer prompt by entering the 980 slot number that the DP Video Generator / Analyzer module is installed in. In this example it is Slot 6. Refer to the following screen.



```
Debian GNU/Linux 5.0
xpscope-4a login: qd
Password:
Last login: Fri Feb 19 15:58:11 CST 2016 on pts/3
Linux xpscope-4a 2.6.26-2-686 #1 SMP Sun Mar 4 22:19:19 UTC 2012 i686

The programs included with the Debian GNU/Linux system are free software;
the exact distribution terms for each program are described in the
individual files in /usr/share/doc/*/copyright.

Debian GNU/Linux comes with ABSOLUTELY NO WARRANTY, to the extent
permitted by applicable law.
#p-scope>6
INFO: default slot set to 6
#dp-scope>
```

The dp-scope>asss prompt is presented as shown above. Note that Slot 6 become the “default” slot and does not need to be entered on the command line; it is optional.

15.2 Command Line Conventions

Since the 980 can be equipped with multiple modules, there is a convention for addressing commands to specific modules.

The addressing convention is as follows:

```
<IN/OUT><Slot><Port>: command_string
```

The configuration used in this example is a 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module in Slot 6.

Example: Load a test pattern for the transmitter port (Tx1 port 0) on the 980 DP 1.4 USB-C/eDP Video Generator / Analyzer module which is equipped in Slot 6:

```
OUT60:IMGL SMPTEBar
```

If you are using the second Tx port (Tx2):

```
OUT61:IMGL SMPTEBar
```

If the Rx port is active the Tx1 port will not be available and you will receive an error (below). In this case you will have to use Tx2.

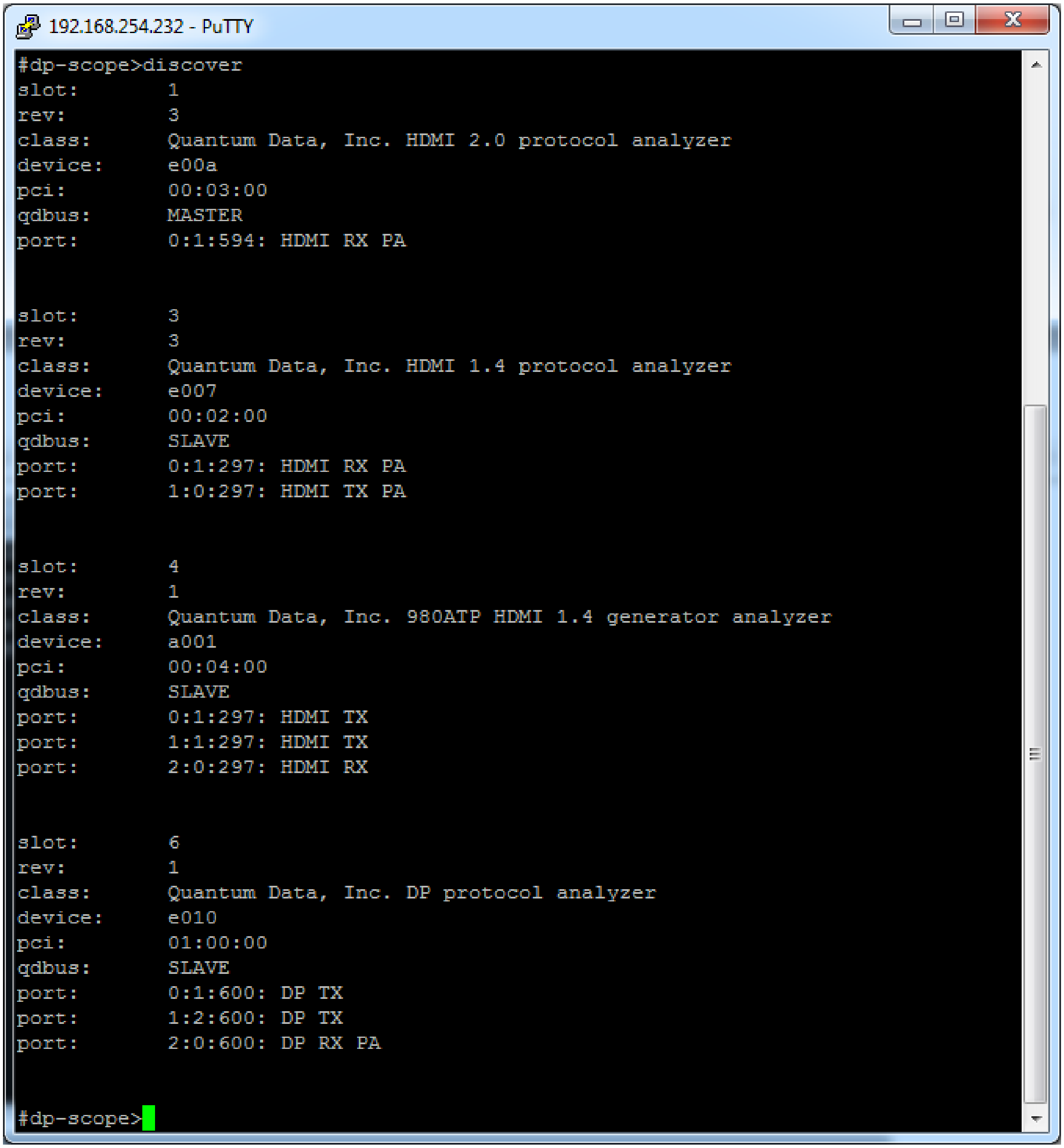
```
#dp-scope>out60:fmtu?
ERROR: Invalid Command: ¥out60:fmtu?
rxhprime: DP HDCP2 set hprime in rxstatus
rxlnkfail: DP HDCP2 set link integrity failure in rxstatus
rxpair: DP HDCP2 set pair in rxstatus
```

Note 2: Commands are not case sensitive.

Note 3: If the slot number has been established as the default (by entering the slot number on the command line) then you can leave the slot out of the command:

```
OUT0:IMGL SMPTEBar
```

To determine what modules are installed in what slots enter the discover command as shown:



```
#dp-scope>discover
slot:       1
rev:        3
class:      Quantum Data, Inc. HDMI 2.0 protocol analyzer
device:     e00a
pci:        00:03:00
qdbus:      MASTER
port:       0:1:594: HDMI RX PA


slot:       3
rev:        3
class:      Quantum Data, Inc. HDMI 1.4 protocol analyzer
device:     e007
pci:        00:02:00
qdbus:      SLAVE
port:       0:1:297: HDMI RX PA
port:       1:0:297: HDMI TX PA


slot:       4
rev:        1
class:      Quantum Data, Inc. 980ATP HDMI 1.4 generator analyzer
device:     a001
pci:        00:04:00
qdbus:      SLAVE
port:       0:1:297: HDMI TX
port:       1:1:297: HDMI TX
port:       2:0:297: HDMI RX


slot:       6
rev:        1
class:      Quantum Data, Inc. DP protocol analyzer
device:     e010
pci:        01:00:00
qdbus:      SLAVE
port:       0:1:600: DP TX
port:       1:2:600: DP TX
port:       2:0:600: DP RX PA


#dp-scope>
```

The discover command in the example above indicates that the DP module is installed in Slot 6.

14.1 Video-Related commands

Refer to the following tables for the supported commands.

ALLU

Command supported?: Y	Query supported?: N

Same as the FMTU command.

Example:

```
FMTL 720p60
ALLU
```

DVQM

Command supported?: Y	Query supported?: Y

Sets the quantization mode (color range) for the video. Valid values are: 0 = 0-255; 2 = 16-235.

Requires FMTU or ALLU to activate.

Query returns the current setting of the digital quantization mode.

Examples:

```
DVQM 2      // sets the mode or range to 16-235).
```

or

```
DVQM 0      // sets the mode or range to 0-255).
DVQM?       // returns the current value.
```

DVSM

Command supported?: Y	Query supported?: Y

Sets the sampling mode between 4:4:4 and 4:2:2 in YCbCr mode. Valid values are: 2 = 4:2:2; 4 = 4:4:4.

Requires FMTU or ALLU to activate.

Query returns the current setting of the digital sampling mode.

Examples:

```
DVSM 2      // sets the sampling to 4:2:2.
```

or

```
DVSM 4      // sets the sampling to 4:4:4.
DVSM?       // returns the current value.
```

DVST

Command supported?: Y	Query supported?: Y

Sets the digital video signal type. Valid values are: RGB = 10; YCbCr = 14.

Requires FMTU or ALLU to activate.

Query returns the current setting of the digital video signal type.

Example:

```
DVST 10     // activates the HDMI/DVI output for RGB video).
DVST?       // returns the current value.
```

FMTL

Command supported?: Y	Query supported?: Y

Loads a format. Takes a format name as a parameter. Requires FMTU or ALLU to activate.

Requires FMTU or ALLU to activate.

Query returns the currently loaded format.

Examples:

```
FMTL 720p60   // loads the 720p60 format.
FMTL?         // returns the current value.
```

FMTU

Command supported?: Y	Query supported?: Y

Uses the currently loaded format.   Takes no parameters.

Query returns the currently used format.

Example:

```
FMTL 720p60
FMTU
```

IMGL

Command supported?: Y	Query supported?: Y

Loads an image. Takes an image name as a parameter.

Requires IMGU, FMTU or ALLU to activate.

Query returns the currently loaded image.

Example:

```
IMGL SMPTEBar    // loads smptebar image
```

IMGU

Command supported?: Y	Query supported?: Y

Uses (activates) the currently loaded image.   Takes no parameters.

Query returns the currently used image.

```
IMGL SMPTEBar
IMGU
```

ISUB

Command supported?: Y	Query supported?: Y

Enables or disables activation of alternate versions of test images if they have alternate versions. Takes no parameters.

Query returns the current setting.

```
IMGL graysall   // loads the SlideBox image
ISUB 1          // enables alternate versions of the image
IVER 1          // activates the first version of an image
IMGU             // invokes the image and image version.
ISUB 0          // disables alternate versions of the image
```

IVER

Command supported?: Y	Query supported?: Y

Enables or disables activation of alternate versions of test images if they have alternate versions. Takes no parameters.

Query returns the current setting.

```
IMGL graysall    // loads the SlideBox image
ISUB 1           // enables alternate versions of the image
IVER 100         // activates the 100th version of the image
IMGU             // invokes the image and image version.
```

NBPC

Command supported?: Y	Query supported?: Y

Sets the number of bits per component on HDMI. Valid values are: 8 = 8 bits per component; 10 = 10 bits per component; 12 = 12 bits per component. Only affects output when color space is RGB or YCbCr 4:4:4.

Requires FMTU or ALLU to activate.

Query returns the current setting of the number of bits per component.

Example:

```
NBPC 12      // sets the component bit depth to 12 bits
NBPC?       // returns the current value.
```

OUTG

Command supported?: Y	Query supported?: Y

Sets the enable gate of video output. (This is defaulted to 1 – only set to 0 to disable video when absolutely necessary.)
Requires FMTU or ALLU to activate.
Query returns the current setting for the enable gate for the video.
Example:

```
OUTG 1       // enables the outputs.
OUTG?        // returns the current setting.
```

REDG/GRNG/BLUG

Command supported?: Y	Query supported?: Y

Enables red/green/blue, respectively. (Also see XVSG.)
Requires FMTU or ALLU to activate.
Query returns the current setting for enabling red, green, blue video.
Examples:

```
REDG 1      // enables the red output channel.
GRNG 0      // disables the green output channel.
BLUG 1      // enables the blue output channel.
BLUG?       // returns the current setting.
```

SCAN

Command supported?: Y	Query supported?: Y

Sets the current format to either progressive (SCAN 1) or interlaced (SCAN 2).
Requires FMTU or ALLU to activate.
Query returns the current setting for the scan type.
Example:

```
SCAN 1     // sets the output to progressive.
SCAN?      // returns the current setting.
```

XVSI

Command supported?: Y	Query supported?: Y

Sets the video interface of the unit.
Requires FMTU or ALLU to activate.
Query returns the current interface activation setting.
Examples:

```
XVSI 2     // Sets DVI Computer formats
XVSI 3     // Sets DVI TV formats
XVSI 4     // Sets active interface to HDMI
```

14.2 Audio Generation-Related commands

Refer to the following table lists the audio related commands for generation.

DASI

Command supported?: Y	Query supported?: Y

Sets the digital audio signal interface.
Requires FMTU or ALLU to activate.
Valid values are:

0 – off (if previously selected audio is not analog)

1 – DP

6 - HDMI

Examples:

```
DASI 6      // sets the digital audio signal to DisplayPort.
DASI?       // returns the current setting.
```

ARAT

Command supported?: Y	Query supported?: Y

Sets the audio sampling rate on HDMI LPCM audio.

Requires FMTU or ALLU to activate.

Parameter values:
- *rate* = sampling rate; 32000, 44100, 48000, 88200, 96000, 176400, 192000

Examples:

```
ARAT 48000   // sets the sampling rate to 48kHz.
ARAT?       // returns the current setting of the sampling rate.
```

NBPA

Command supported?: Y	Query supported?: Y

Sets the number of bits per sample in analog and HDMI PCM audio.

Requires FMTU or ALLU to activate.

Parameter values:
- *bits* = number of bits per sample; 16, 20 or 24

Examples:

```
NBPA 24    // sets the value of audio depth.
NBPA?     // returns the current setting.
```

NDAC

Command supported?: Y	Query supported?: Y

Sets the number of digital audio channels for an LPCM audio signal.

Requires FMTU or ALLU to activate.

Parameter values:
- *ch* = channels; 2 - 8

Examples:

```
NDAC 8    // sets the number of channels to 8.
NDAC?    // returns the current setting.
```

SAMP

Command supported?: Y	Query supported?: Y

Sets the amplitude on either a specific channel or all channels.

Requires FMTU or ALLU to activate.

Syntax: SAMP <*amp*> <*ch*>

Possible parameter values:
- *amp* amplitude; min = -99dB, max = 0dB
- *ch* = channel; 0 - 7

Examples:

```
SAMP -12      // sets all channels to -12dB.
```

Or

```
SAMP -3 1     // sets channel #1 to -3dB – valid channels are 0-7.
SAMP?        // returns the current setting.
```

SRAT

Command supported?: Y	Query supported?: Y

Sets the sine wave frequency on either a specific channel or all channels.

Requires FMTU or ALLU to activate.

Examples:

```
SRAT 1000   // Sets all channels to 1KHz.
Or
SRAT 440 1  // Sets channel #1 to 440Hz – valid channels are 0-7.
SRAT?      // returns the current value.
```

14.3 Analyzer-Related commands

Refer to the following tables for the supported commands related to the analyzer function for testing DP source devices.

LINK VSTAT

Command supported?: Y	

Queries for the incoming DisplayPort stream attributes.

Example:

```
LINK VSTAT
```

Sample response:

```
Lane count: 4          // lanes used
Bandwidth: 8.1        // link rate
Hactive: 1920          // horizontal active video (pixels)
Htotal: 2200           // horizontal total video including “blanking” (pixels)
Vactive: 1079          // vertical active video (lines)
Vtotal: 1125           // vertical total video including “blanking” (lines)
Scan: Progressive
BPC: 8                 // bits per component
YCC Color: N/A
Components: Adobe RGB
HDCP encryption: off  // status of HDCP encryption
```

DPRX MSA

Command supported?: Y	

Queries for the incoming DisplayPort main stream attributes and presents the results in hex format. The main stream attributes are Attributes describing the main video stream format in terms of geometry and color format. They are inserted once per video frame during the video blanking period.

Example:

```
DPRX MSA
```

Sample response:

```
Clocks, H Total: 0x00000898    // horizontal total clock cycles
Hsync Polarity: 0x00000001     // horizontal sync pulse polarity 0 = active high pulse
                                  or 1 = active low pulse
Clocks, V Total: 0x00000465    // vertical total clock cycles
Vsync Polarity: 0x00000001     // vertical sync pulse polarity 0 = active high pulse
                                  or 1 = active low pulse
```

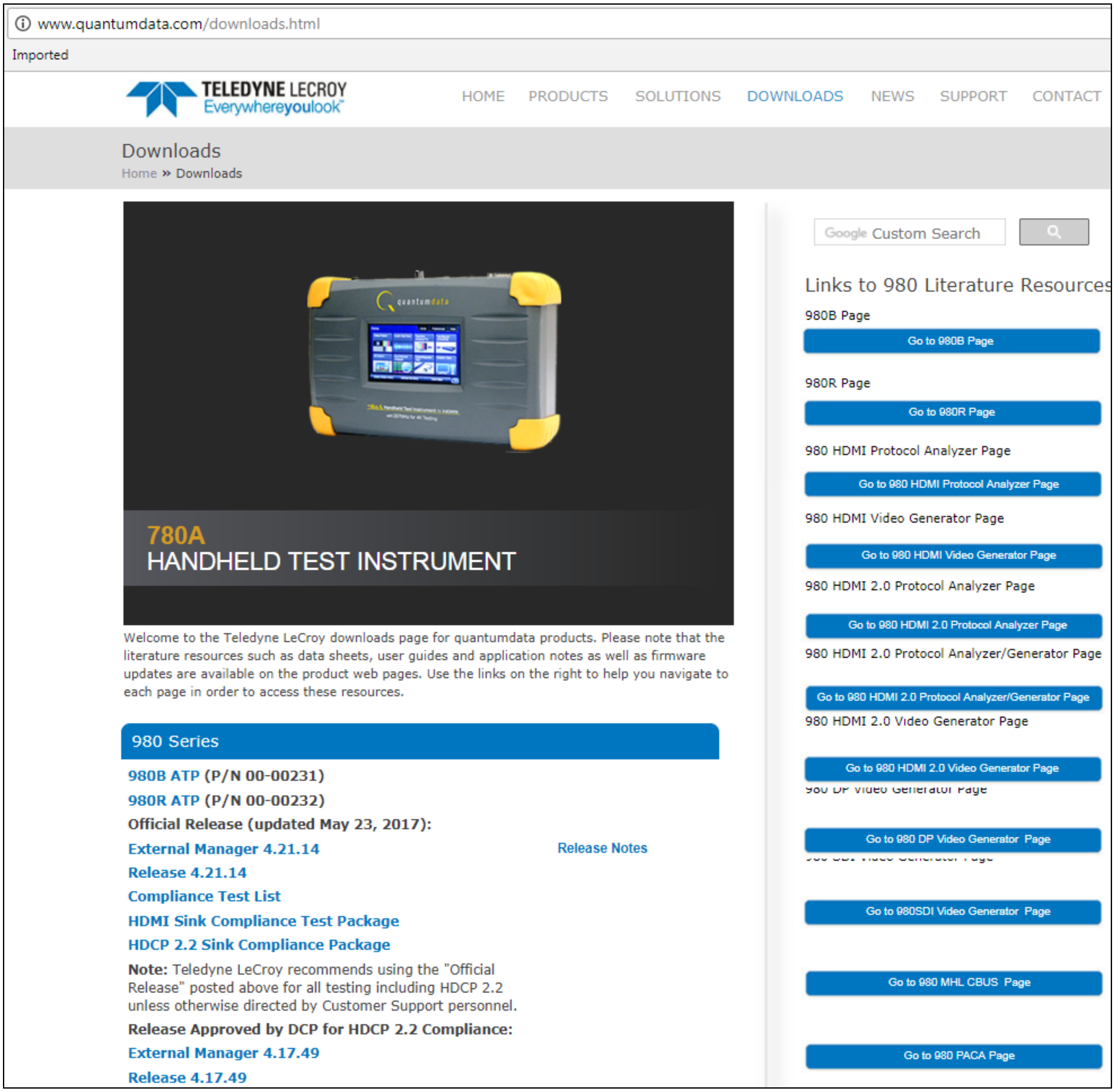
```
HSync Width: 0x0000002c        // horizontal sync pulse width
VSync Width: 0x00000005        // vertical sync pulse width
Horz Resolution: 0x00000780    // horizontal active resolution clock cycles
Vert Resolution: 0x00000438    // vertical active resolution clock cycles
Horz Start: 0x000000c0         // starting pixel for active resolution
Vert Start: 0x00000029         // starting line for active resolution
Misc0: 0x00000038
Misc1: 0x00000000
M Vid: 0x00002333              // M value for video
N Vid: 0x00008000              // N value for video
VB-ID: 0x00000010
```

15 Upgrading the 980 Manager and 980

This Chapter provides information about upgrading your 980 and 980 GUI Manager. Detailed procedures are not provided in this document. ***Please be sure to refer to the Release Notes for a specific release for detailed upgrade instructions.***

Quantum Data periodically provides maintenance release of software and firmware. The most recent versions are available on the downloads page of the Quantum Data website.

http://www.quantumdata.com/downloads/index.asp



Welcome to the Teledyne LeCroy downloads page for quantumdata products. Please note that the literature resources such as data sheets, user guides and application notes as well as firmware updates are available on the product web pages. Use the links on the right to help you navigate to each page in order to access these resources.

980 Series

980B ATP (P/N 00-00231)

980R ATP (P/N 00-00232)

Official Release (updated May 23, 2017):

External Manager 4.21.14 Release Notes

Release 4.21.14

Compliance Test List

HDMI Sink Compliance Test Package

HDCP 2.2 Sink Compliance Package

Note: Teledyne LeCroy recommends using the "Official Release" posted above for all testing including HDCP 2.2 unless otherwise directed by Customer Support personnel.

Release Approved by DCP for HDCP 2.2 Compliance:

External Manager 4.17.49

Release 4.17.49

Links to 980 Literature Resources

980B Page

Go to 980B Page

980R Page

Go to 980R Page

980 HDMI Protocol Analyzer Page

Go to 980 HDMI Protocol Analyzer Page

980 HDMI Video Generator Page

Go to 980 HDMI Video Generator Page

980 HDMI 2.0 Protocol Analyzer Page

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980 HDMI 2.0 Protocol Analyzer/Generator Page

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980 HDMI 2.0 Video Generator Page

Go to 980 HDMI 2.0 Video Generator Page

980 DP Video Generator Page

Go to 980 DP Video Generator Page

Go to 980SDI Video Generator Page

Go to 980 MHL CBUS Page

Go to 980 PACA Page

Two software packages are available for upgrading the 980:

1. Embedded firmware and gateware package for the 980 instrument. This is a Debian software package for installation in the Linux-based instrument. (The file extension is .deb.) This package also includes the embedded Graphical User Interface that will be installed for the Touch Screen User Interface. The 980 software package includes the firmware and gateware for all available modules.
2. Graphical User Interface for Windows PCs. This is the 980 Manager GUI that can be used to control all 980 instruments from a Windows PC.

   Notes:

   1. If the Windows-based 980 Manager GUI and the embedded firmware are both being upgraded, we recommend upgrading the 980 Manager first, and then upgrading the embedded firmware.
   2. Be sure to check the release notes associated with the download files. Any special installation instructions will be noted in the release notes.

16 Image Reference

16.1 Standard image descriptions

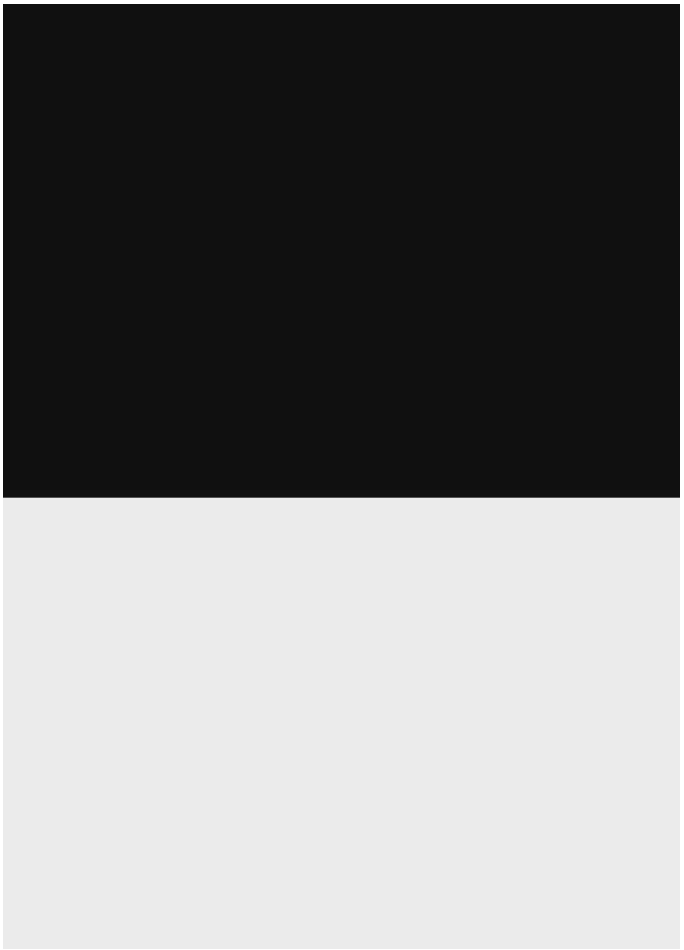
This section provides a reference for the test patterns available with the 980 Video Generator Module.

16.2 3DXTalk

The 3DXTalk is an image for testing 3D crosstalk.

16.2.1 Description

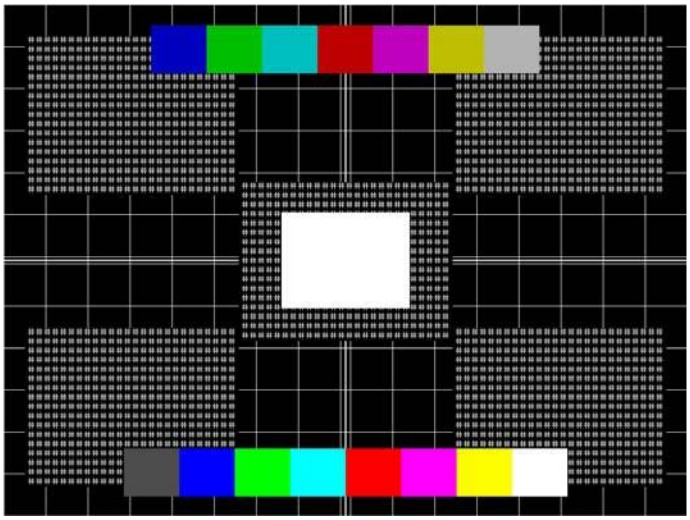
Test image for testing 3D crosstalk.



16.3 Acer1

16.3.1 Description

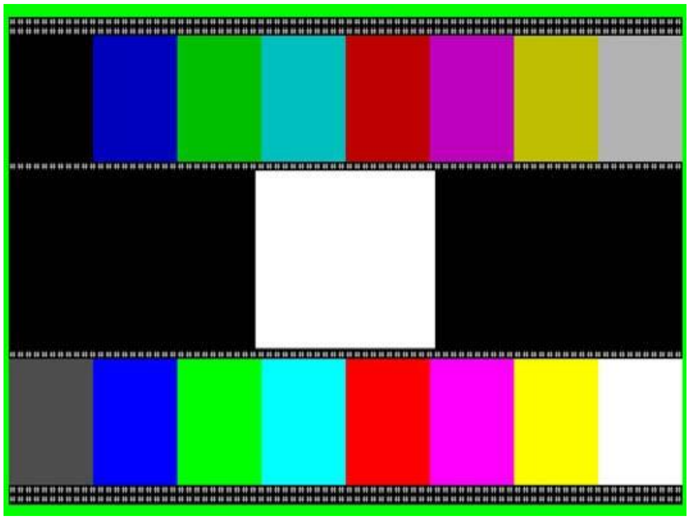
Special test image developed per customer specifications. Consists of two sets of color bars and five blocks of “#” characters on a white crosshatch with a black background.



16.4 Acer2

16.4.1 Description

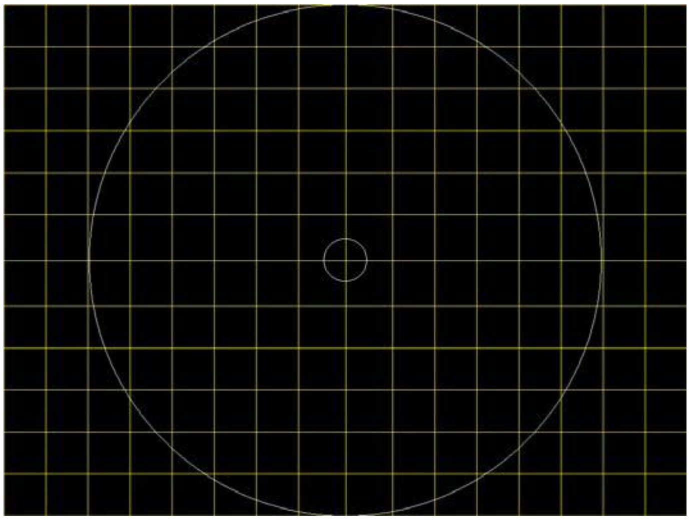
Special test image developed per customer specifications. Consists of colorbars, lines of “#” characters, and a green border.



16.5 Acer3, Acer4, Acer5, Acer6

16.5.1 Description

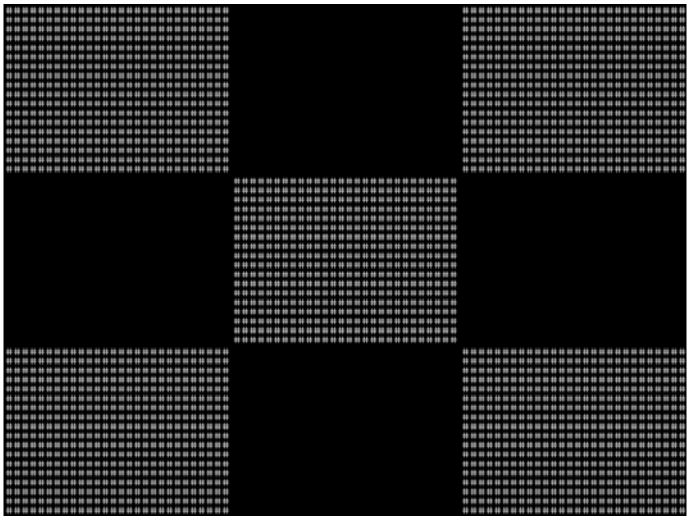
Special test images developed per customer specifications. Consists of large and small white circles centered on either a yellow (Acer3), magenta (Acer4), cyan (Acer5), or white (Acer6) crosshatch on a black background. The Acer3 image is shown below.



16.6 Acer7 and Acer8

16.6.1 Description

Special test image developed per customer specifications. In the primary version, five blocks of either white “#” (Acer7) or “H” (Acer8) characters on a black background are displayed. A secondary version displays black characters on a white background. The Acer7 image is shown below.



16.7 Acer9

16.7.1 Description

Special test image developed per customer specifications. In the primary version, a mostly white field is displayed with two rows of color bars at the bottom. A secondary version displays a black field with the two rows of color bars at the bottom.

16.8 AFDtest

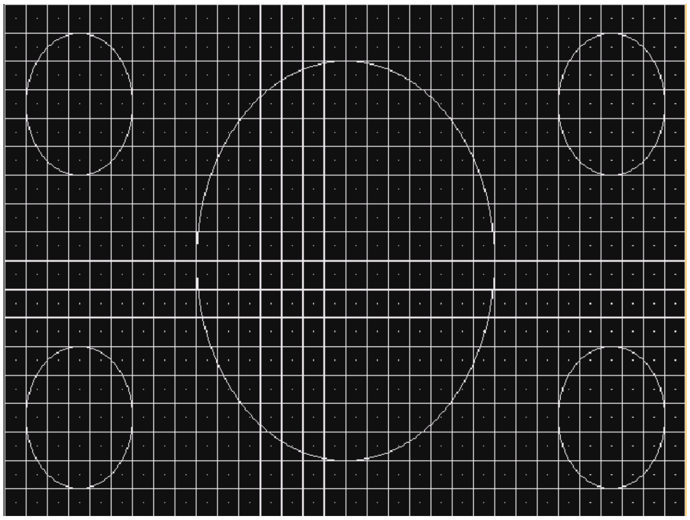
16.8.1 Description

Used to test HDMI content mapping using different EIA/CEA-861-B formats. There are 10 different versions of this image.

16.9 Anamorph

16.9.1 Description

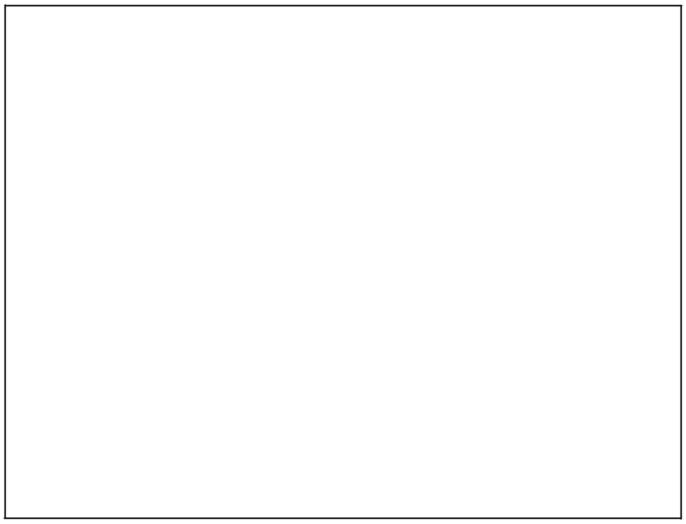
The primary version displays a white background with a small black pixel in the center fills the active video area. A secondary version displays a black background with a small white pixel in the center.



16.10 AnsiGray

16.10.1Description

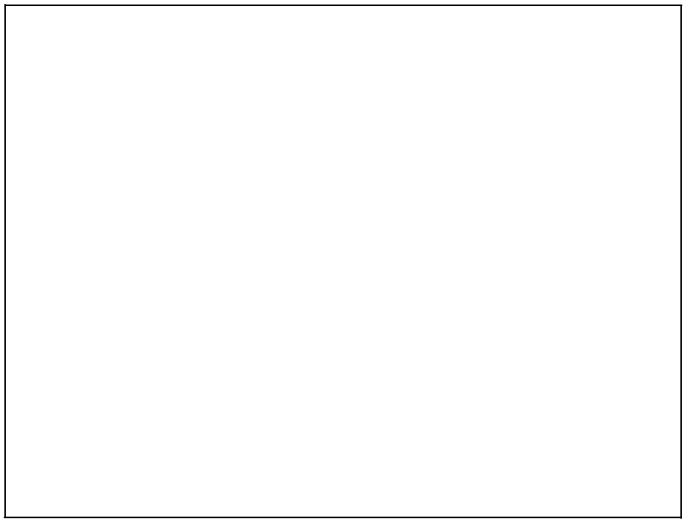
The primary version displays a white background with a small black pixel in the center fills the active video area. A secondary version displays a black background with a small white pixel in the center.



16.11 AnsiLght

16.11.1Description

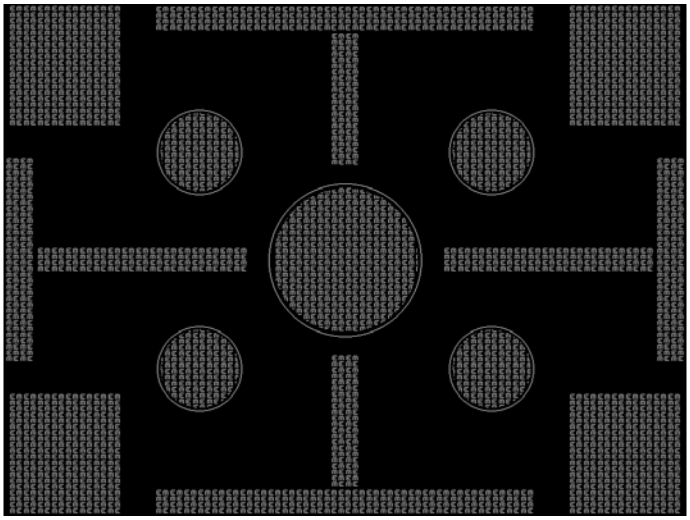
The primary version displays a white background with a small black pixel in the center fills the active video area. A secondary version displays a black background with a small white pixel in the center.



16.12 Apple 1

16.12.1Description

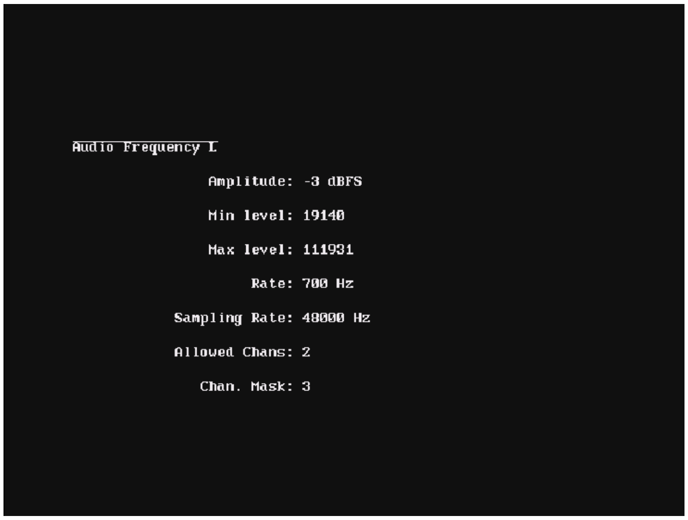
Special test image developed per customer specifications. A secondary version shows reverse (black characters on white background).



16.13 Audio_L, Audio_Lf, Audio_R, Audio_Rf, Audio_X, Audio_Xf

16.13.1Description

Used to configure HDMI audio output signal. The Audio_L is shown below. For more information, see “Testing HDMI audio” on page 305.

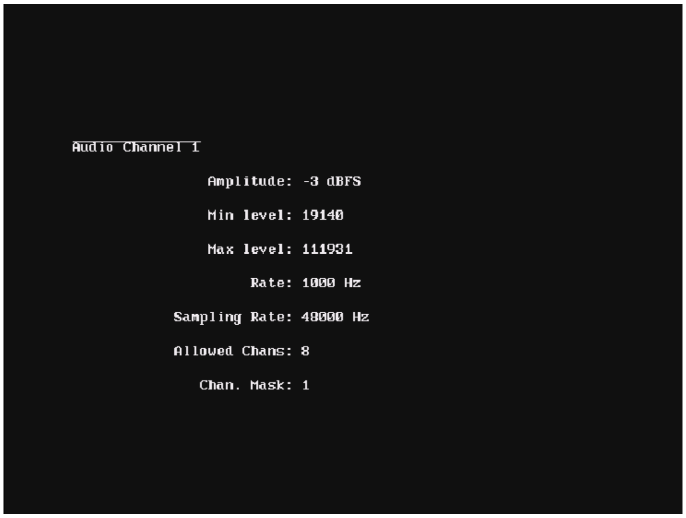


```
Audio Frequency L

                Amplitude: -3 dBFS

                Min level: 19140

                Max level: 111931

                     Rate: 700 Hz

            Sampling Rate: 48000 Hz

            Allowed Chans: 2

               Chan. Mask: 3
```

16.14 Audio_1, Audio_1f, Audio_2, Audio_2f, Audio_3, Audio_3f, Audio_4, Audio_4f, Audio_5, Audio_5f , Audio_6, Audio_6f, Audio_7, Audio_7f, Audio_8, Audio_8f

16.14.1Description

To support testing of HDMI audio, the 882 provides 8-channel LPCM audio (using an internally-generated sinewave) at the highest audio sampling rate (192 kHz).

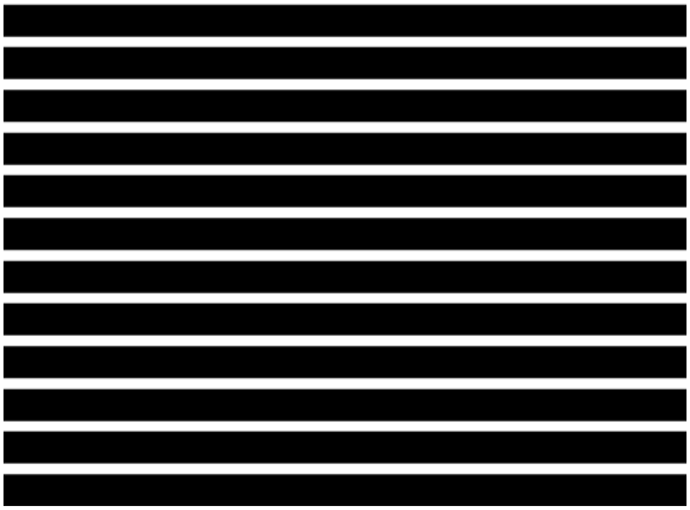


```
Audio Channel 1

          Amplitude: -3 dBFS

          Min level: 19140

          Max level: 111931

               Rate: 1000 Hz

      Sampling Rate: 48000 Hz

      Allowed Chans: 8

         Chan. Mask: 1
```

16.15 BarBlack

16.15.1Description

Special test image developed per customer specifications. A secondary version shows reverse (black lines on white background).

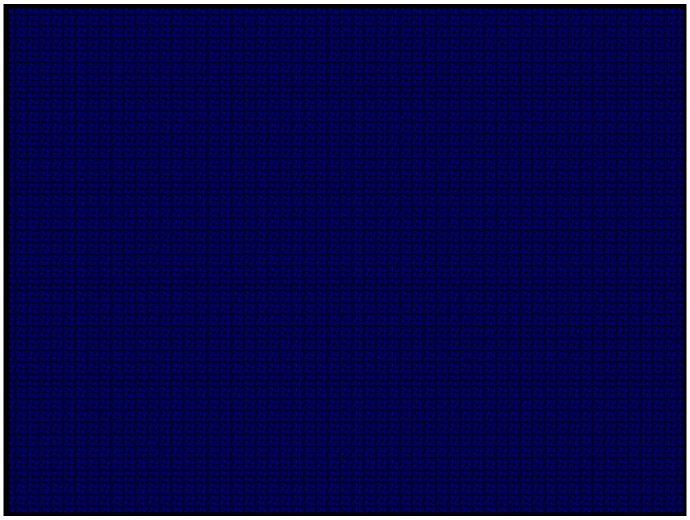


16.16 BLU_EM, GRN_EM, RED_EM, WHT_EM, MEME1111, MEMESony, MESony_B, MESony_G, and MESony_R

16.16.1 Description

In the primary version, the screen is filled with blue (BLU and B), green (GRN and G), red (R), or white (WHT, MEME1111, MEMEPlus, and MEMESony) EM character blocks on a black background. Only the white character has a secondary version. It is drawn with black characters on a white background.

A bitmap of a single character block is shown here. The BLU_EM image is shown below.



16.16.2 Purpose

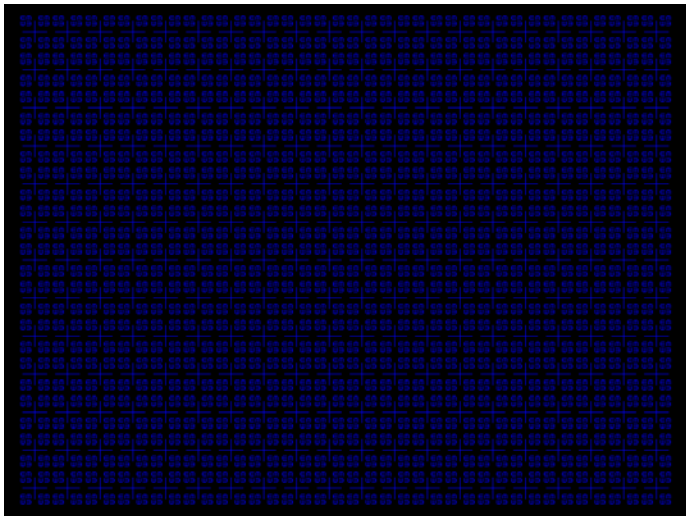
This pattern is specified by some display manufacturers for checking and adjusting focus one color at a time.

16.17 BLU_EM+, GRN_EM+, RED_EM+, WHT_EM+, MEMEPlus, MEPlus_B, MEPlus_G, and MEPlus_R

16.17.1Description

In the primary version, the screen is filled with blue (BLU and B), green (GRN and G), red (R), or white (WHT and Sony) EM character blocks on a black background. Only the white character has a secondary version. It is drawn with black characters on a white background.

A bitmap of a single character block is shown here. The BLU_EM+ image is shown below.



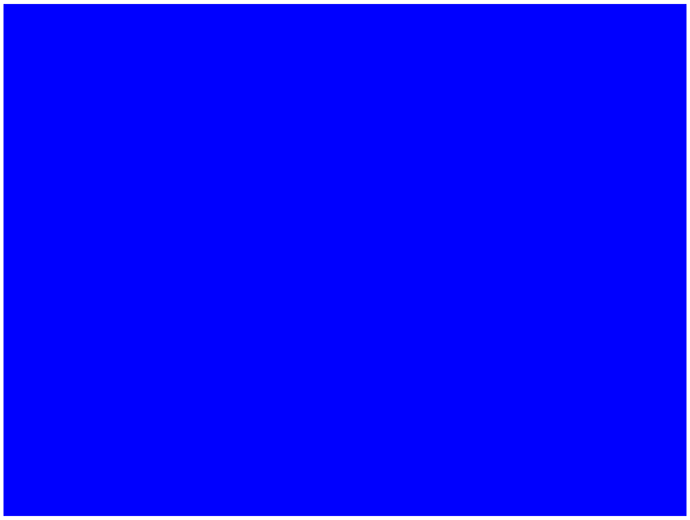
16.17.2Purpose

This pattern is specified by one or more display manufacturers for checking and adjusting focus one color at a time.

16.18 BLU_PIC, GRAY_PIC, GRN_PIC, RED_PIC, WHT_PIC

16.18.1Description

A solid blue (BLU), gray, green (GRN), red, or white (WHT) box fills the active video area. Only the white fill has a secondary version. It can be changed to a black fill by pressing the **Step** key. The BLU_PIC image is shown below.



16.18.2Test

Purity adjustment.

16.18.3Purpose

To produce correct colors in a displayed image, the electron beams from each of the three (3) guns in the CRT should strike only their matching phosphors. A white image shows patches of various colors on a monitor with bad purity. The purity adjustment(s) should be performed before doing any brightness or color tests. In some cases, purity adjustments involve loosening and repositioning the yoke, in which case purity should be adjusted prior to doing any geometry tests.

Method The methods used for adjusting purity on a color monitor depend on the type of monitor and CRT (for example; Delta, In-Line or Single Gun). In most cases, the first step is to degauss the CRT.

Note: *For a Delta Gun CRT, turn on only the red output. A solid uniform field of red should appear. If the color is not uniform, adjust the yoke and the Purity Tabs assembly.*

If purity cannot be corrected to acceptable limits, the monitor may not have been properly degaussed or there may be a defect in the CRT or purity assembly.

16.18.4Test

Shadow mask warping.

16.18.5Purpose

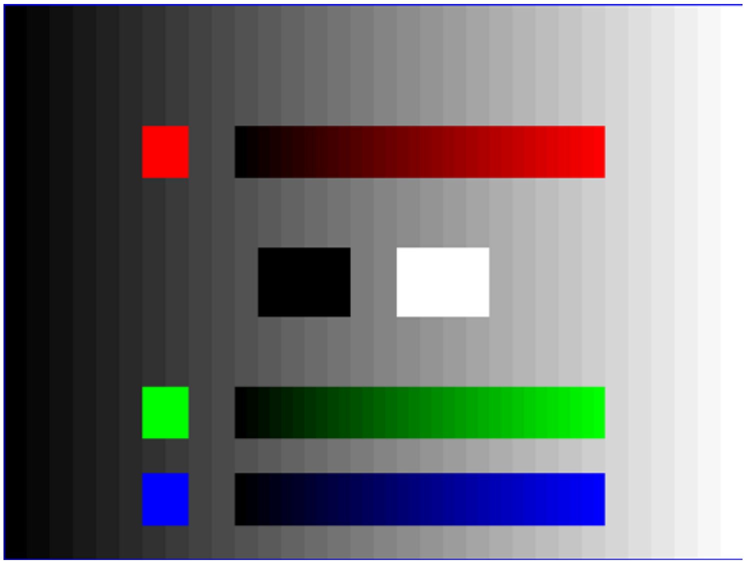
The purity characteristics of your CRT can change over time if you leave it on with a lot of video being displayed. This may be due to the CRT’s electron beams striking its shadow mask with enough energy to cause the mask to heat. This internal heating may be enough to cause the shadow mask to warp and give bad purity.

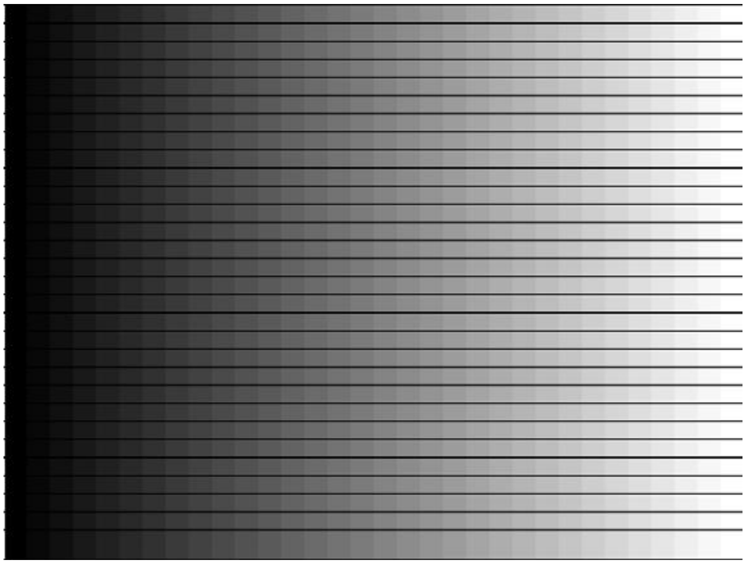
Method Set the purity image to white and allow the monitor to run for a few minutes. Any mask warping shows up as a change in purity. You can use a color meter to measure the change. The BriteBox pattern may also be useful for measuring shadow mask warping.

16.19 Bosch

16.19.1Description

Special test image developed per customer specifications. This image has 6 versions.





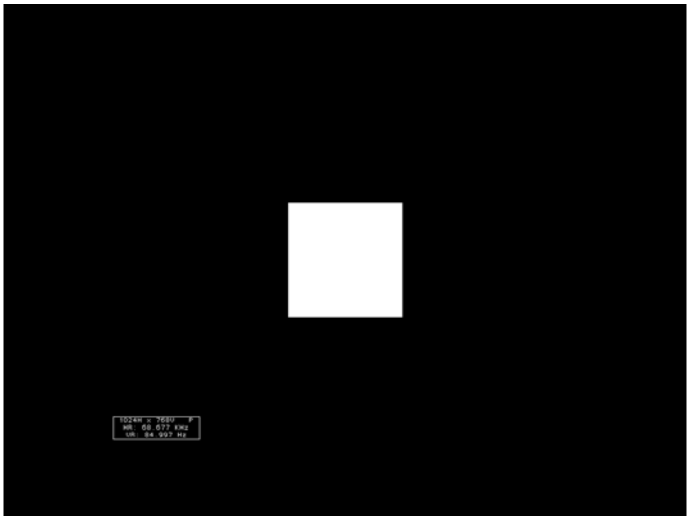
16.20 Box_50mm, Box_64mm, Box100mm, Box150mm, Box200mm, Box250mm

16.20.1Description

The primary version has a solid white box in the center of the active video. Depending on the image selected, the box is sized by square millimeters. If there is room, information on the current format appears below and to the left of the box. This shows the number of active pixels and lines as well as the horizontal and vertical scan rates. A forward slash (/) after the number of active lines indicates the format is interlaced.

Note: *The box will be the correct size only if the correct physical active video size is set in the format.*

The Box_50mm image is shown below. The secondary version draws a black box and black text on a white background.



16.20.2Test

Brightness control adjustment.

16.20.3Purpose

The wrong brightness setting may cause other tests such as Contrast, Focus, and Beam Size to be invalid. An accurate brightness setting helps give repeatable measurements throughout other tests.

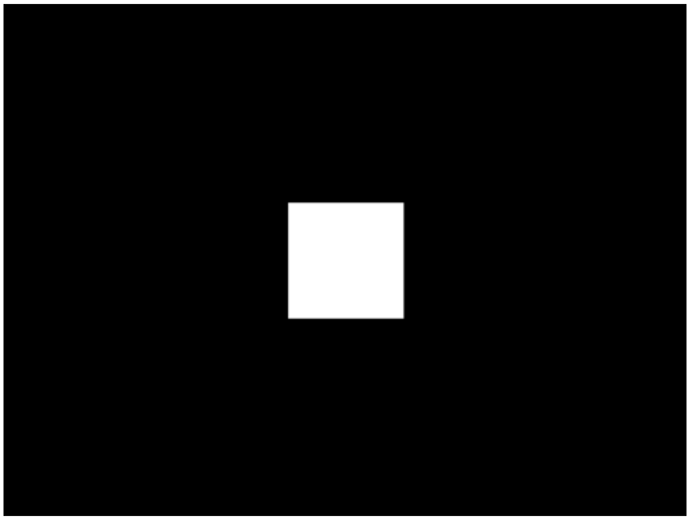
16.20.4Method

Center your light meter probe within the center square and adjust the monitor’s brightness control to obtain the required light meter reading.

16.21 BriteBox

16.21.1Description

The primary version has a single white box in the center of active video. The box size is controlled by the MSIZ system parameter. The secondary version adds four boxes in the corners of active video.



16.21.2Test

Brightness control adjustment.

16.21.3Purpose

The wrong brightness setting may cause other tests such as Contrast, Focus, and Beam Size to be invalid. An accurate brightness setting helps give repeatable measurements throughout other tests.

16.21.4Method

Center your light meter probe within the center square and adjust the monitor’s brightness control to obtain the required light meter reading.

16.21.5Test

Brightness uniformity.

16.21.6Purpose

The light output of most picture tubes varies slightly when measured across the CRT face.

This test can be used to verify that the light output variation is within your specification limits.

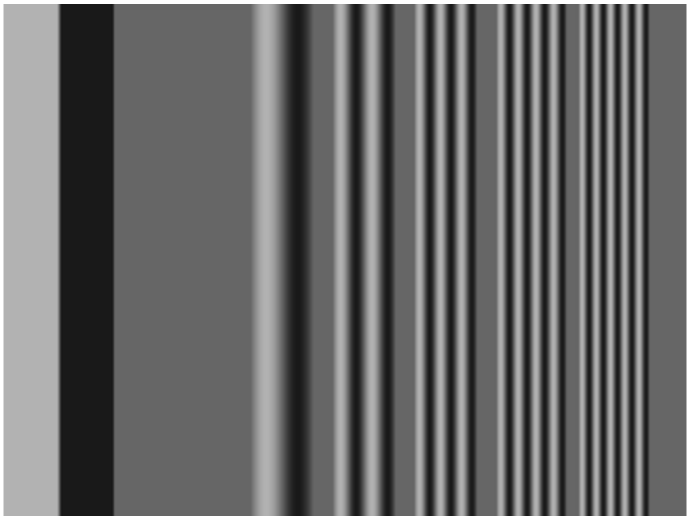
16.21.7Method

Select the inverted version and perform the Brightness Control Adjustment test on the center box. Then, center the light meter probe in each of the corner squares and note the reading you get for each square. The deviation between each of the corner readings and the center reading should be within your specification limits.

16.22 Burst (TV formats only)

Description

The left side starts with reference white (+100 IRE) and black (+7.5 IRE) levels. This is followed by six bursts of sine waves. Each burst is at a different frequency, forming vertical lines of various widths. The frequencies, going from left to right, are 0.5, 1, 2, 3, 3.58, and 4.43 MHz.



16.22.1Test

Frequency response.

16.22.2Method

When viewed on a TV screen, the peak intensities of all of the bursts should match the white reference level. The darkest portions between the peaks should match the black reference level.

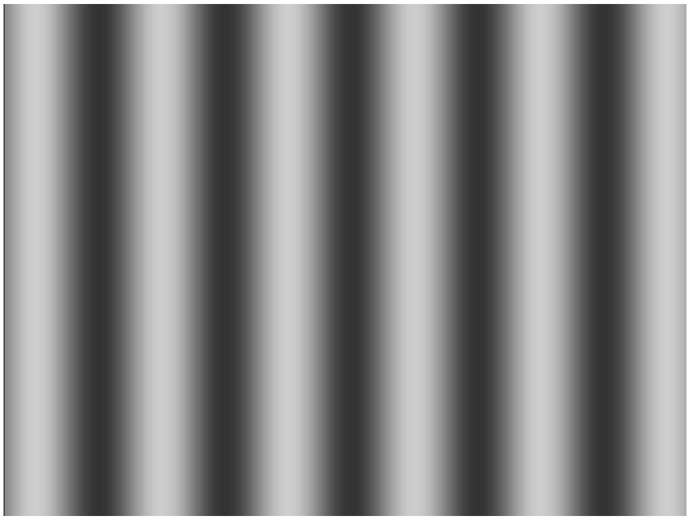
The image can also be used with a TV waveform analyzer to check the frequency response of a video system. One scan line of the image, as it would appear on a waveform analyzer, is shown at the top of the next page. High frequency roll-off (loss) would show up as a decrease in the peak-to-peak swings on the right side of the waveform. Low frequency roll-off would show up as a decrease in the peak-to-peak swings on the left side of the waveform.

Some waveform analyzers can be set to detect and display the amplitude of the peaks. A typical amplitude waveform for a good system is shown at the bottom of the next page.

16.23 BurstTCE

16.23.1Description

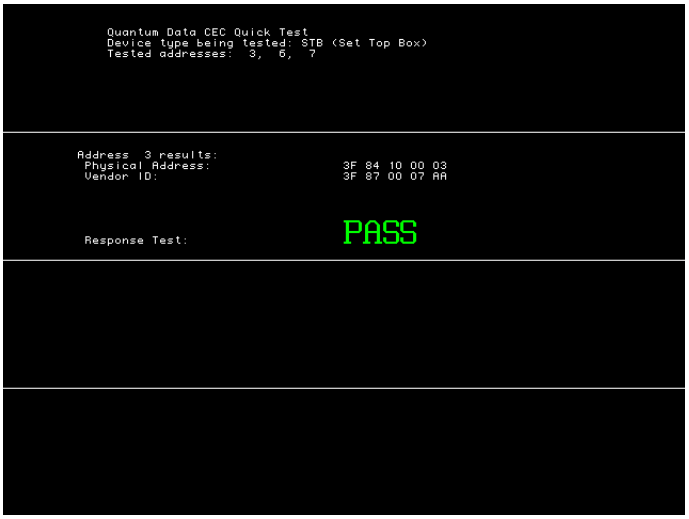
Fills screen with a 0.5 MHz frequency. This can be increased in 0.5 MHz increments through the **Settings/Rendition** dialog box.



16.24 CECTest1, CECTest2

16.24.1Description

Fills screen with a 0.5 MHz frequency. This can be increased in 0.5 MHz increments through the **Settings/Rendition** dialog box.

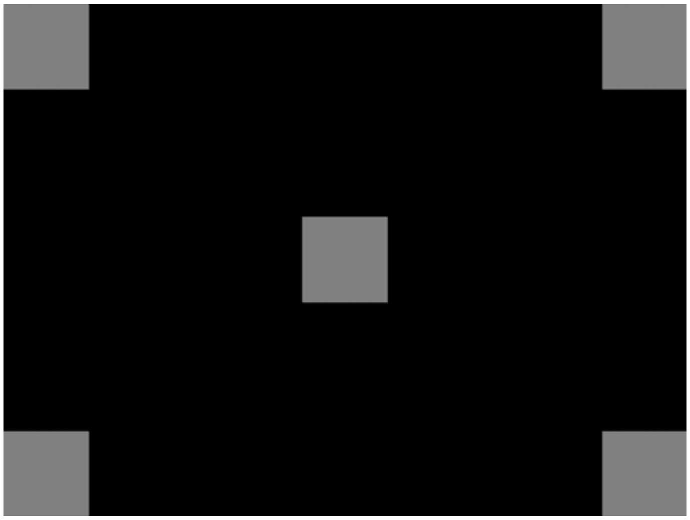


```
    Quantum Data CEC Quick Test
    Device type being tested: STB (Set Top Box)
    Tested addresses:  3,  6,  7

Address  3 results:
 Physical Address:                3F 84 10 00 03
 Vendor ID:                       3F 87 00 07 AA

 Response Test:                   PASS
```

16.25 Check511

16.25.1Description

Consists of five small boxes in the corners and at the center of the active video. The boxes are on a black background. Each box consists of alternating black and white pixels that form a very fine checkerboard. The secondary version inverts the image, creating a white background. The colors of the individual pixels in the boxes also are inverted.



16.25.2Test

Verify monitor resolution.

16.25.3Purpose

The resolution of your monitor should meet or exceed the design specifications.

16.25.4Method

First adjust the brightness, contrast, and focus to their correct settings. You should be able to see individual and distinct pixels in each of the boxes. Failure to see distinct pixels may indicate you have a defective video amplifier, focus correction circuit, or picture tube.

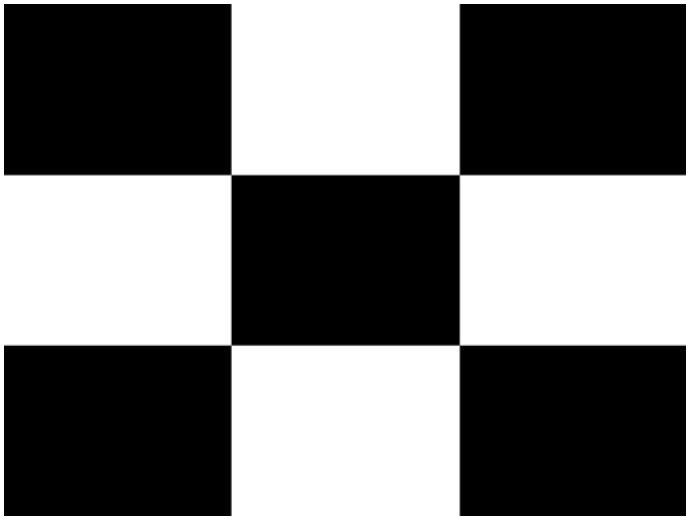
Note: *If multi-colored areas appear on a mask-type color picture tube, you may have a problem with convergence or you may be exceeding the resolution of the picture tube.*

16.26 CheckBy3

16.26.1Description

The active video area is equally divided into a 3x3 checkerboard of black and white boxes.

The primary version has four white boxes as shown in the image below. The secondary version has five white boxes (reverse).



16.26.2Test

Contrast ratio.

16.26.3Purpose

The pattern is based on a proposed ANSI method of measuring the contrast ratio of video projection systems.

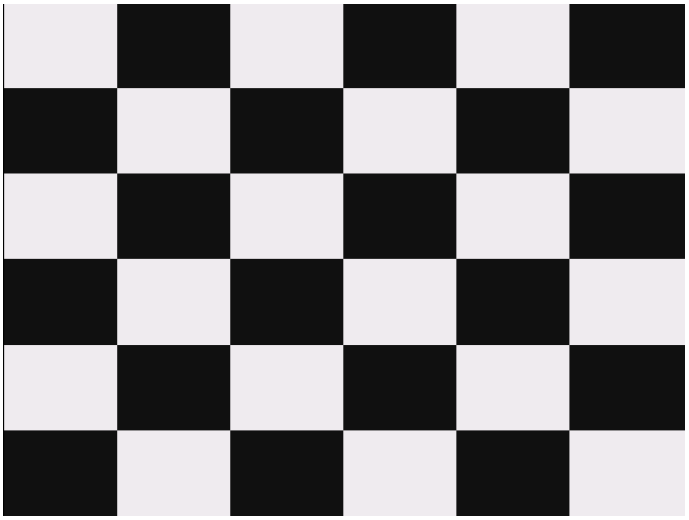
Method Using a light meter probe, measure and record the light-level reading (in foot lamberts) in the center of each of the black and white boxes. The contrast ratio is expressed as the average of all of the white readings divided by the average of all of the black readings.

16.27 CheckBy6

16.27.1Description

The active video area is equally divided into a 6x6 checkerboard of black and white boxes.

The primary version has four white boxes as shown in the image below. The secondary version has five white boxes (reverse).



16.27.2Test

Contrast ratio.

16.27.3Purpose

The pattern is based on a proposed ANSI method of measuring the contrast ratio of video projection systems.

Method Using a light meter probe, measure and record the light-level reading (in foot lamberts) in the center of each of the black and white boxes. The contrast ratio is expressed as the average of all of the white readings divided by the average of all of the black readings.

16.28 Check_02

16.28.1Description

Primary version is shown below. The secondary version has reverse (black lines on white background).

16.29 Check_11

16.29.1Description

In the primary version, the active video area is filled with alternating black and white pixels that form a very fine checkerboard, as shown below. The secondary version inverts the colors in the image. The inverted image looks almost the same as the non-inverted version.

16.29.2Test

Verify monitor resolution.

16.29.3Purpose

The resolution of your monitor should meet or exceed the design specifications.

16.29.4Method

Adjust the brightness, contrast, and focus to their correct settings first. You should be able to see individual and distinct pixels in each of the boxes. Failure to see distinct pixels may indicate you have a defective video amplifier, focus correction circuit, or picture tube.

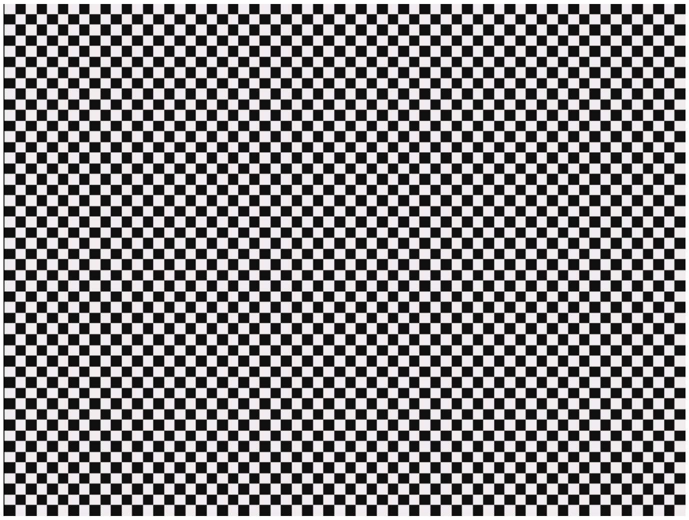
Note: *If multi-colored areas appear on a mask-type color picture tube, you may have a problem with convergence, or you may be exceeding the resolution of the picture tube.*

16.30 Checkers

16.30.1Description

This image has two color checker type arranged in a checker board pattern. It enables you to show a contrast of color depth for each type of checker type. For example you can specify one tile to use 12 bit deep color and the other checker tile to use 10 bit color. You can then view the image and see whether distinquish between the two checker types. You need to set the pixel depth in the generator to 24 bit (PELD = 32) in order to access 512 grayscale or color levels for each tile for a single image rendered on a display.

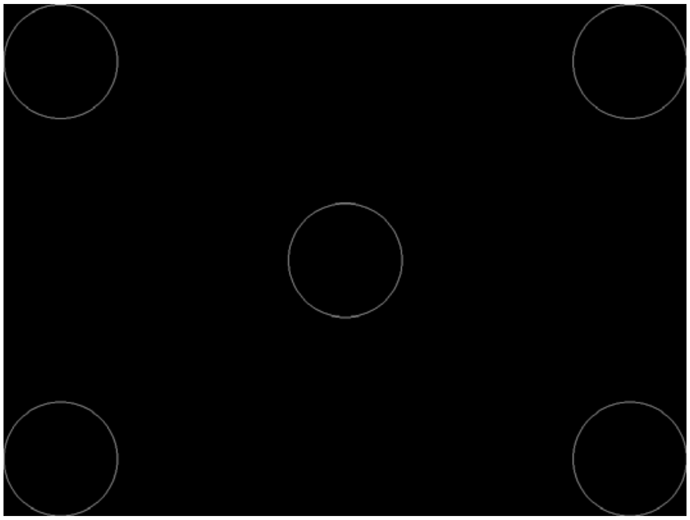
The following is a sample of the Checkers image is rendered on a display.



16.31 CirclesL

16.31.1Description

Special test image developed per customer specifications. In the primary version (shown below), the image consists of five large white circles on a black background. The circles are positioned in the center and in the corners of the active video area. The secondary version inverts the image to black circles on a white background.



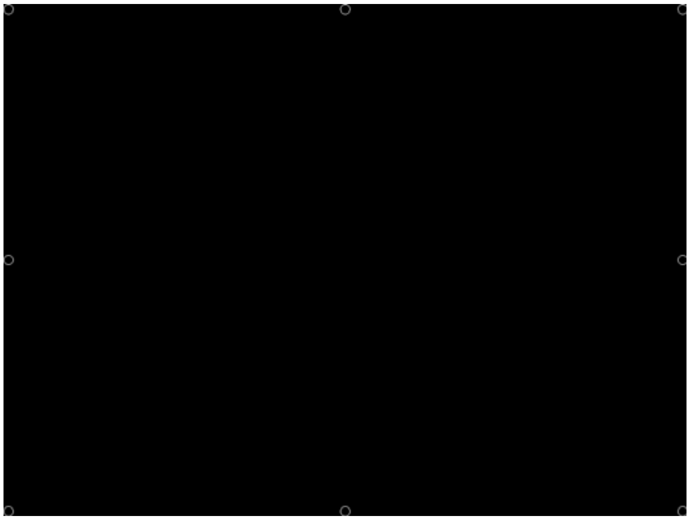
16.31.2Purpose

This pattern is specified by some monitor manufacturers for checking and adjusting video scan size, linearity, and over scanning.

16.32 CirclesS

16.32.1Description

Special test image developed per customer specifications. In the primary version (shown below), the image consists of eight small white circles on a black background. The circles are positioned in the corners of the active video area and centered on each edge of the active video area. The secondary version inverts the image to black circles on a white background.



16.32.2Purpose

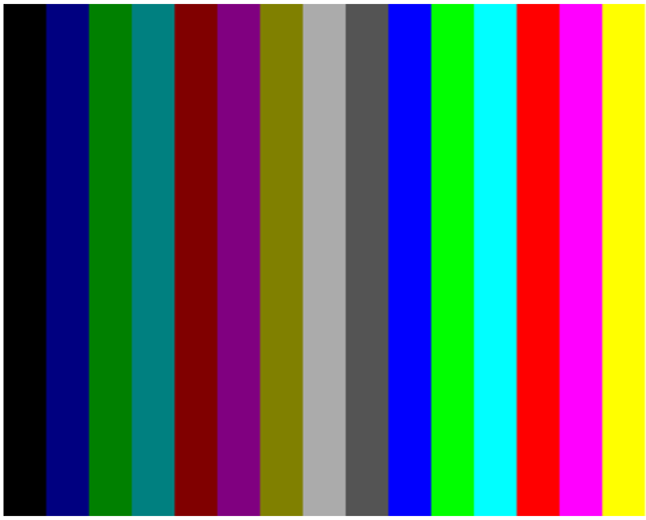
This pattern is specified by some monitor manufacturers for checking and adjusting video scan size, linearity, and over scanning.

16.33 ColorBar

16.33.1Description

The primary version (shown below) has 16 full-height vertical color bars. The secondary version splits the field into a top and bottom half. The bars in the bottom half of the screen are in reverse order.

Note: *When outputting digital video, 33% Gray changes to 50% Gray, and 67% Gray becomes either Black or some gray level depending on how the display interprets the video information.*



16.33.2Test

Verify that all video channels are functional.

16.33.3Purpose

To verify that none of the video channels are bad or connected incorrectly.

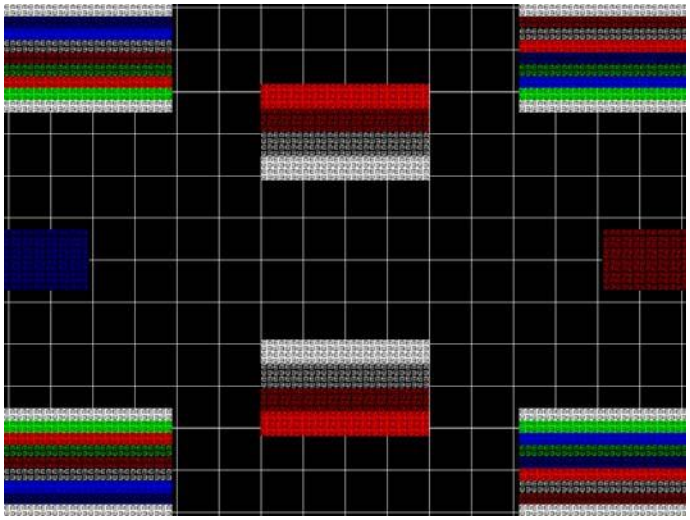
16.33.4Method

Compare the sequence of color bars with the table. Missing bars may indicate a dead or unconnected channel. The transition between the bars should be sharp and distinct. Each bar should also be uniform in color and intensity across its entire width. Non-uniformity may indicate problems with the response of the video amplifiers. If all the bars are present but in the wrong order, one or more inputs may be swapped.

16.34 ComFocus

16.34.1 Description

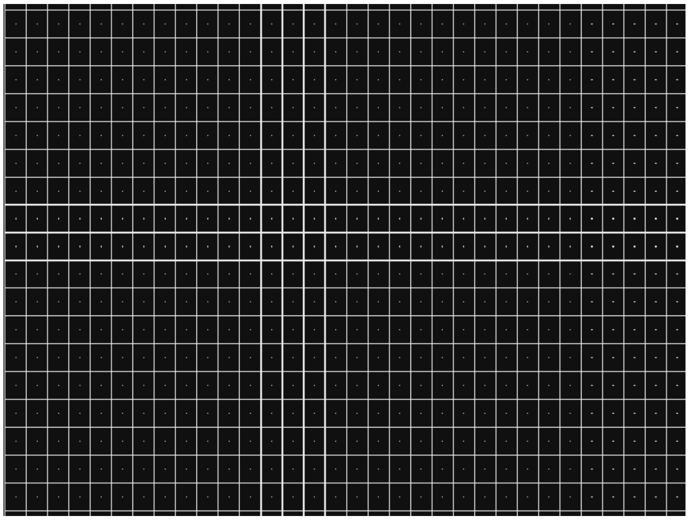
Special test image developed per customer specifications.



16.35 Crosshtch

16.35.1Description

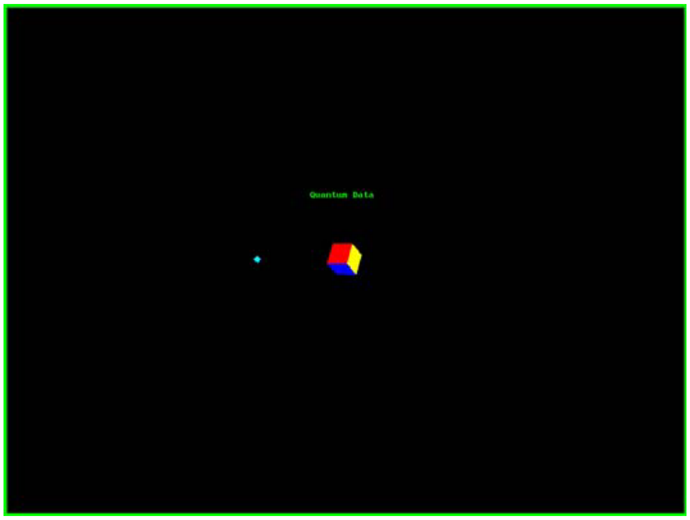
Use the following pattern to check and adjust geometric distortion, focus, beam shape, and convergence or color registration.



16.36 Cubes

16.36.1Description

This is an animated image consisting of one small multicolored cube orbiting around a larger multicolored cube. Each cube also is spinning on its own axis. The default text string is *Quantum Data*, which can be changed using commands. The primary version (shown below) has a black background and a thick green border. The secondary version uses a white background.



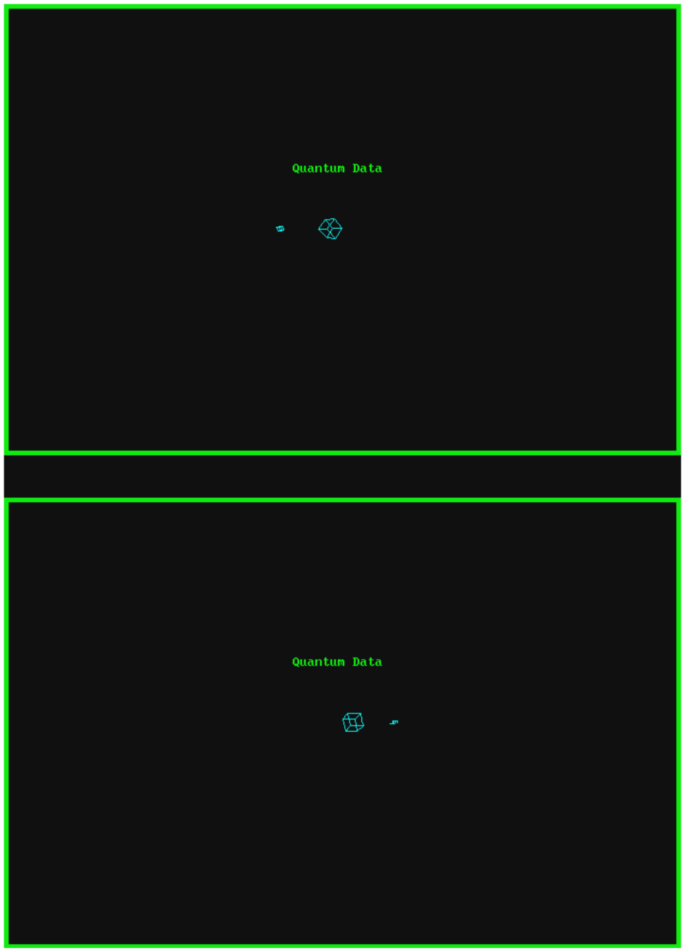
16.36.2Purpose

Can be used for show demonstrations with your own text.

16.37 CUBES3D

16.37.1Description

Test image for testing 3D motion.



16.38 DecodAdj

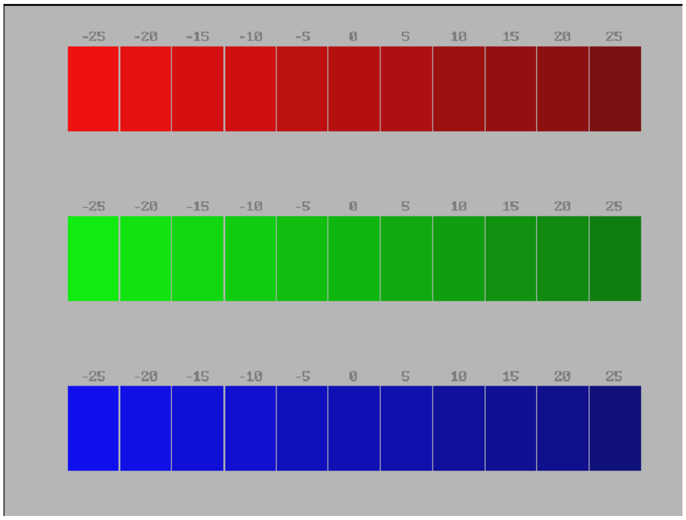
16.38.1Description

To check the color decoder performance to determine if the decoder over-emphasizes red or green colors.

16.39 DecodChk

16.39.1Description

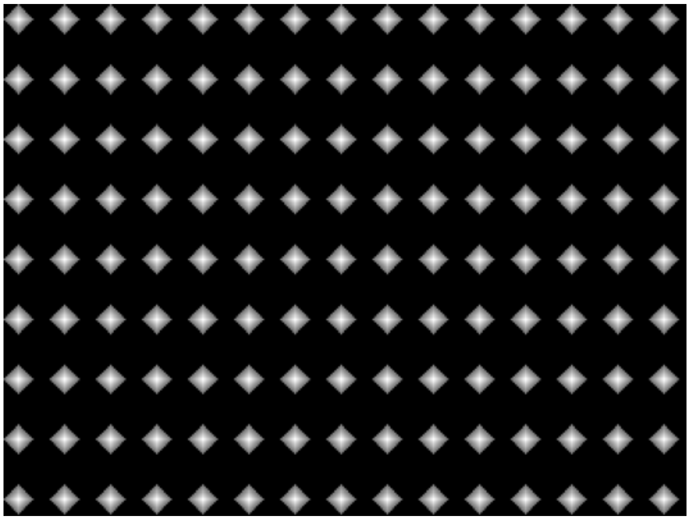
To check the color decoder performance to determine if the decoder over-emphasizes red or green colors.



16.40 Diamond1

16.40.1Description

Special test image developed per customer specifications.

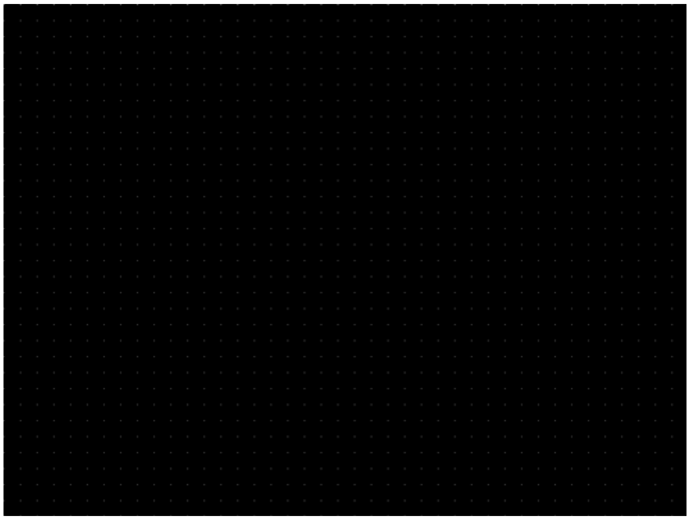


16.41 Dot1606, Dot1610, Dot1612, Dot1615, Dot1812, Dot1815, Dot2016

16.41.1Description

The primary version has white pixel dots on a black background. The secondary version has black pixel dots on a white background.

The primary version of the Dot2016 image is shown below.



16.42 DOT_10,DOT_12,DOT24

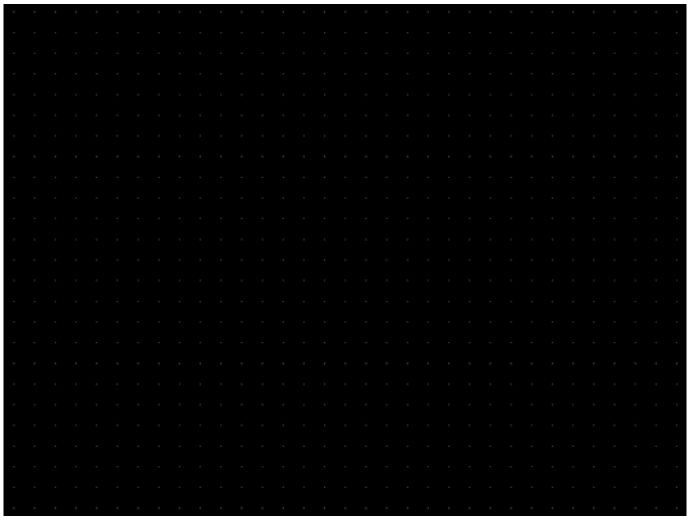
16.42.1Description

The active video area is filled with multiple rows of white, single pixel dots. The dots define the corners of what would appear to be square boxes if all connecting pixels were lit. The number of rows of boxes and the number of boxes per row depends on which version of the image is selected and the screen aspect ratio of the currently-loaded format. The number in the image's name refers to the number of boxes that will be formed along the minor axis for most aspect ratios. The generator calculates the ratio and then finds the closest match from the following table.

Aspect Ratio		**Dot_10**		**Dot_12**		**Dot_24**	
W : H	Decimal	Number of Rows	Boxes per Row	Number of Rows	Boxes per Row	Number of Rows	Boxes per Row
16 : 9	1.777 É	10	16	10	16	18	32
5 : 3	1.666 É	10	16	10	16	18	30
4 : 3	1.333 É	10	14	12	16	24	32
1 : 1	1.000	10	10	12	12	24	24

The primary version has white pixel dots on a black background. A secondary version has black pixel dots on a white background.

The primary version of the Dot_24 image is shown below.



16.42.2Purpose

To accurately produce an image on a color monitor, the three electron beams in the CRT must meet (converge) at the same location at the same time. Small dots displayed on a misconverged monitor appear as a group of multi-colored dots.

16.42.3Method

The convergence adjustments of most color monitors fall into two main categories. The first set of adjustments, usually called Static Convergence, aligns the three beams in the center of the display. This method involves turning on all three guns and adjusting the various magnets on the convergence assembly to produce all white dots in the center of the display. The convergence assembly is located on the neck of the CRT. Different monitors and CRT types may each require their own magnet-adjustment sequence.

After the center of the display is properly converged, the outer areas are adjusted by using the monitor’s Dynamic Convergence controls. The number of controls, the area of the screen they affect, and their adjustment procedure depends on the monitor under test.

16.42.4Test

Focus adjustments.

16.42.5Purpose

An out-of-focus monitor displays fuzzy pixels which, in turn, result in poorly formed and hard-to-read characters.

16.42.6Method

On monitors with a single (static) focus adjustment, adjust the control for the best average focus over the entire screen. The focus at certain locations should be within specified limits.

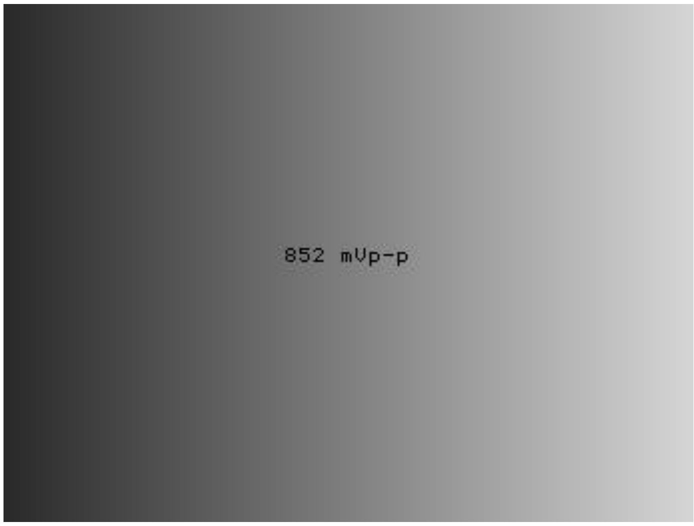
Some monitors have a static and one or more dynamic focus controls. The sequence for adjusting them and the areas of the screen they affect depend on the monitor under test.

16.43 DV_Swing, DVSwing2

16.43.1Description

This image is only available with DVI and HDMI. The DV_Swing image is used to temporally change the digital video swing (DVSS format parameter) between 90 and 1620 mVp-p of the HDMI and DVI digital output for the active format. This image displays the current video swing value over a graduated (ramp) background. This image is supported by HDMI boards (revision F or later), and DVI boards with FPGA F1 or later.

Note: *The DVSC command can be used to set the swing value between 150 and 1500 mVp-p.*



16.43.2Method

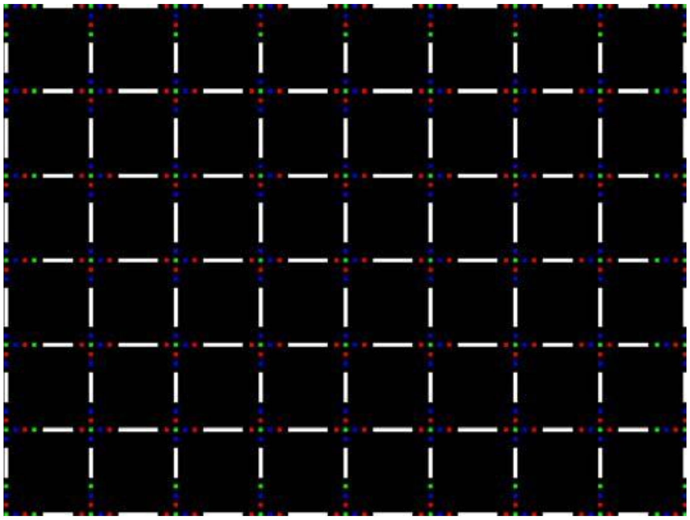
To adjust the swing in 6 mV increments, press the Contents key and then the Options key.

You then enable More and use the +/- increment keys to proceed through the subimages.

16.44 Dyna

16.44.1Description

This image has multiple versions that display different sizes of the same pattern. Version 0 is shown below.



16.44.2Description

Displays EDID from the display connected with the generator.

16.45 EdidData, Edid2

16.45.1Description

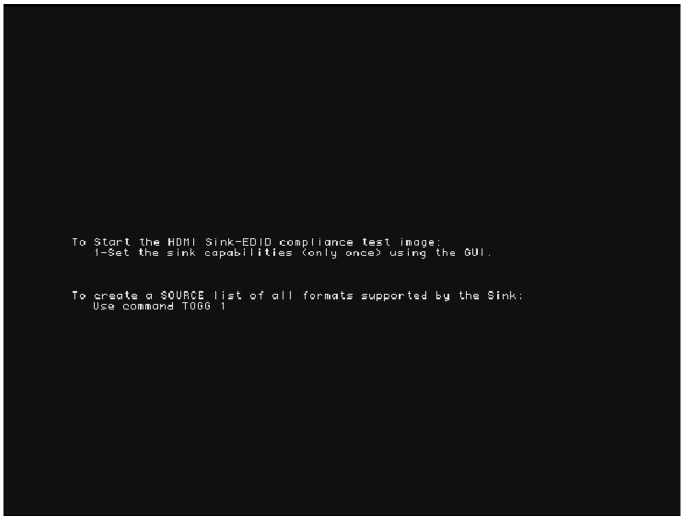
Displays EDID from the display connected with the generator.

```
To view the EDID data screens:
Press Settings->Rendition and then change the Rendition
          where n = 1 to 13
```

16.46 EdidHdmi1, EdidHdmi2

16.46.1Description

Displays EDID from the HDMI display connected with the generator.

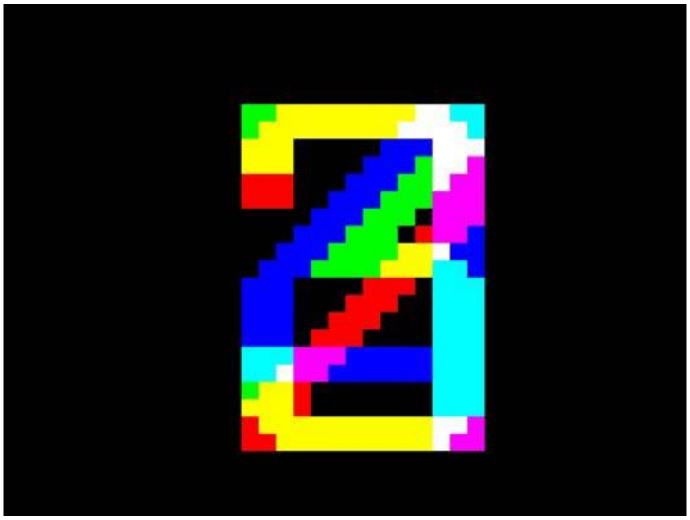


```
To Start the HDMI Sink-EDID compliance test image:
   1-Set the sink capabilities (only once) using the GUI.


To create a SOURCE list of all formats supported by the Sink:
   Use command TOGG 1
```

16.47 Elbit

16.47.1Description

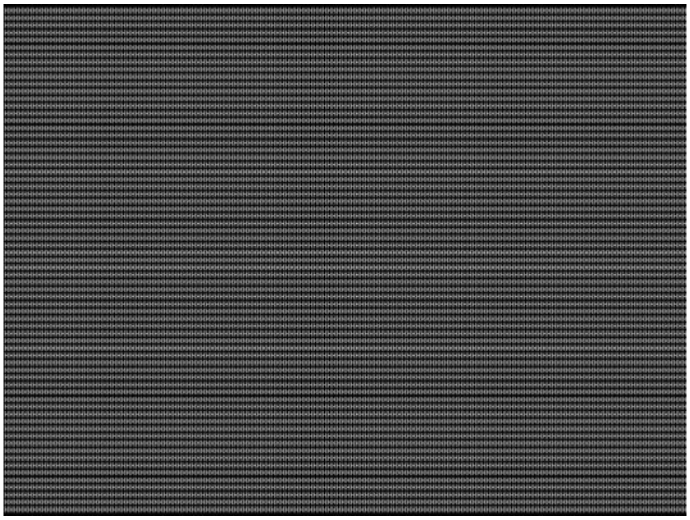
Special test image developed per customer specifications. This image has 19 versions.



16.48 EMITest1 , EMITest3 , EMITest3 , EMITest4 , EMITest5

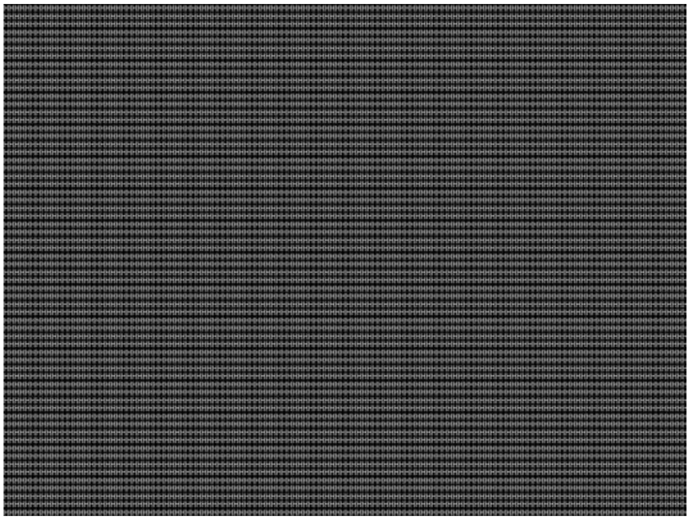
16.48.1Description

Special test images used for electro-magnetic interference (EMI) testing of displays. The entire active video area is filled with an “H” character. The primary versions of these images draw white characters on a black background. The secondary versions draw black characters on a white background. The EMITest1 image is shown below.



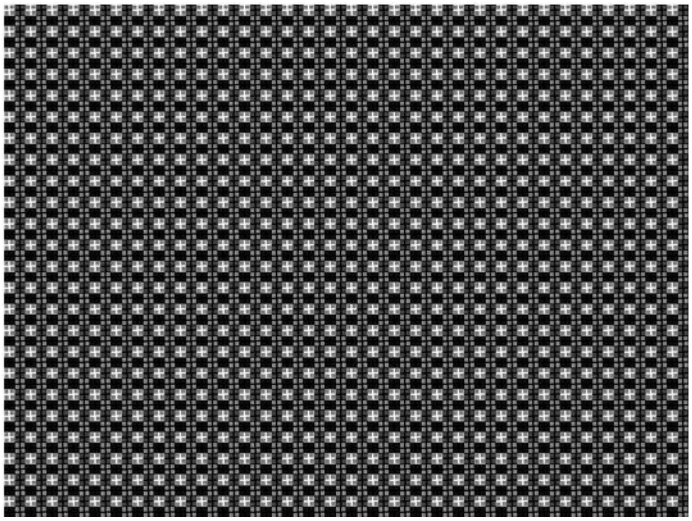
The EMITest2 image is the same as EMITest1, but with the bottom row of characters constantly drawn left-to-right and then cleared.

The EMITest3 image is the same as EMITest1, but with a larger version of the “H” character.



The EMITest4 image is the same as EMITest3, but with the bottom row of characters constantly drawn left-to-right and then cleared.

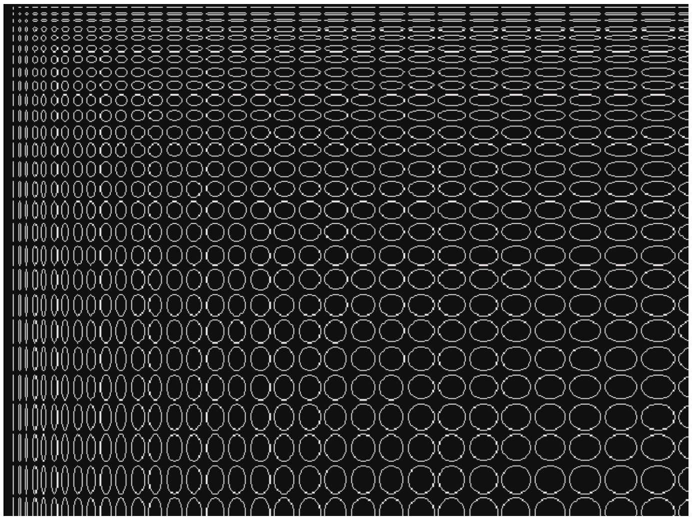
The EMITestS image is shown below.



16.49 Examples

16.49.1Description

Special test images used for electro-magnetic interference (EMI) testing of displays. The entire active video area is filled with an “H” character. The primary versions of these images draw white characters on a black background. The secondary versions draw black characters on a white background. The EMITest1 image is shown below.



16.50 Flat, Flat07, Flat13, Flat20, Flat27, Flat33, Flat40, Flat47, Flat53, Flat60, Flat67, Flat73, Flat80, Flat87, Flat93, FlatGray, Flat_01, Flat_02, Flat_03, Flat_04, Flat_05, Flat_06, Flat_07, Flat_08, Flat_09, Flat_10, Flat_11, Flat_12, Flat_13, Flat_14, Flat_15, Flat_16

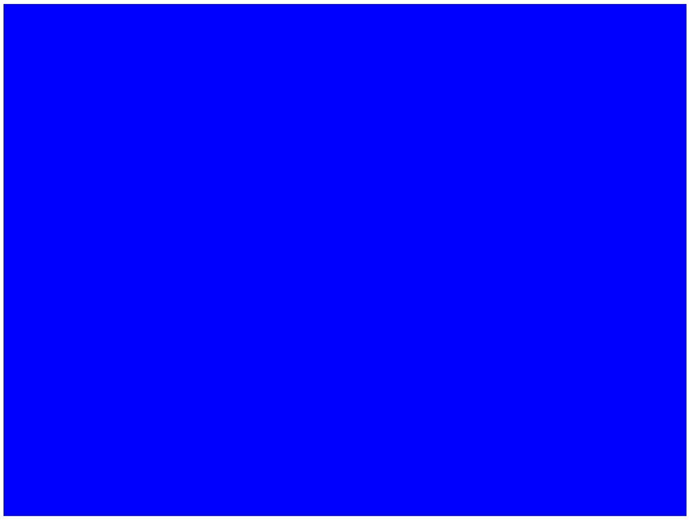
16.50.1 Description

The entire active video area is filled with a shade of gray. Each image displays a different shade of gray. The FlatGray image is shown below.

16.51 Flat_B, Flat_G, Flat_R

16.51.1Description

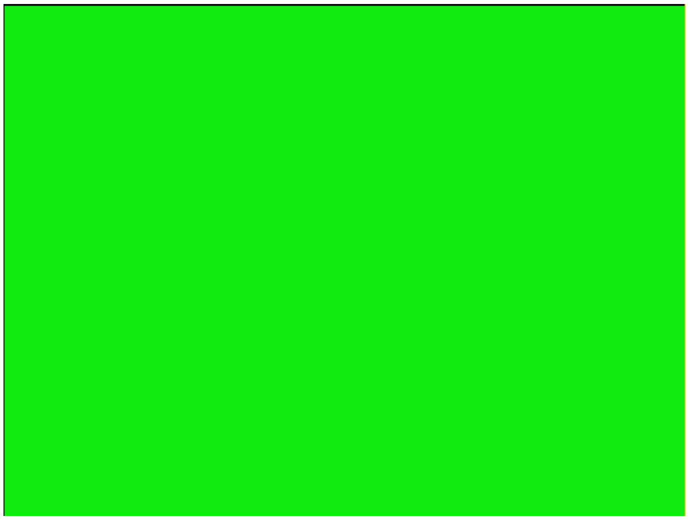
The screen is filled with blue (B), green (G) or red (R). The Flat_B image is shown below.



16.52 FlashRGB

16.52.1Description

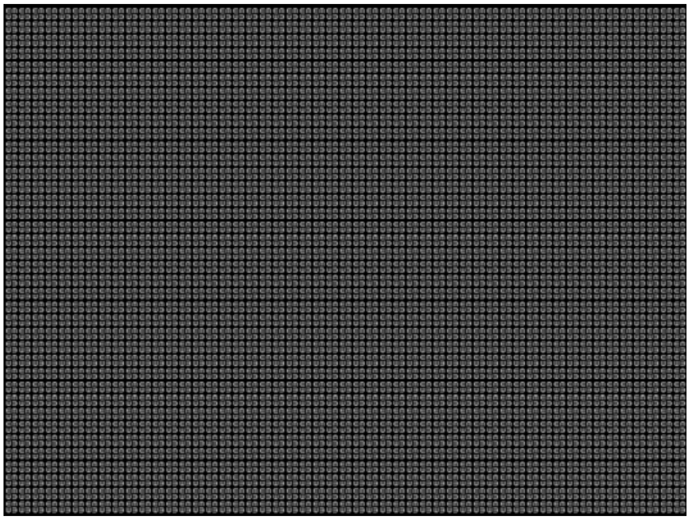
The screen is filled with blue (B), green (G) or red (R).



16.53 Focus20

16.53.1 Description

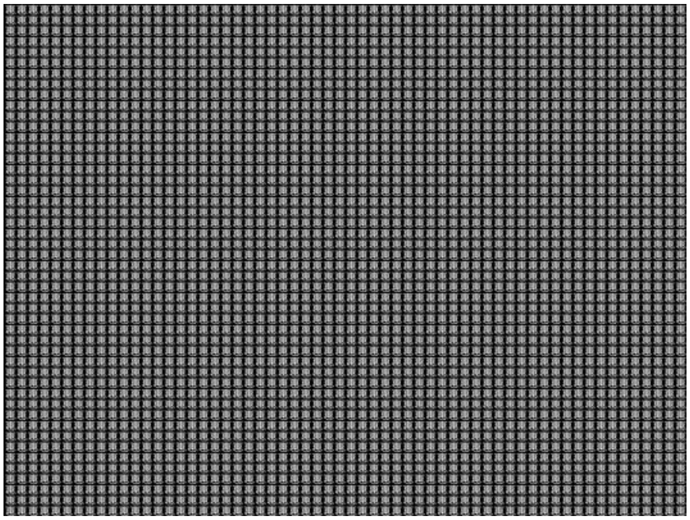
Primary version shown below. The secondary version has black characters on a white background.



16.54 FocusC14

16.54.1Description

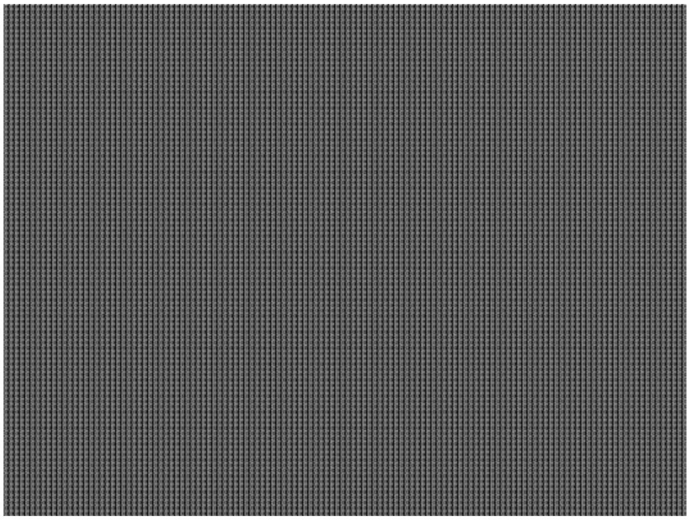
Primary version shown below. The secondary version has black characters on a white background.



16.55 FocusCCx

16.55.1 Description

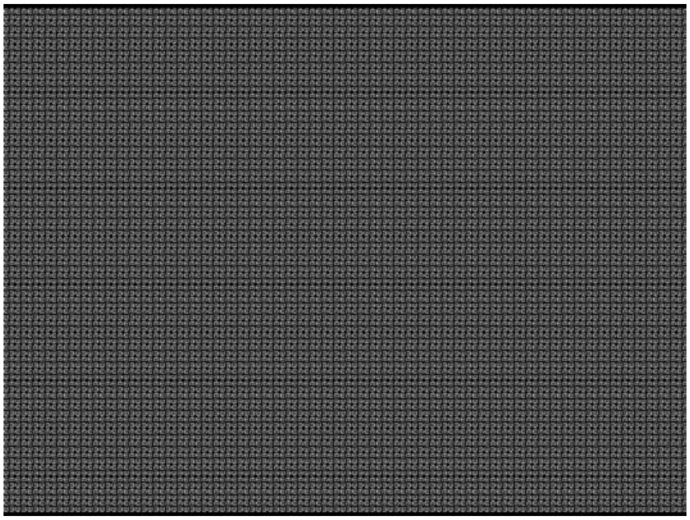
Primary version shown below. The secondary version has black characters on a white background.



16.56 FocusEM

16.56.1Description

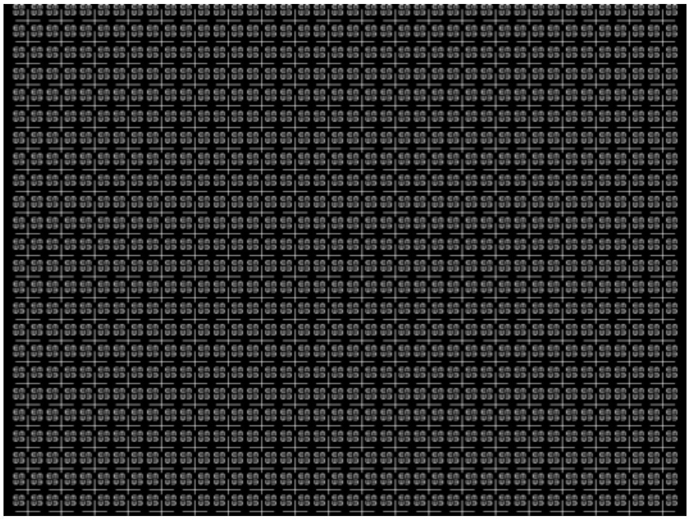
Primary version shown below. The secondary version has black characters on a white background.



16.57 FocusEMP

16.57.1Description

Primary version shown below. The secondary version has black characters on a white background.



16.58 FocusM00 - FocusM15

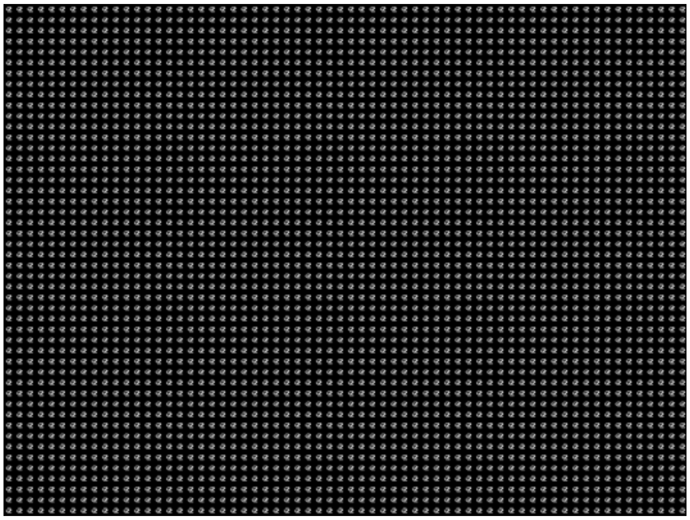
16.58.1 Description

The FocusM00 image is shown below.

16.59 Focus_@6, Focus_@7, Focus_@8, Focus_@

16.59.1Description

In the primary versions, the screen is filled with white “@” characters on a black background. The secondary versions are drawn with black characters on a white background. The primary version of the Focus_@6 image is shown below.



16.59.2Test

Focus adjustments.

16.59.3Purpose

An out-of-focus monitor displays fuzzy graphic images and poorly formed, hard-to-read text characters.

16.59.4Method

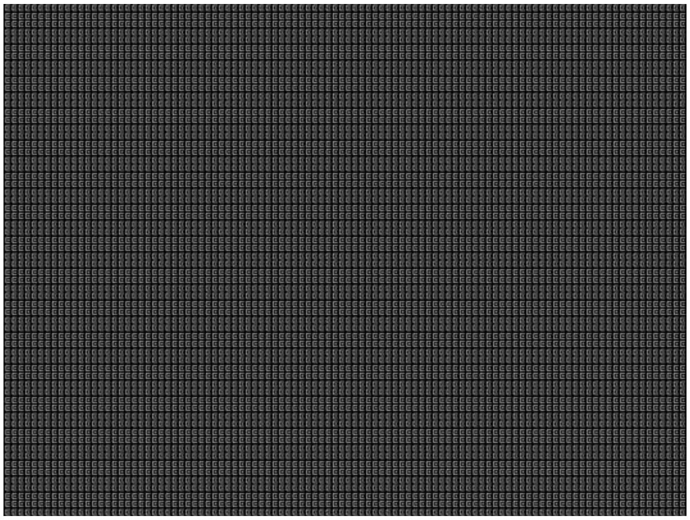
On monitors with a single (static) focus adjustment, adjust the control for the best average focus over the entire screen. The focus at certain locations of the screen should be within specified limits.

Some monitors have a static and one or more dynamic focus controls. The sequence for adjusting them and the areas of the screen that they affect depend on the monitor under test.

16.60 Focus_Cx

16.60.1Description

In the primary version (shown below), the screen is filled with white Cx characters on a black background. The secondary version is drawn with black characters on a white background.



16.60.2Test

Focus adjustments.

16.60.3Purpose

An out-of-focus monitor displays fuzzy graphic images and poorly formed, hard-to-read text characters.

16.60.4Method

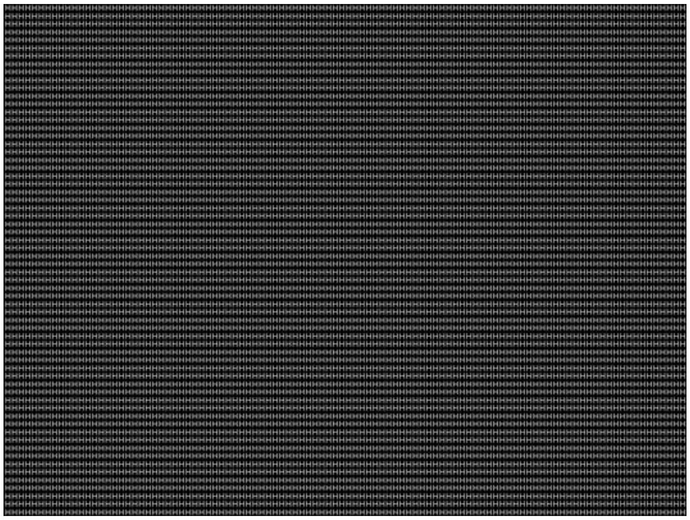
On monitors with a single (static) focus adjustment, adjust the control for the best average focus over the entire screen. The focus at certain locations of the screen should be within specified limits.

Some monitors have a static and one or more dynamic focus controls. The sequence for adjusting them and the areas of the screen that they affect depend on the monitor under test.

16.61 Focus_H

16.61.1Description

In the primary version (shown below), the screen is filled with white H characters on a black background. The secondary version is drawn with black characters on a white background.



16.61.2Test

Focus adjustments.

16.61.3Purpose

An out-of-focus monitor displays fuzzy graphic images and poorly formed, hard-to-read text characters.

16.61.4Method

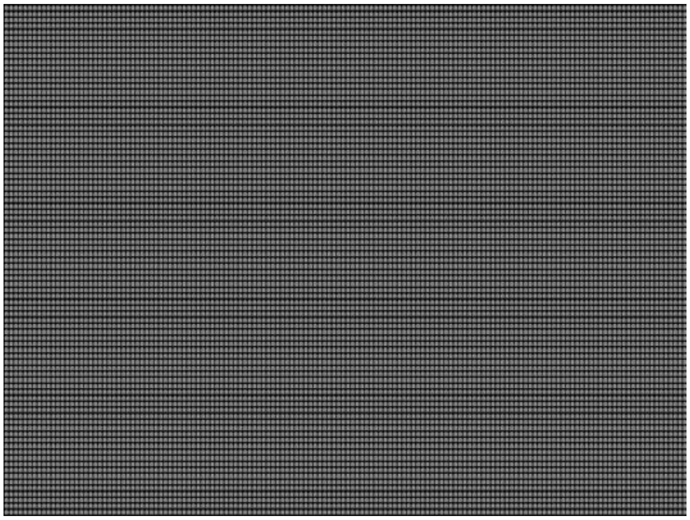
On monitors with a single (static) focus adjustment, adjust the control for the best average focus over the entire screen. The focus at certain locations of the screen should be within specified limits.

Some monitors have a static and one or more dynamic focus controls. The sequence for adjusting them and the areas of the screen that they affect depend on the monitor under test.

16.62 Focus_MM

16.62.1Description

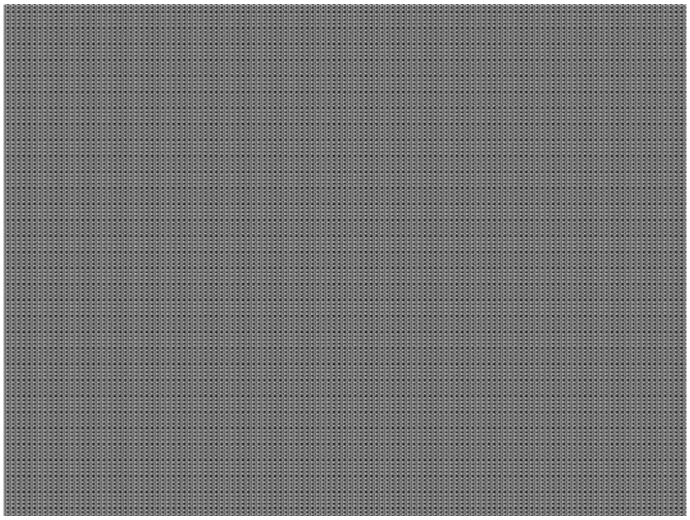
In the primary version (shown below), the screen is filled with white M characters on a black background. The secondary version is drawn with black characters on a white background.



16.63 Focus_Oo

16.63.1Description

In the primary version (shown below), the screen is filled with white Oo characters on a black background. The secondary version is drawn with black characters on a white background.



16.63.2Test

Focus adjustments.

16.63.3Purpose

An out-of-focus monitor displays fuzzy graphic images and poorly formed, hard-to-read text characters.

16.63.4Method

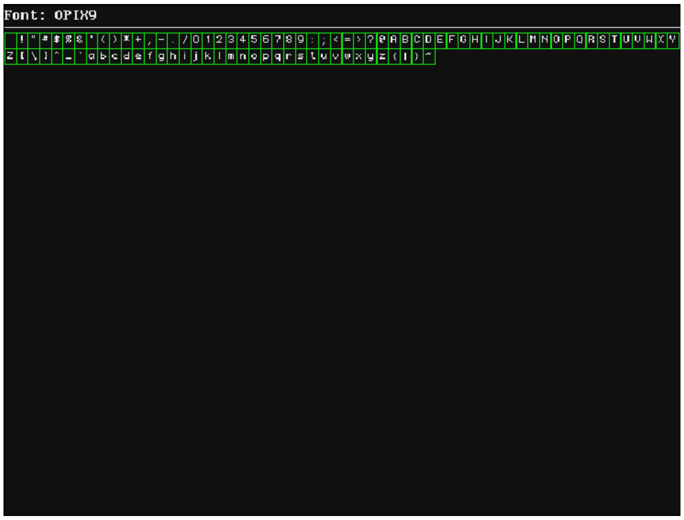
On monitors with a single (static) focus adjustment, adjust the control for the best average focus over the entire screen. The focus at certain locations of the screen should be within specified limits.

Some monitors have a static and one or more dynamic focus controls. The sequence for adjusting them and the areas of the screen that they affect depend on the monitor under test.

16.64 FontViewer

16.64.1Description

A listing of the data contained in any format. The primary image lists the settings of the format driving the display. The secondary image can be used to list the contents of any stored format (via the Location field).

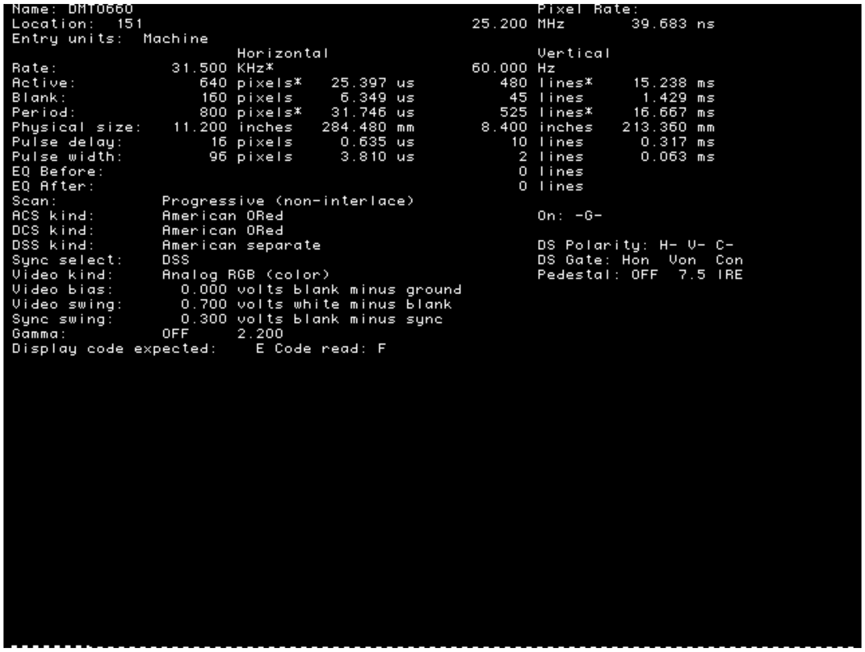


16.65 Format

16.65.1Description

A listing of the data contained in any format. The primary image lists the settings of the format driving the display. The secondary image can be used to list the contents of any stored format (via the Location field).

This pattern works best at display resolutions of at least 640 pixel by 480 lines.

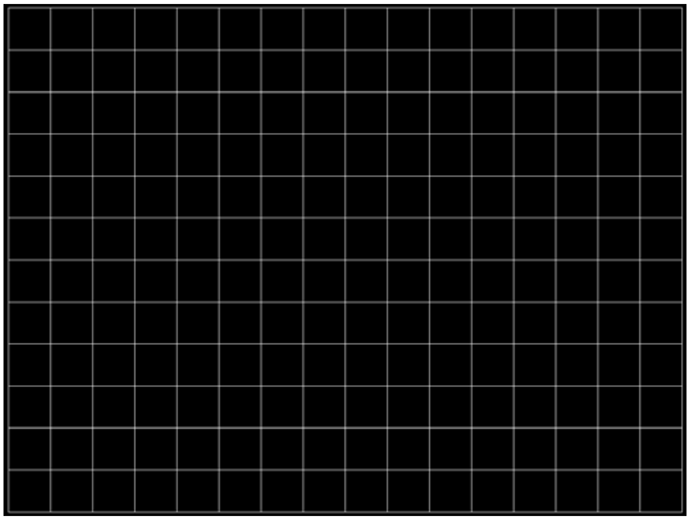


```
Name: DMT0660                                           Pixel Rate:
Location:  151                                   25.200 MHz       39.683 ns
Entry units:  Machine
                        Horizontal                      Vertical
Rate:            31.500 KHz*                     60.000 Hz
Active:             640 pixels*   25.397 us         480 lines*    15.238 ms
Blank:              160 pixels     6.349 us          45 lines      1.429 ms
Period:             800 pixels*   31.746 us         525 lines*    16.667 ms
Physical size:   11.200 inches   284.480 mm       8.400 inches   213.360 mm
Pulse delay:         16 pixels     0.635 us          10 lines      0.317 ms
Pulse width:         96 pixels     3.810 us           2 lines      0.063 ms
EQ Before:                                            0 lines
EQ After:                                             0 lines
Scan:           Progressive (non-interlace)
ACS kind:       American ORed                           On: -G-
DCS kind:       American ORed
DSS kind:       American separate                       DS Polarity: H- V- C-
Sync select:    DSS                                     DS Gate: Hon  Von  Con
Video kind:     Analog RGB (color)                      Pedestal: OFF  7.5 IRE
Video bias:       0.000 volts blank minus ground
Video swing:      0.700 volts white minus blank
Sync swing:       0.300 volts blank minus sync
Gamma:          OFF     2.200
Display code expected:    E Code read: F
```

16.66 Geom_1 – Geom_5

16.66.1Description

The primary version of the Geom_1 image is shown below. Secondary version is drawn with black lines on a white background.



16.67 Gray25, Gray40

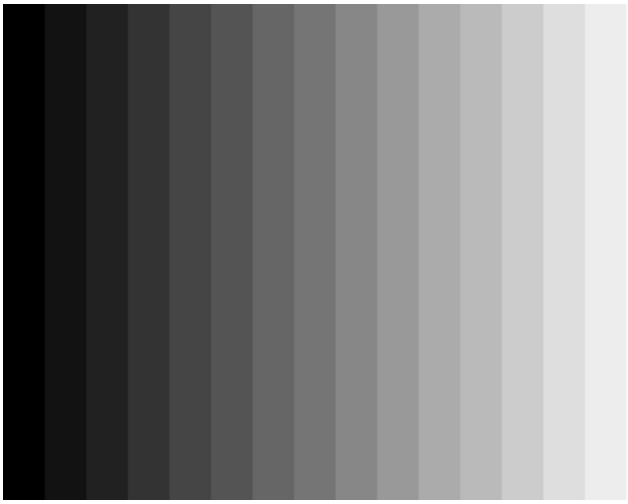
16.67.1 Description

The Gray25 image is shown below.

16.68 GrayBar

16.68.1Description

The primary version (shown below) has 16 full-height vertical graybars. The intensity of the bars is shown below. The secondary version splits the field into a top and bottom half. The bars in the bottom half of the screen are in reverse order.



16.68.2Test

Video color tracking (color monitors)

16.68.3Purpose

To verify that a color monitor accurately reproduces colors at all intensities.

16.68.4Method

Perform the Brightness Control Adjustment and Brightness Uniformity tests first.

Changes in brightness from bar to bar should be uniform. All of the bars should appear as an untinted gray at all levels.

16.68.5Test

Video gain linearity (monochrome monitors)

16.68.6 Purpose

To check the video linearity (grayscale) modulation)

16.68.7Method

Perform the Brightness Control Adjustment and Brightness Uniformity tests first.

Changes in brightness from bar to bar should be visible and uniform.

16.69 GrayL1, GrayL3

16.69.1Description

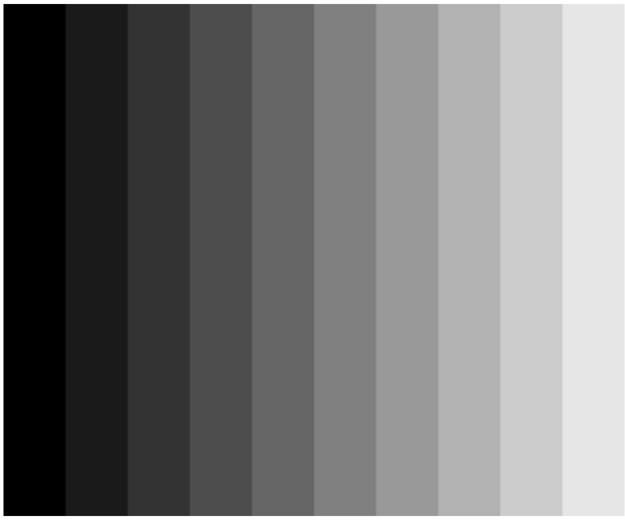
The GrayL1 image is shown below.

16.70 Grays5, Grays9, Grays11, Grays16, Grays32, Grays64

16.70.1Description

These images have the designated number of full-height vertical graybars.

The Grays11 image is shown below.



16.71 GraysAll

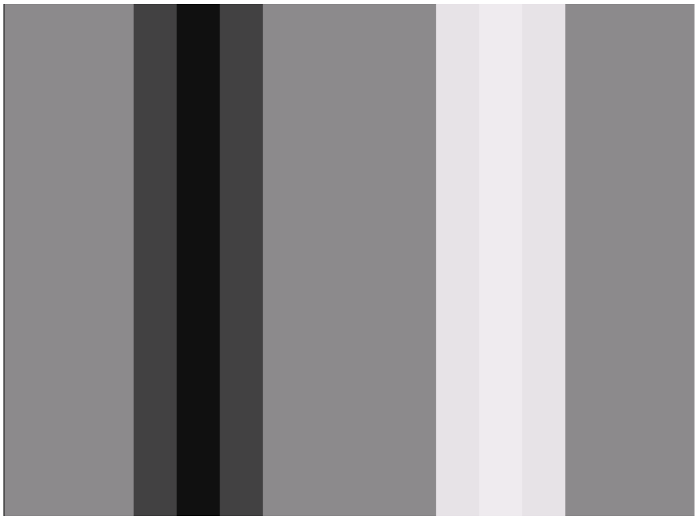
16.71.1Description

Contains 256 grayscale versions, from 0 (full black) to 255 (full white).

16.72 GraysMHL

16.72.1 Description

Contains 256 grayscale versions, from 0 (full black) to 255 (full white).



16.73 Gray_PIC

16.73.1Description

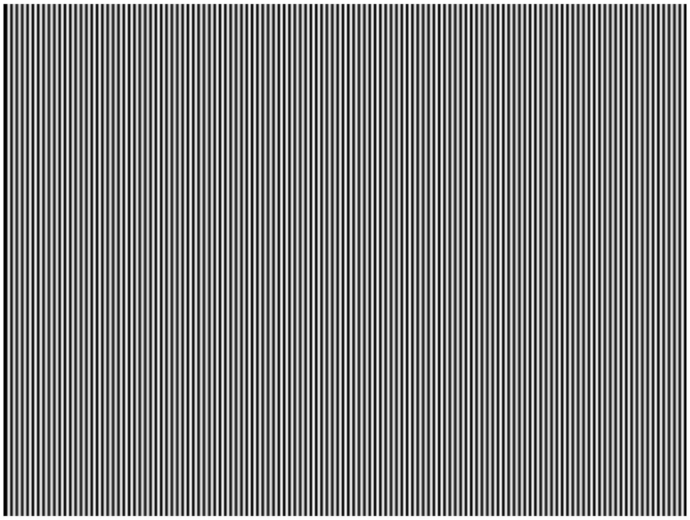
A solid gray box fills the active video area.

16.74 Grill_11, Grill_15, Grill_22, Grill_33, Grill_44

16.74.1Description

The entire active video area is filled with alternating black and white stripes. The stripes are drawn at different resolutions. Each of the stripes is four (4) pixels wide in the Grill_44 image and three (3) pixels wide in the Grill_33 image. Each of the stripes is two (2) pixels wide in the Grill_22 image and one (1) pixel wide in the Grill_11 image.

The primary versions draw vertical stripes. The secondary versions draw horizontal stripes. The primary version of the Grill_44 image is shown below.



16.74.2Test

Verify monitor resolution.

16.74.3Purpose

The resolution of your monitor should meet or exceed the design specifications.

16.74.4Method

First adjust the brightness, contrast, and focus to their correct settings. You should be able to see individual and distinct stripes in all areas of the display at all four resolutions. Failure to see distinct lines at the highest resolution (Grill_11) may indicate you have a defective video amplifier or picture tube.

Note: *If multi-colored lines appear on a mask-type color picture tube, you may have a problem with convergence or you may be exceeding the resolution of the picture tube.*

16.75 GRN_EM, GRM_EM+, GRN_HTCH, GRN_PIC

16.75.1Description

In the primary version, the screen is filled with green (GRN) character blocks on a black background. Only the white character has a secondary version. It is drawn with black characters on a white background.

16.76 H_Stair

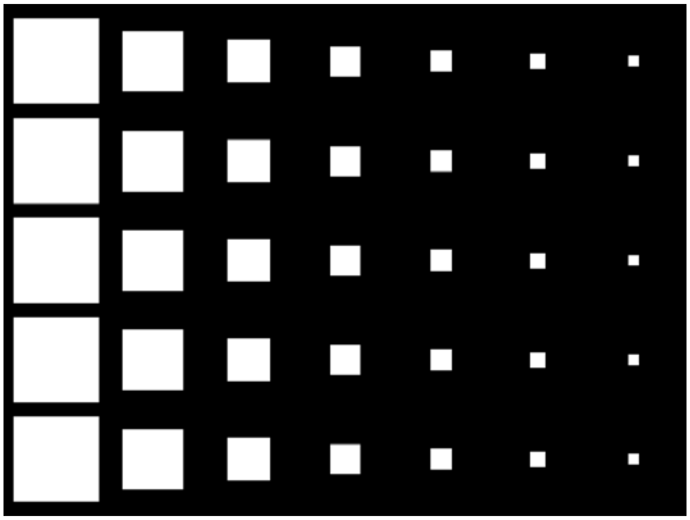
16.76.1Description

The active video area goes from full black at the bottom edge of the screen to full white at the top edge.

16.77 HalfArea

16.77.1Description

Primary version shown below. Secondary version is drawn with black boxes and white background.



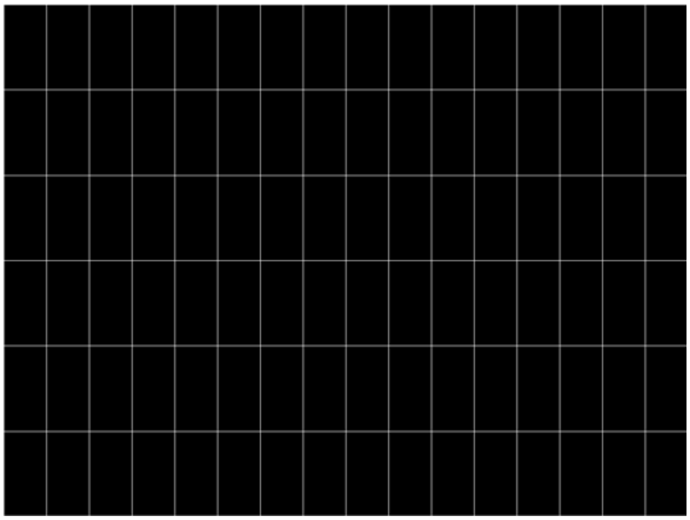
16.78 HalfClk

16.78.1Description

16.79 Hat1606, Hat1610, Hat1612, Hat1615

16.79.1Description

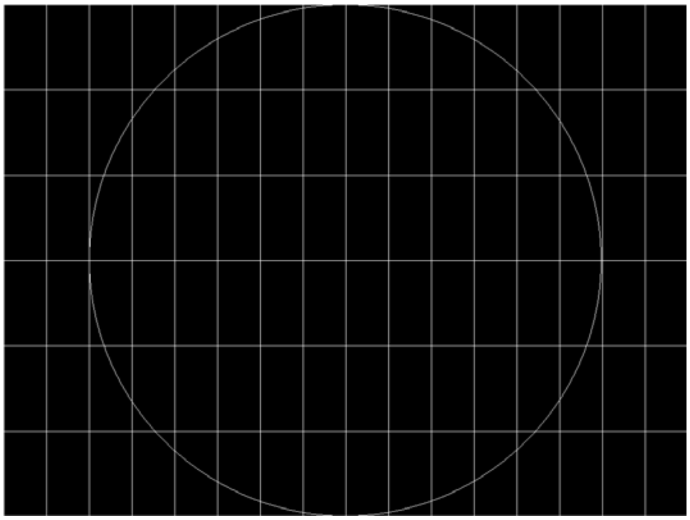
Primary version of Hat1606 is shown below. Secondary version is inversed.



16.80 Hat1606A, Hat1610A, Hat1612A, Hat1615A

16.80.1Description

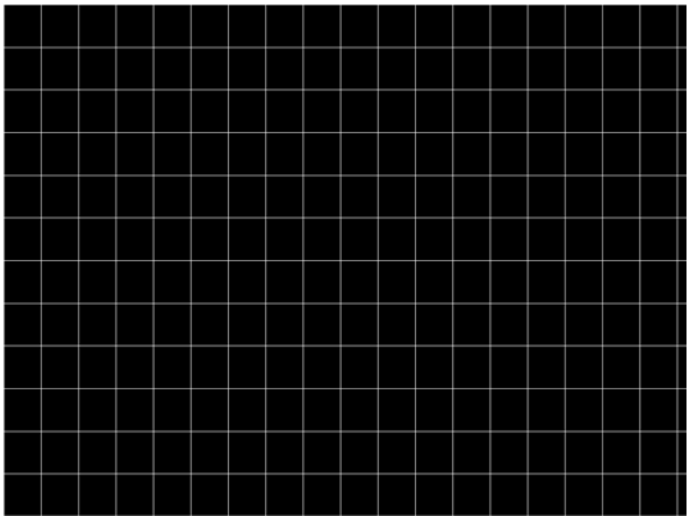
Primary version of Hat1606A is shown below. Secondary version is inversed.



16.81 Hat1812, Hat1815

16.81.1Description

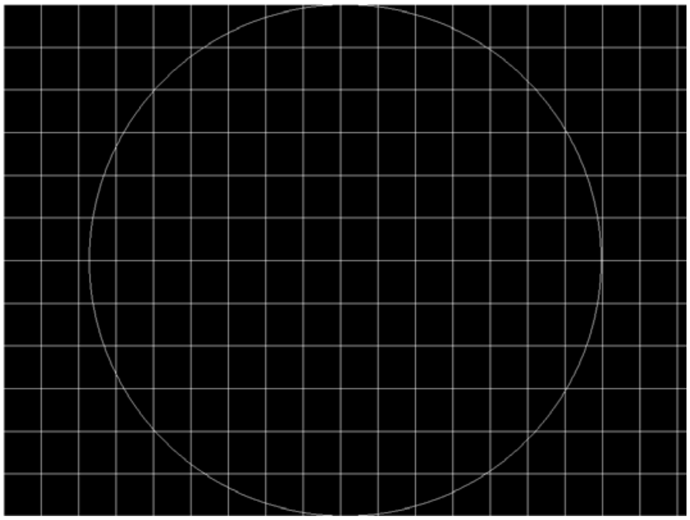
Primary version of Hat1812 is shown below. Secondary version is inversed.



16.82 Hat1812A, Hat1815A

16.82.1Description

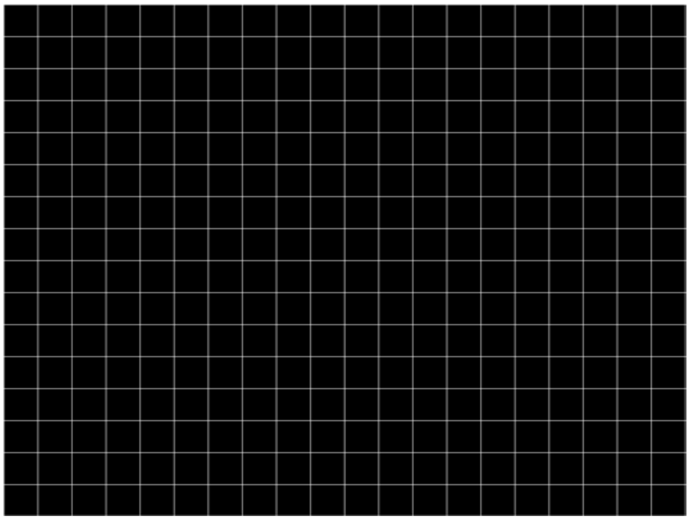
Primary version of Hat1812A is shown below. Secondary version is inversed.



16.83 Hat2016

16.83.1Description

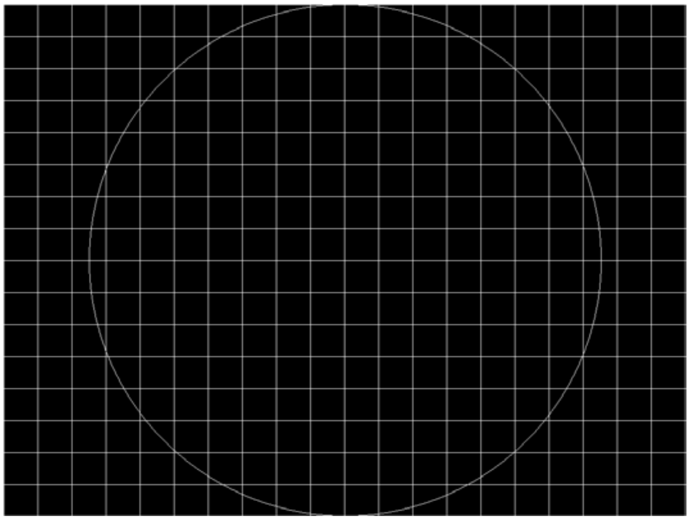
Primary version is shown below. Secondary version is inversed.



16.84 Hat2016A

16.84.1 Description

Primary version is shown below. Secondary version is inversed.



16.85 Hatch_6, Hatch_10i, Hatch_10o, Hatch_12i, Hatch_12o, Hatch_24i, Hatch_24o, Hatch_24s, Hatch_G, Hatch_M, GRN_HTCH, and MAGENTA

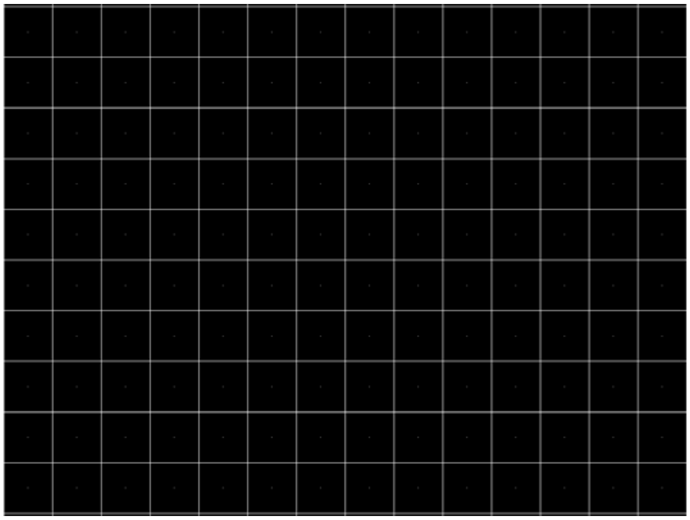
16.85.1Description

The primary versions consist of a white, green (G and GRN), or magenta (M) crosshatch drawn on a black background. The lines form square boxes. A single pixel dot is located in the center of each crosshatch box. The number of boxes formed depends on the version of the image selected and the screen aspect ratio of the currently loaded format. The number in the image's name refers to the number of boxes that are formed along the minor axis for most aspect ratios. The generator calculates the ratio and then finds the closest match from the table on the next page. Version names indicate the drawing method, as follows:

- Versions ending in "i" draw from the inside (center) out. Any partial boxes are placed around the perimeter of the image.
- Versions ending in "o" draw from the outside in. Any partial boxes are placed along the centerlines of the image.
- Versions ending in "s" are the "i" version plus a 1-pixel thick border.

The secondary versions invert the images to black lines and dots on a white background. Hatch_G, Hatch_M, GRN_HTCH and Magenta do not have secondary versions.

The primary version of the Hatch_10i image is shown below.



Aspect Ratio		**Dot_10**		**Dot_12**		**Dot_24**	
W : H	Decimal	Boxes Vertically	Boxes Horizontally	Boxes Vertically	Boxes Horizontally	Boxes Vertically	Boxes Horizontally
16 : 9	1.777 É	10	16	10	16	18	32
5 : 3	1.666 É	10	16	10	16	18	30
4 : 3	1.333 É	10	14	12	16	24	32
1 : 1	1.000	10	10	12	12	24	24

3 : 4	0.750	14	10	16	12	32	24

16.85.2Test

Convergence adjustment (color monitors only).

16.85.3Purpose

To accurately produce an image on a color monitor, the three electron beams in the CRT must meet (converge) at the same location at the same time. Lines displayed on a misconverged monitor appear as several multi-colored lines, and the transitions between different colored areas contain fringes of other colors.

16.85.4Method

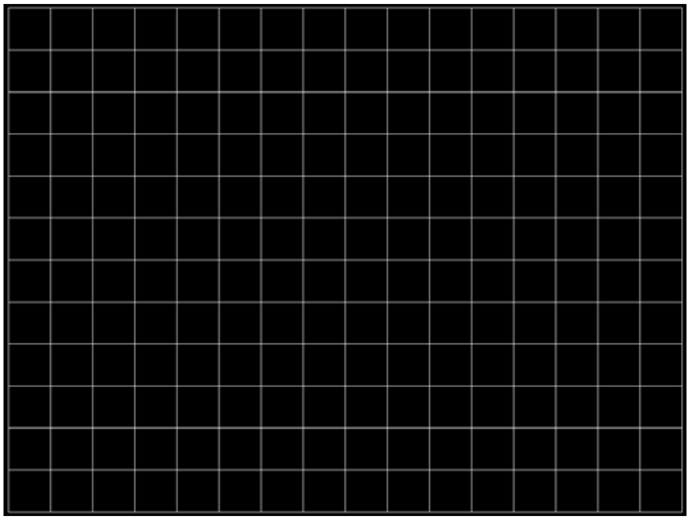
The convergence adjustments of most color monitors fall into two main categories. The first set of adjustments, usually called Static Convergence, aligns the three beams in the center of the display. This method involves turning on all three guns and adjusting the various magnets on the convergence assembly to produce all white dots in the center of the display. The convergence assembly is located on the neck of the CRT. Different monitors and CRT types may each require their own magnet adjustment sequence.

After the center of the display is properly converged, the outer areas are adjusted by using the monitor’s Dynamic Convergence controls. The number of controls, the area of the screen they affect, and their adjustment procedure depends on the monitor under test.

16.86 Hatch_16, Hatch_20

16.86.1Description

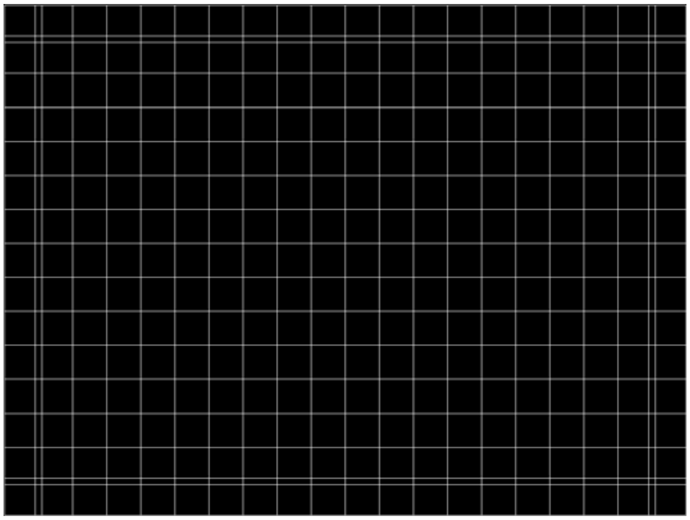
The primary version of the Hatch_16 image is shown below. The secondary versions draw black lines on a white background.



16.87 Hatch20

16.87.1 Description

Primary version shown. The secondary version draws black lines on a white background.

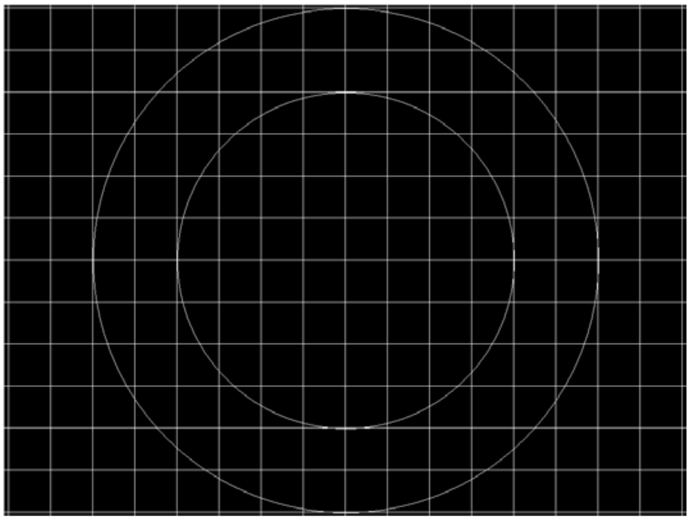


16.88 Hatch4x3, Hatch5x4 and Hatch8x8

16.88.1Description

These are different versions of a crosshatch pattern that may be called for by some display manufacturers' test procedures. The primary version consists of white crosshatch and circles on a black background. The secondary version inverts the image to black lines on a white background.

The primary version of the Hatch4x3 image is shown below.



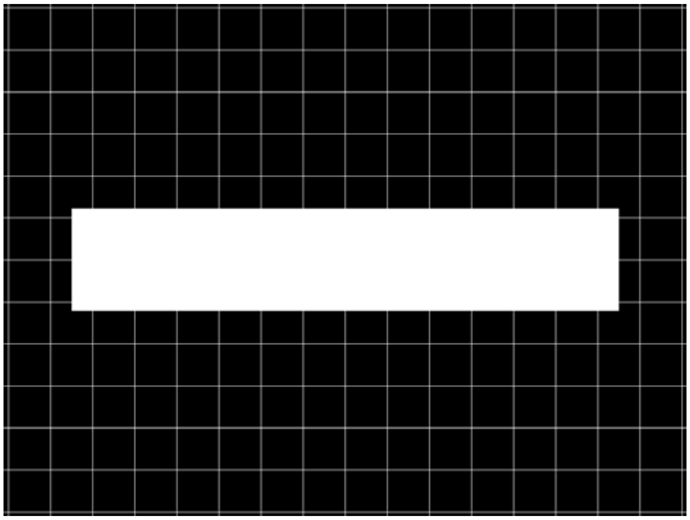
16.88.2Purpose

This is a general purpose test image that can be used to check and adjust video scan linearity and geometry and color convergence.

16.89 Hatch64W

16.89.1Description

This is a crosshatch pattern that may be called for by some manufacturers’ test procedures. The primary version (shown below) consists of an 8x8 white crosshatch on a black background. A white rectangular patch is added in the center. The secondary version inverts the image to black lines and box on a white background.



16.89.2Purpose

Method This is a general purpose test image that can be used to check and adjust video scan linearity and geometry, and color convergence. The large white rectangle also allows for checking a display’s high voltage regulation. This is done by observing the vertical lines at the left and right edges of the image. They should be fairly straight and not pull in the area of the white rectangle.

16.90 HdcpProd, Hdcp2

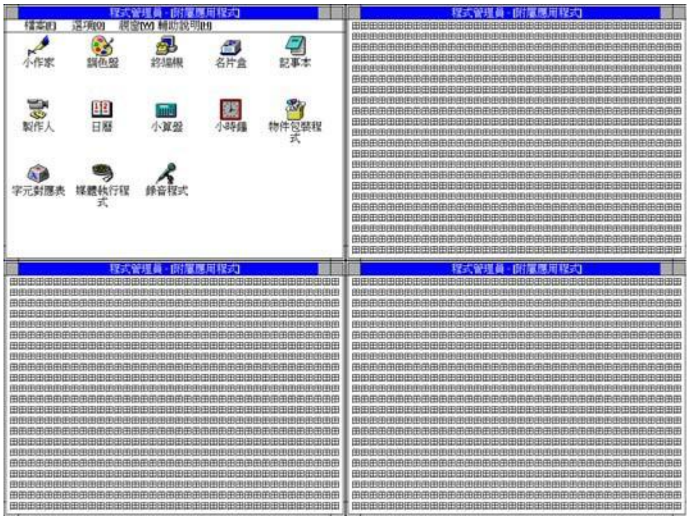
16.90.1Description

Used with HDCP feature.

16.91 Hitatchi

16.91.1Description

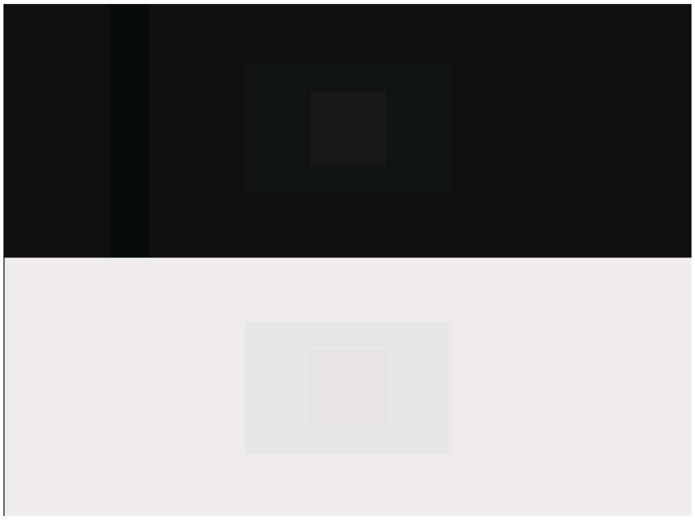
Special test image developed per customer specifications. The image consists of a 2x2 cluster of Microsoft Windows® screen simulations using Japanese characters.



16.92 HiLoTrk

16.92.1Description

The image consists of the middle of the 100-percent-white bottom portion is a 97.5-percent-white box within a larger 95-percent-white box.

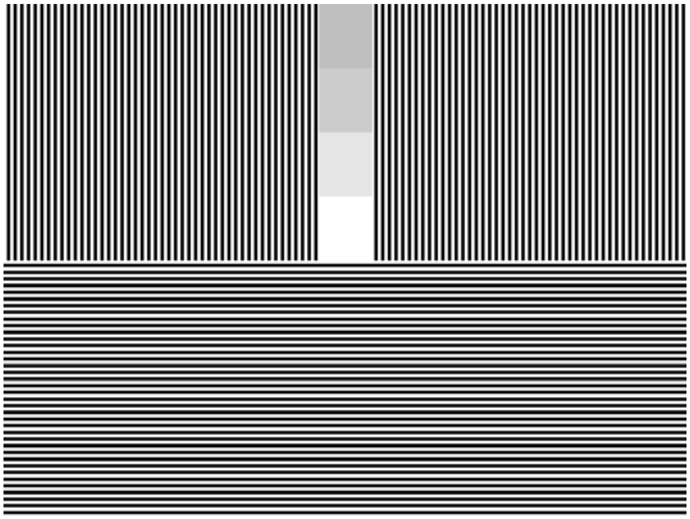


16.93 HSVnRGB

16.93.1Description

16.94 Imex1

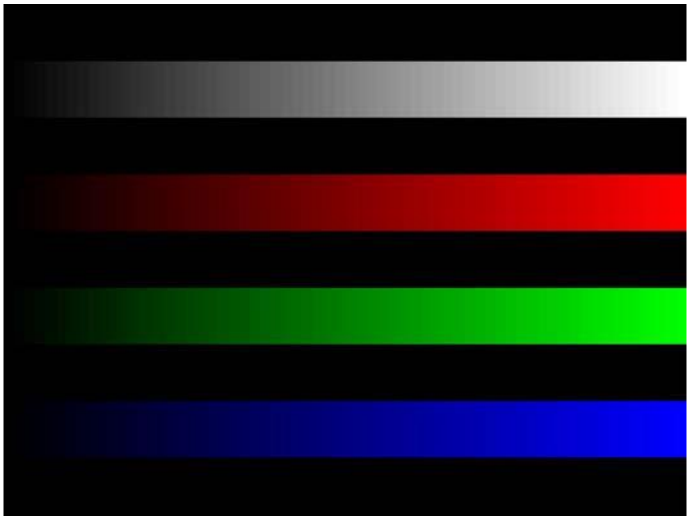
16.94.1Description



16.95 InFocus1

16.95.1Description

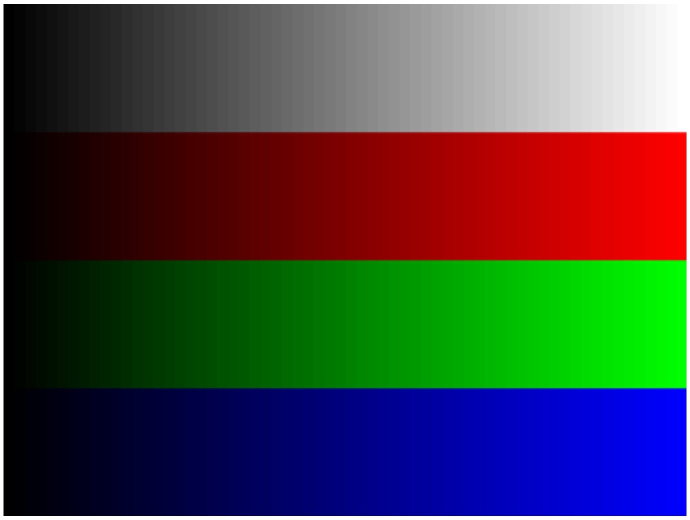
Special test image developed per customer specifications.



16.96 InFocus2

16.96.1Description

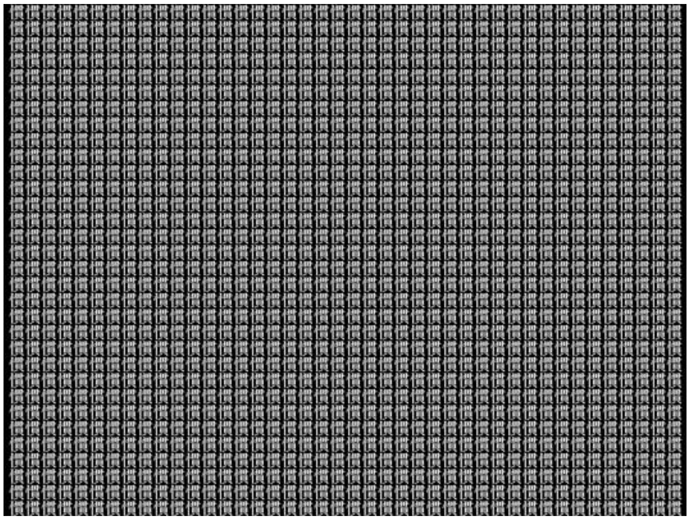
Special test image developed per customer specifications.



16.97 KanjiKAN

16.97.1Description

In the primary version (shown below), the screen is filled with white Japanese Kan characters on a black background. The secondary version is drawn with black characters on a white background.



16.97.2Test

Focus adjustments.

16.98 L80

16.98.1Description

Special test image developed per customer specifications. Each image has three versions. The primary version of the LGLCDTVB image is shown below.

16.99 LGLCDTVB, LGLCDTVG, LGLCDTVR, LGLCDTVW

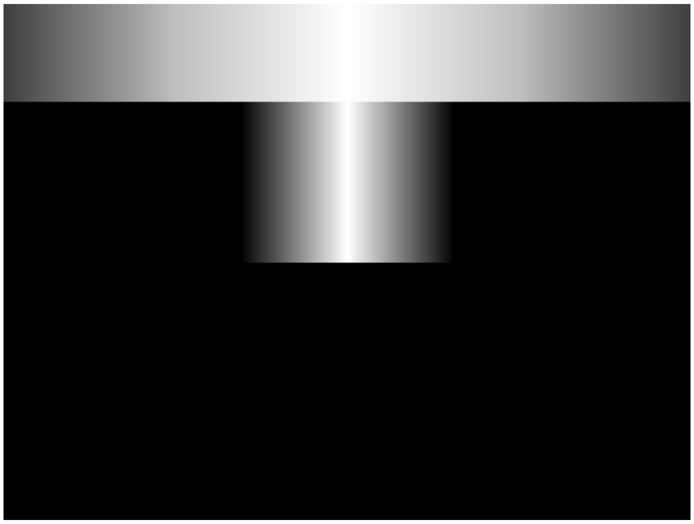
16.99.1Description

Special test image developed per customer specifications. Each image has three versions. The primary version of the LGLCDTVB image is shown below.

16.100 LGRamp

16.100.1 Description

Special test image developed per customer specifications. The image provides a grayscale of two objects. The secondary version of the LGRamp image is shown below.



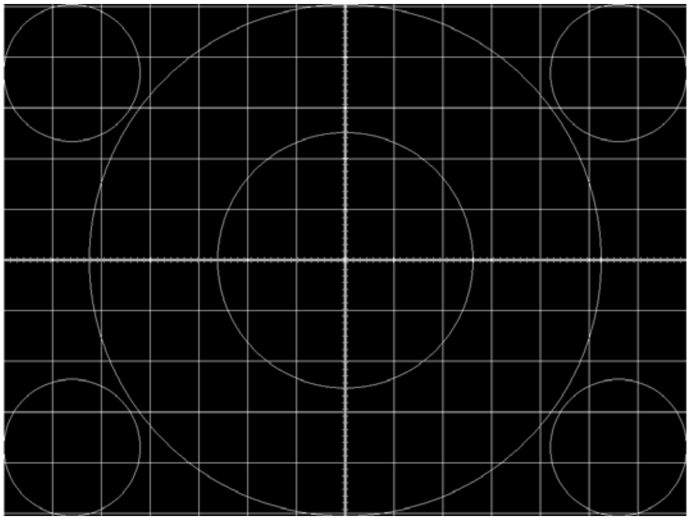
16.101 Linearty (Linearity)

16.101.1 Description

This image has three parts. The first part consists of six (6) white circles. A large circle is drawn in the center of the screen. Its diameter equals the lesser of the video height or width of the display. A smaller circle is drawn at half the diameter and concentric with the larger circle. A circle also is drawn in each of the corners of the screen. The diameter of the corner circles equals one-fifth of the display width.

The second part of the image consists of a white crosshatch. The number of boxes in the crosshatch depends on the physical size of the display.

The last part of the image consists of white tic marks on the horizontal and vertical center lines of the image. The marks are one pixel thick at every other pixel location. Every fifth mark is slightly longer. The color of the pattern can be changed with the individual video output controls.



16.101.2 Test

Linearity adjustment.

16.101.3 Purpose

To present an undistorted display, the horizontal and vertical sweeps of the electron beam across the face of the CRT should be at uniform speeds. Any non-uniformity in the sweep causes portions of an image to stretch while other portions are compressed. Non-linearity in a monitor shows up in several ways. It may be present across the entire screen, in a large portion of the screen, or localized in a very small area.

16.101.4 Method

The circles in the image can be used to do a general adjustment of a monitor's linearity controls. Adjust the controls to form perfectly round circles. The crosshatch image can be used to measure linearity and to make finer control adjustments. All the full boxes in the crosshatch should be identical in size. Measure them with a ruler or a gauge made for the monitor under test. Any deviation should be within your specification limits. Use the tic marks and a ruler or gauge to measure linearity over a small portion of the display. Compare the number of tic marks per unit of measure with an adjacent or overlapping area.

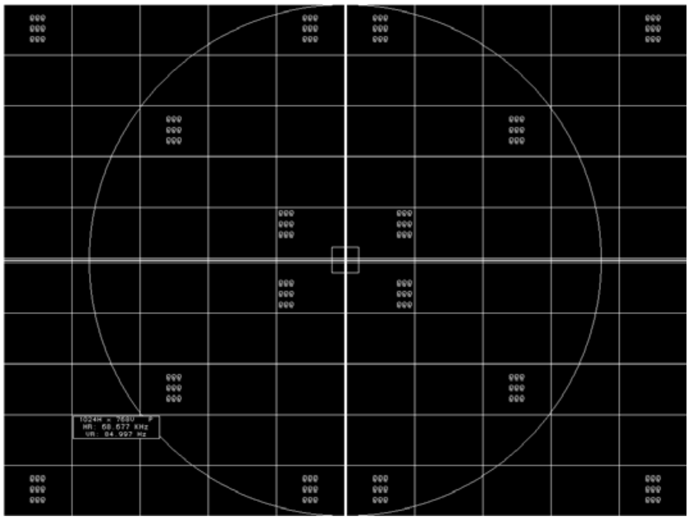
16.102 LinFocus

16.102.1 Description

This image has several parts. The first part consists of a large circle in the center of the screen. Its diameter equals the lesser of the video height or width of the display.

The second part is a 10x10 box crosshatch. The crosshatch is drawn in from the outside edges, with any extra pixels in the boxes placed along the vertical and horizontal axis. The vertical centerline is two pixels thick if the format has an even number of active pixels per line. The horizontal centerline is two pixels thick if the format has an even number of active lines per frame. A smaller box is added at the center of the image. The box is one-half the height and two-fifths the width of one of the crosshatch boxes. Current format data is shown in the lower left quadrant of the image. It shows the number of active pixels (H) and lines (V) as well as the vertical and horizontal scan rates.

The primary version (shown below) consists of a white pattern on a black background. The secondary version has a black pattern on a white background.



The image also includes blocks of focus-checking characters at various locations. The blocks are positioned inside the crosshatch boxes and are up to 3x3 characters in size. The size of the blocks is limited by the number of characters that can fit in one box.

16.102.2 Test

Linearity adjustment

16.102.3 Test

Focus adjustment.

16.102.4 Purpose

An out-of-focus monitor displays fuzzy graphic images and poorly formed, hard-to-read characters when text is displayed on the screen.

16.102.5 Method

On monitors with a single (static) focus adjustment, adjust the control for the best average focus over the entire screen. The focus at certain locations of the screen should be within specified limits.

Some monitors have a static and one or more dynamic focus controls. The sequence for adjusting them and the areas of the screen they affect depend on the monitor under test.

16.103 LipSync, LipSyncB

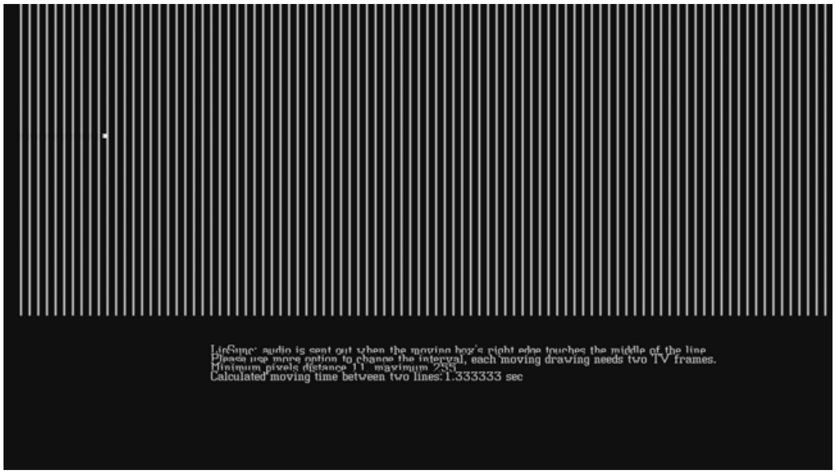
16.103.1 Description

The lipsync image enables you to test for synchronization between HDMI video and audio.

The image enables you to select between a range of intervals. You can access the subimages to control the interval of each video/audio synchronization event through the Content->Options menu and incrementing with the +/- keys. There are 255 distinct settings (different intervals) available.

When you first select the Lipsync image, the interval is set at 0.66733 sec per audio event (shown below) for progressive formats and 1.333333 sec for interlaced formats. When you enable subimages with Content->Option, the default inital screen at image rendition 0 is one sync event per 1.101100 sec for progressive formats and 2.2 sec for interlaced formats. You can increase this up to 8.475133 sec at image rendition 254 which is one video/audio synchronization event per 8.46666 seconds for progressive formats and

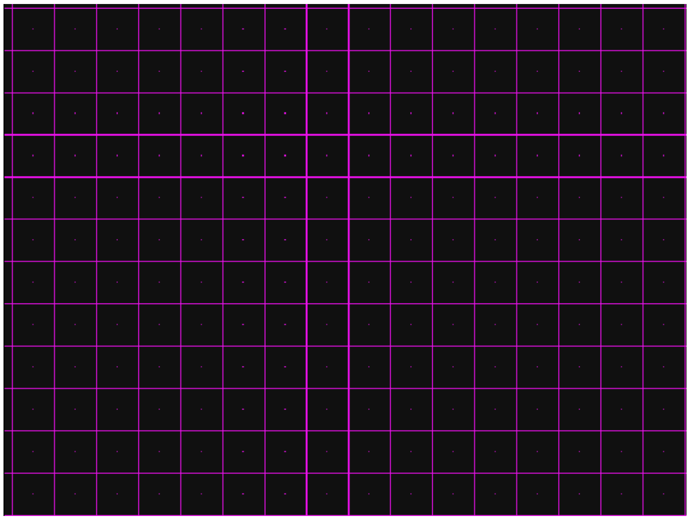
16.933332 for interlaced formats.



LipSync: audio is sent out when the moving box's right edge touches the middle of the line
Please use more option to change the interval, each moving drawing needs two TV frames.
Minimum pixels distance 11, maximum 255
Calculated moving time between two lines:1.333333 sec

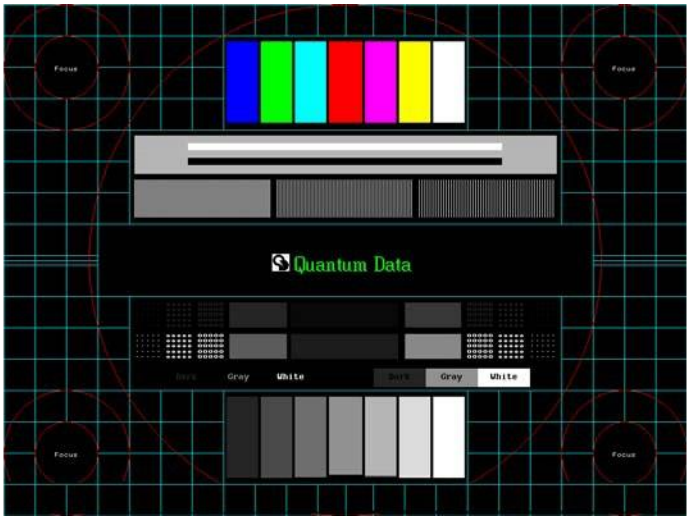
16.104 MAGENTA

16.104.1 Description



16.105 Master

16.105.1 Description

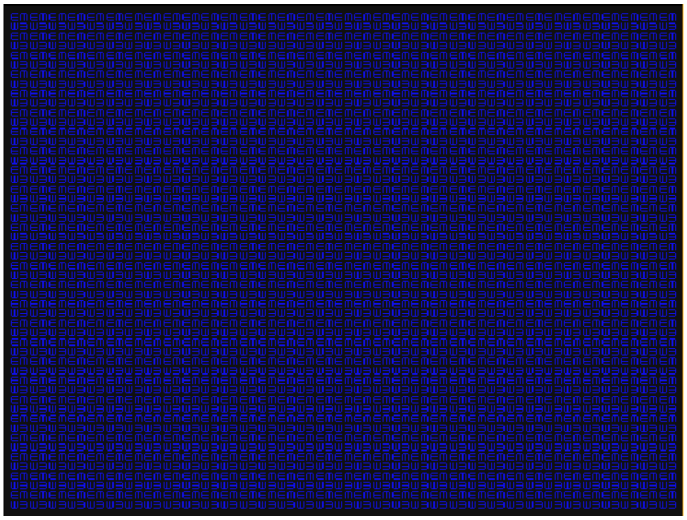


16.106 MESony_R, MESony_G, MESony_B,

16.106.1 Description

In the primary version, the screen is filled with blue (B), green (G), red (R) EM character blocks on a black background. Only the white character has a secondary version. It is drawn with black characters on a white background.

A bitmap of a single character block is shown here. The MESony_B image is shown below.

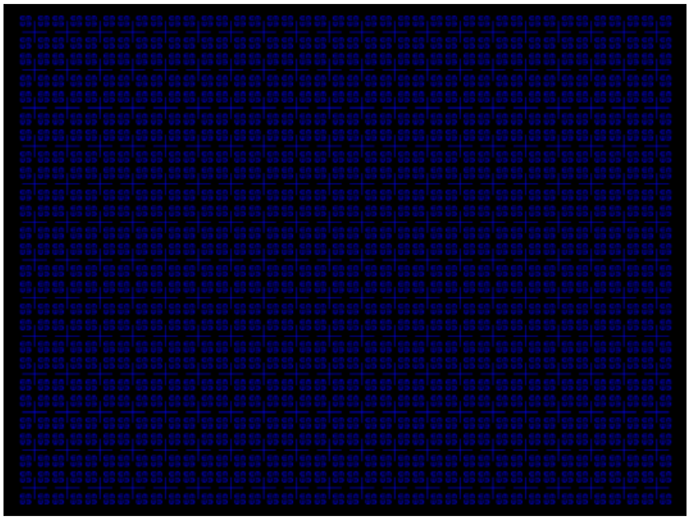


16.107 MEMEPlus, MEPlus_B, MEPlus_G, and MEPlus_R

16.107.1 Description

In the primary version, the screen is filled with blue (BLU and B), green (GRN and G), red (R), or white (WHT and Sony) EM character blocks on a black background. Only the white character has a secondary version. It is drawn with black characters on a white background.

A bitmap of a single character block is shown here. The BLU_EM+ image is shown below.



16.107.2 Test

Focus.

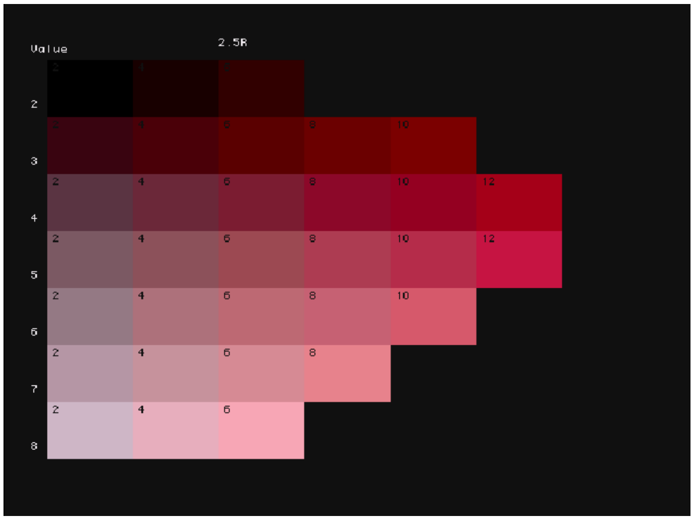
16.107.3 Purpose

This pattern is specified by one or more display manufacturers for checking and adjusting focus one color at a time.

16.108 MnslCLR

16.108.1 Description

There are a series of these images (40 in total) that are accessible as sub images through the 882E front panel. Each hue in the MnslCLR image set has 4 sub hues, labeled 2.5, 5, 7.5 and 10, that represent a hue as it traverses around the perimeter of the diagram above and transitions into the adjacent hues. Each such sub image depicts the chroma and value variances of one of these sub hues. Each sub image provides a color block for each chroma and value level for that sub hue. The value varies along the vertical axis and the chroma varies along the horizontal axis.



16.109 MnslGM

16.109.1 Description

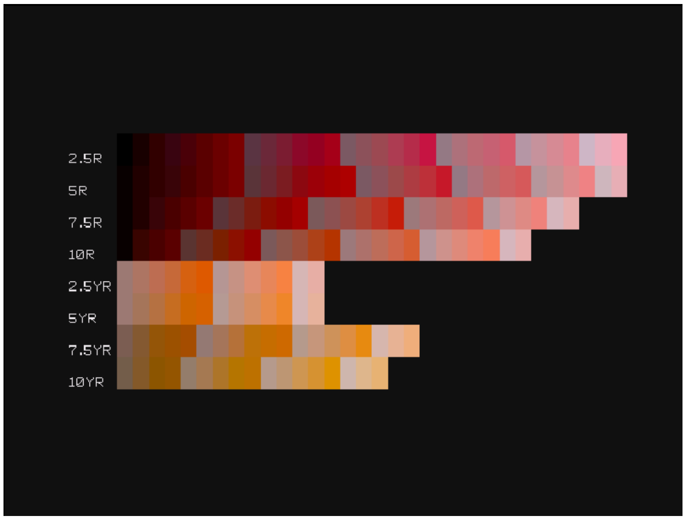
This is a color checker image with 24 colors arranged in a checker board.

16.110 MnslPG

16.110.1 Description

There are a series of these images (5 in total) that are accessible as sub images through the 882E front panel. Each sub image depicts two hue families (each hue family contains 4 sub hues (2.5, 5, 7.5, 10). Each set of color blocks arranged along a horizontal axis depicts the chroma and value variations for one of the sub hues which is labeled on the left. Each such horizontal set of color blocks is a cancatenation of the value and chroma variations for that particular hue. These cancatenations can be derived from the MnslCLR images. In other words, the MnslPG image is a concatenation of 8 of the MnslCLR images.

The MnslPG Image is shown below.

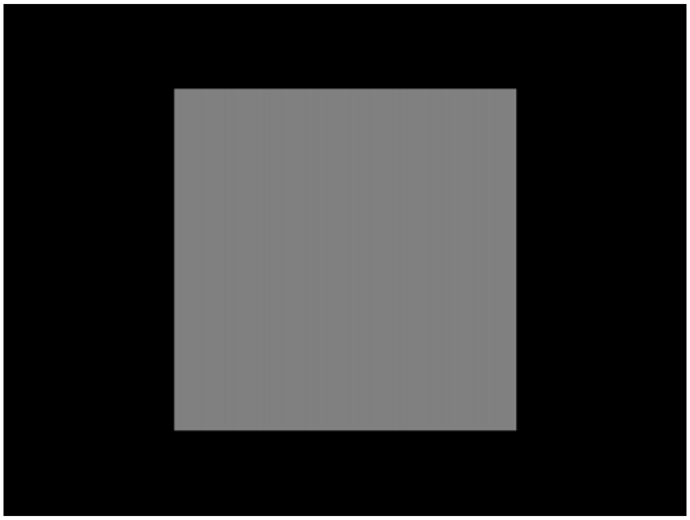


16.111 MoireX, MoireX33, MoireY, MoireY33

16.111.1 Description

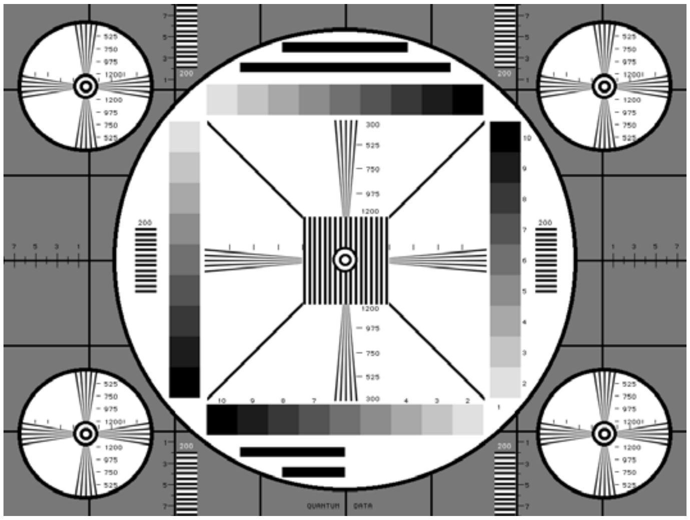
The MoireX and MoireY images consist of black lines on a white background across the active video area. MoireX provides vertical lines; MoireY provides horizontal lines. The MoireX image is shown below.

The primary version of the MoireX33 and MoireY33 images provide a black frame around the black lines. The secondary version draws a white frame around black lines. The primary version of the MoireX33 image is shown below.



16.112 Monoscope

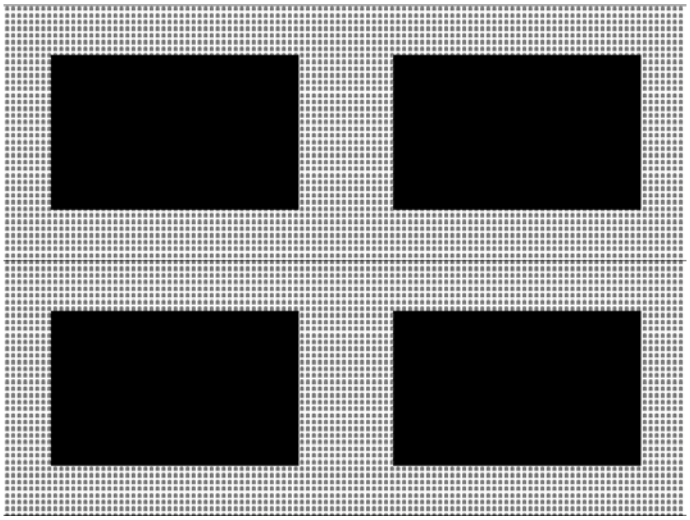
16.112.1 Description



16.113 MSony7, MSony8

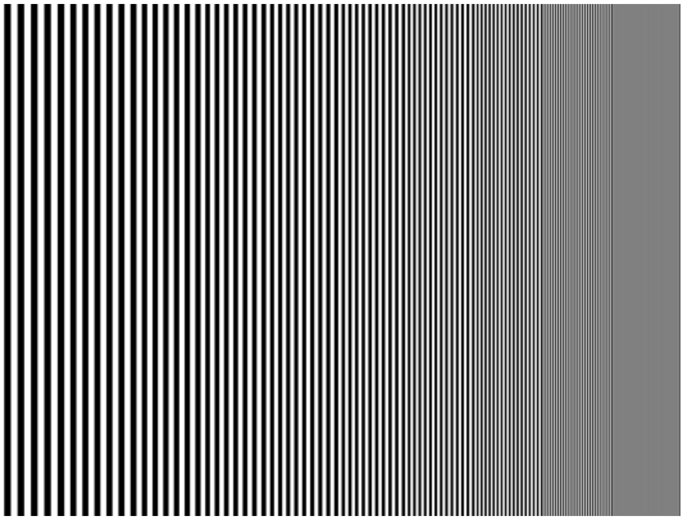
16.113.1 Description

Special test image developed per customer specifications. Primary version of the MSony7 image is shown below. The secondary version draws white boxes and characters with a black background.



16.114 MulBurst

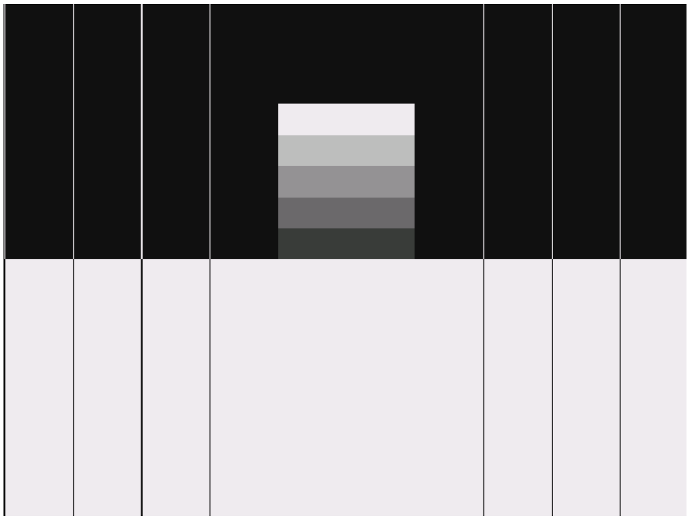
16.114.1 Description



16.115 Needle

16.115.1 Description

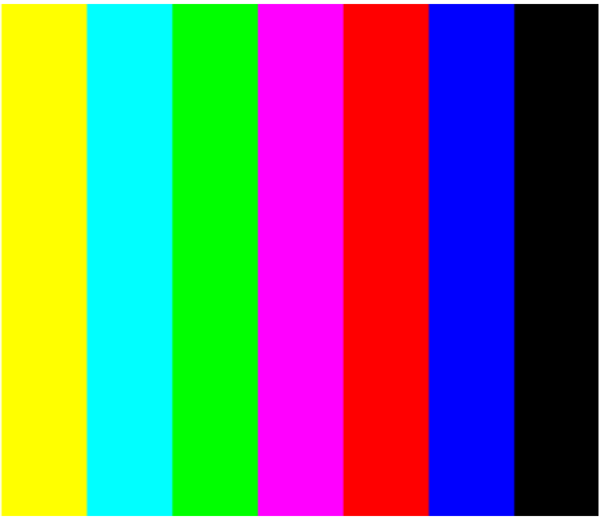
To check and adjust for the proper geometry of display including picture centering, size, pincushion and linearity



16.116 Orion

16.116.1 Description

This image provides a color bar that rotates (shifts) the bars to the right on an incremental basis.



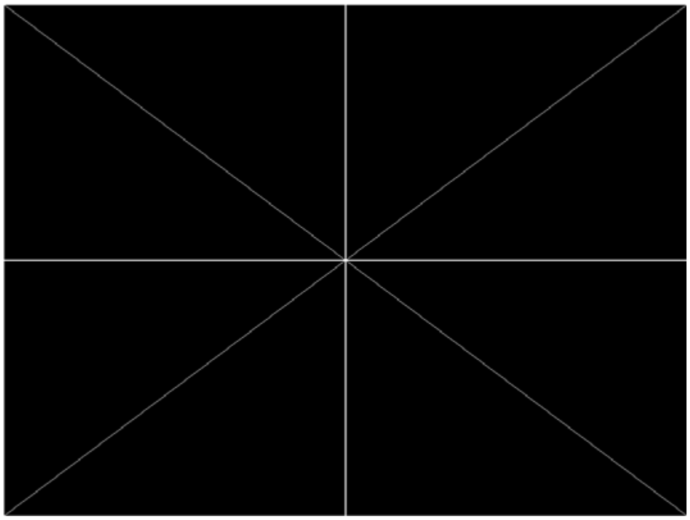
The color bars are shifted to the right at 3 second intervals. You can access additional renditions to adjust the interval between 3, 10, 30 and 60 seconds through the **Settings/Rendition** dialog box.

16.117 Outline0, Outline1, Outline2, Outline3

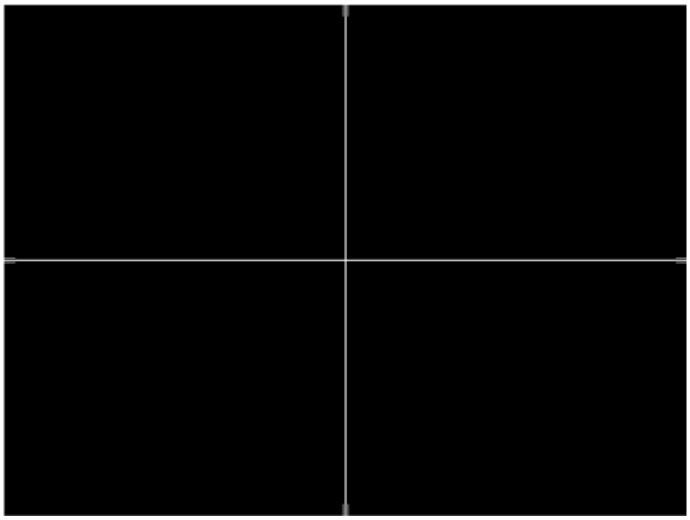
16.117.1 Description

The primary version of the Outline0 image consists of a rectangular white border on a black background. The border is one (1) pixel wide and defines the active video area. Two (2) diagonal lines join the opposite corners. A-full size cross is centered in the image. The horizontal line of the cross is one (1) pixel thick for formats with an odd number of active lines and two (2) pixels thick for formats with an even number of active lines. The vertical line of the cross is one (1) pixel thick for formats with an odd number of active pixels per line and two (2) pixels thick for formats with an even number of active pixels.

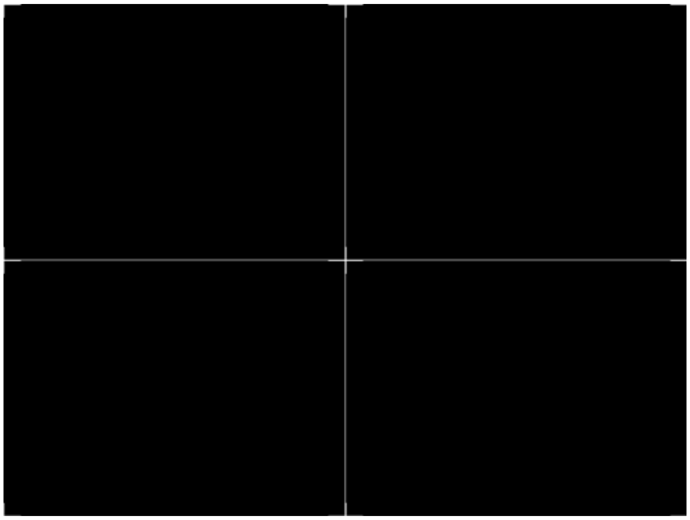
The secondary version of these images draw black lines on a white background.



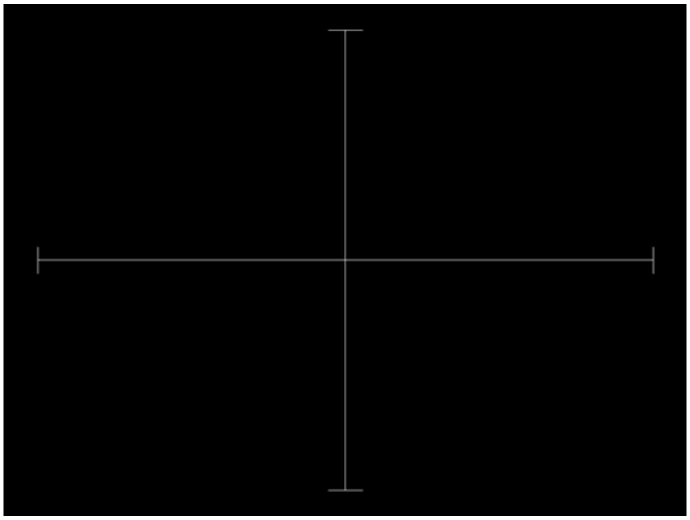
In the Outline1 version, the two diagonal lines are removed and short marker lines are added to the border lines near to where the cross lines meet the border lines. The markers appear at both sides of the cross lines. The distance between the marker lines and the cross lines is the greater of either two (2) pixels or one (1) millimeter.



In the Outline2 version, the two diagonal lines are removed and short marker lines are added to the corners, and where cross lines meet and end.



In the Outline3 version, the two diagonal lines are removed, cross lines are shortened, and short marker lines are added.



16.117.2 Test

Yoke tilt correction.

16.117.3 Purpose

The horizontal axis of a displayed image should line up with the horizontal axis of your monitor. Any tilt is likely due to the yoke being rotated on the neck of the CRT. A rotated yoke makes any displayed image appear rotated.

16.117.4 Method

Place your monitor on a flat surface so the face of the CRT is perpendicular to the surface.

Use a ruler or gauge to measure the height of each end of the image’s horizontal center line from the surface. The difference between the two readings should be within specification for the monitor. If it is out of specification, the yoke must be adjusted. Loosen the hardware that clamps the yoke to the neck of the CRT and rotate the yoke until the line is horizontal. Tighten the yoke-clamp hardware.

16.117.5 Test

Yoke winding orthogonality check.

16.117.6 Purpose

The horizontal and vertical deflection coils on the yoke should have their axes cross at exactly 90 degrees. Improper orientation of the windings causes displayed rectangles to look more like nonorthogonal parallelograms. This type of defect is almost impossible to correct with adjustments. It is usually easier to replace the defective yoke.

16.117.7 Method

First, perform the yoke tilt correction described above. The vertical center line of the image should be perpendicular to the work surface. If the deviation is beyond specification, the monitor should be rejected and sent back for repair, rather than trying to magnet a defective yoke.

16.117.8 Test

Display size correction.

16.117.9 Purpose

A too-large active video size adjustment on a monitor may cause information to be lost around the edges of the screen. A too-small active video size adjustment may make some displayed information hard to read. The correct size is needed to obtain the correct aspect ratio. You need the correct aspect ratio to get round circles and square squares.

16.117.10 Method

First, determine the correct physical size of the active video area for the display. This information usually is given in a display’s specification sheet or service manual. The size should match the sizes in the format you are using. The size setting of the current format can be checked using the Format test image.

Place a ruler or gauge along the horizontal line of the image and adjust the monitor's horizontal size control until the distance between the end points matches the specified value.

Move the ruler or gauge to the vertical line and adjust your monitor's vertical size control until the distance between the end points matches the specified value.

16.117.11 Test

Parallelogram distortion check.

16.117.12 Purpose

Parallelogram distortion is very difficult to correct with magnets because the correction often causes barrel distortion. Therefore, you should decide early whether your monitor meets this specification. The problem usually can be traced to the improper winding of the yoke coils. If the problem is not too severe, it may be corrected by adding or adjusting magnets on the yoke. However, if the distortion is excessive, it may be an indication of a defective yoke which cannot be corrected with magnets.

16.117.13 Method

Measure the lengths of the two (2) diagonal lines. Any difference is an indication of parallelogram distortion. The difference in readings should be within the specifications of the monitor.

If the difference in the readings is too far beyond specification, the monitor should be rejected and sent back for repair, rather than trying to magnet a defective yoke.

16.117.14 Test

Trapezoid distortion correction.

16.117.15 Purpose

This image gives you a way to measure trapezoid distortion in your monitor. If the distortion is not too severe, you may be able to correct it by adding or adjusting magnets on the yoke.

16.117.16 Method

Perform the yoke winding orthogonality check and parallelogram distortion check first to avoid wasting time on a monitor with a defective yoke.

Measure the width of the image at the top and bottom of the display. Any difference in readings should be within the specification limits. Measure the height of the image at both sides of the display. Again, any difference in readings should be within specification limits. If either of the differences is out of specification, the trapezoid distortion of the monitor is out of specification.

Add or adjust magnets on the yoke to correct the problem. The pin and barrel distortion correction should be repeated to make sure that it is still in specification.

16.117.17 Test

Pin and barrel distortion correction.

16.117.18 Purpose

If perfectly linear sweep signals are sent to a perfectly wound deflection yoke mounted on a perfect CRT, you would not necessarily get a perfectly formed raster. Instead you would likely get a raster that had its corners stretched away from the center, resembling a pin cushion. This distortion occurs because the geometry of the deflected electron beam does not match the geometry of the tube face plate. Also, imperfections in the yoke or CRT may affect this problem. In some cases one or more corners may be pulled towards the center of the raster causing it to look like a barrel. Uncorrected raster distortion carries over as distortion of the displayed image.

16.117.19 Method

A slot gauge may be used to determine if the amount of pincushion or barrel distortion is within limits. A basic slot gauge may consist of a piece of opaque film with at least two (2) transparent slots in it. One slot is used for top and bottom distortion and the other is used for the sides. By positioning the correct slot over each portion of the border line, the entire line should be visible. If this cannot be done at all four sides, the monitor requires correcting.

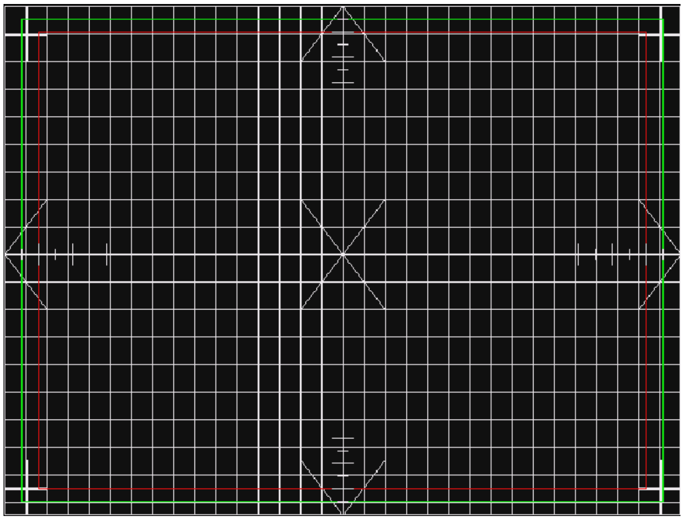
There are two main ways of correcting pincushion distortion. The first involves placing or adjusting magnets on the yoke. This is a trial-and-error method. However, skilled operators develop a feel for how strong a magnet to use and how to place it in order to get the desired correction. If any correction is performed, the trapezoid distortion correction should be repeated.

The other correction method involves adding correction signals to the deflection signal driving the yoke. This method is usually found in color monitors, where adding magnets to the yoke would cause problems with convergence and purity. The type and number ofadjustments depends on the monitor being tested.

16.118 OverScan

16.118.1 Description

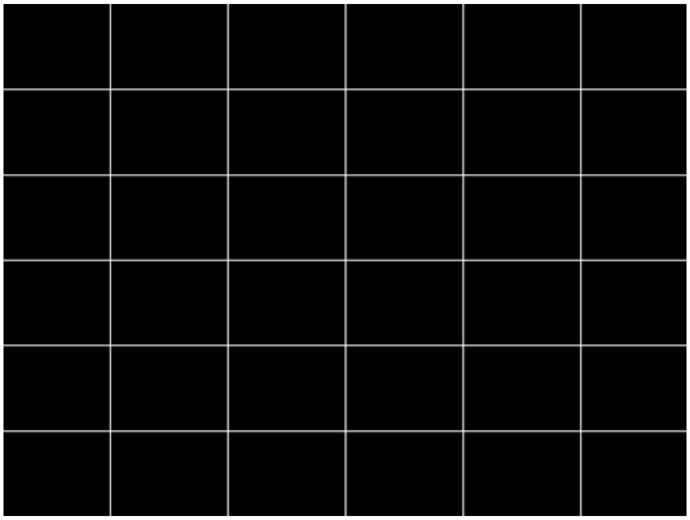
To check and adjust for the proper geometry of display including picture centering, size, pincushion and linearity.



16.119 P1

16.119.1 Description

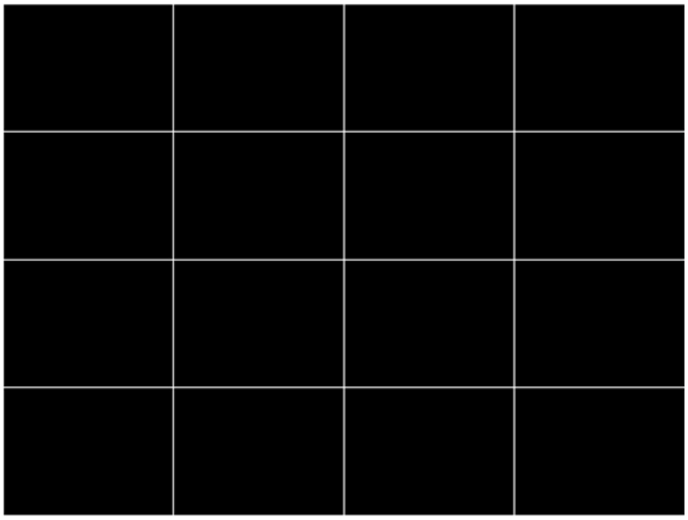
This image is a 6x6 white crosshatch without a border on a black background.



16.120 P2

16.120.1 Description

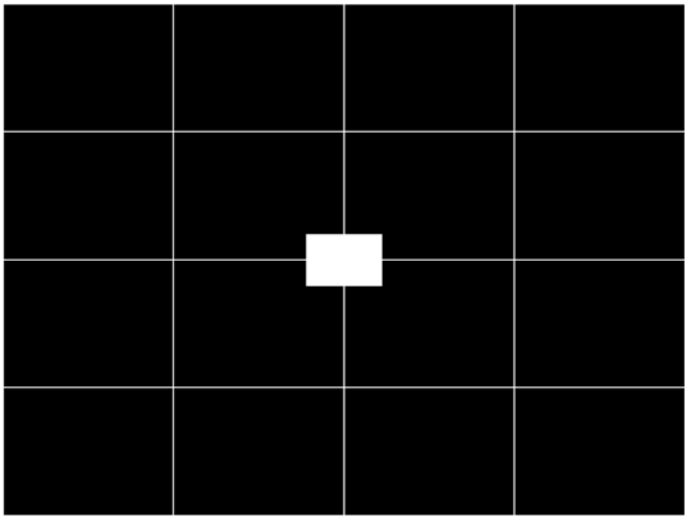
This image is a 4x4 white crosshatch with a border on a black background.



16.121 P3

16.121.1 Description

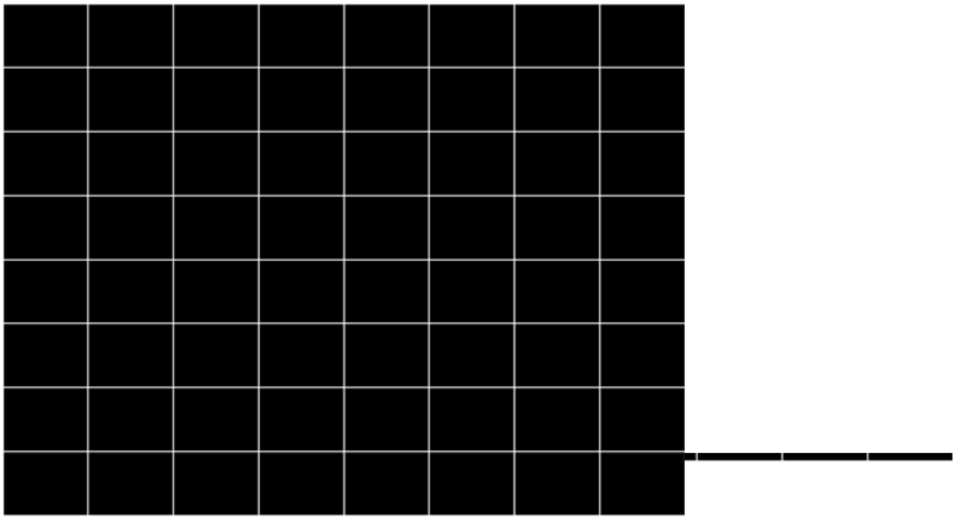
This image is a 4x4 white crosshatch with a border and a small, centered white patch on a black background.



16.122 P4

16.122.1 Description

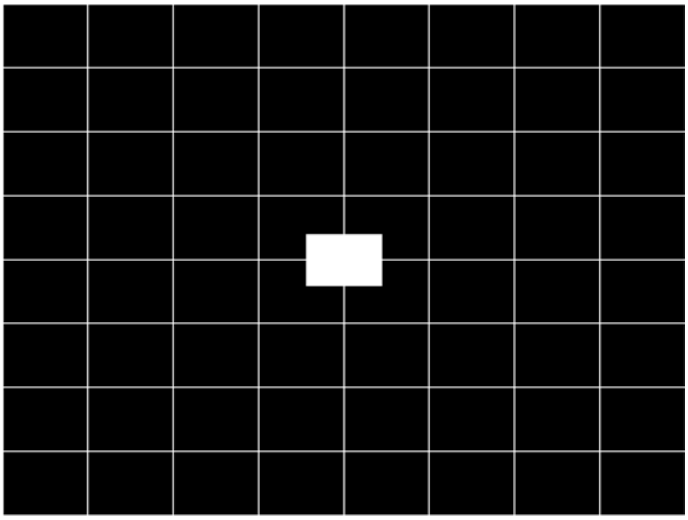
This image is an 8x8 white crosshatch with a border on a black background.



16.123 P5

16.123.1 Description

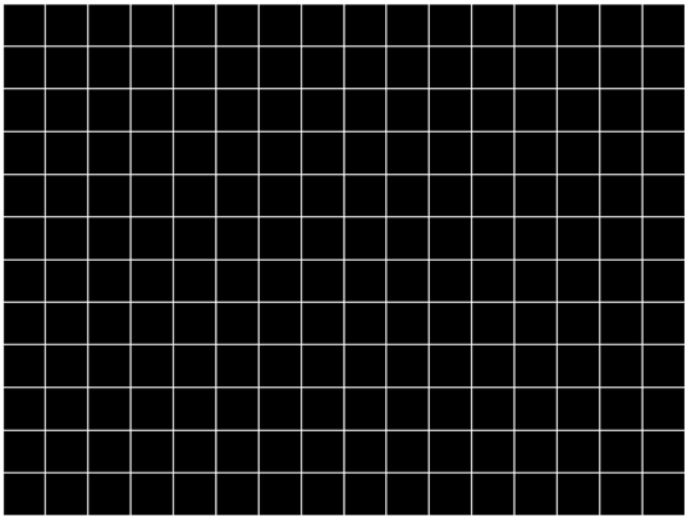
This image is an 8x8 white crosshatch with a border and a small, centered white patch on a black background.



16.124 P6

16.124.1 Description

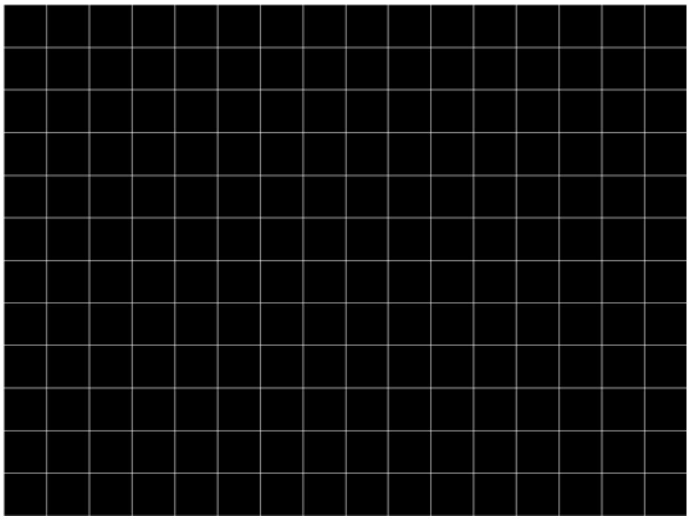
16x12 pixel white crosshatch with a border on a black background.



16.125 P6_Sony

16.125.1 Description

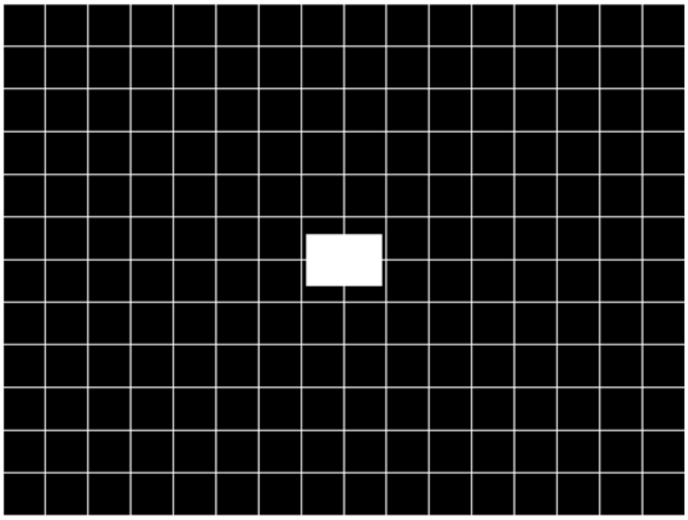
6x12 pixel white crosshatch with a border on a black background.



16.126 P7

16.126.1 Description

16x12 white crosshatch with a border and a small, centered white patch on a black background.



16.127 P8

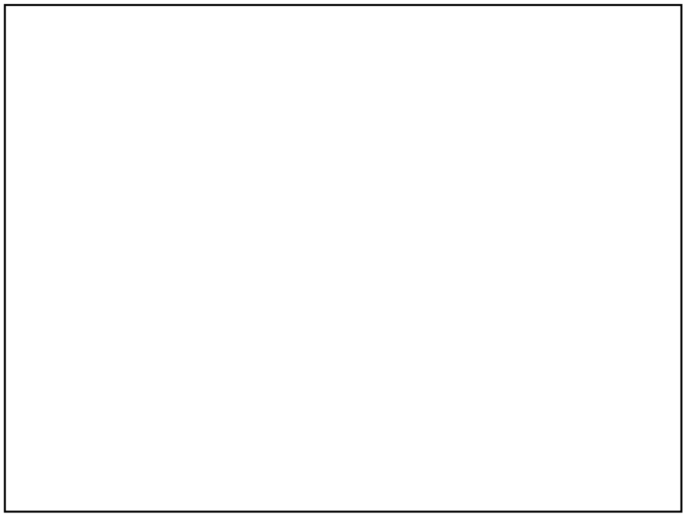
16.127.1 Description

This image is an all black active video area. The secondary version draws an all white video area.

16.128 P9

16.128.1 Description

This image is an all white active video area. The secondary version draws an all black video area.



16.129 PacketTx

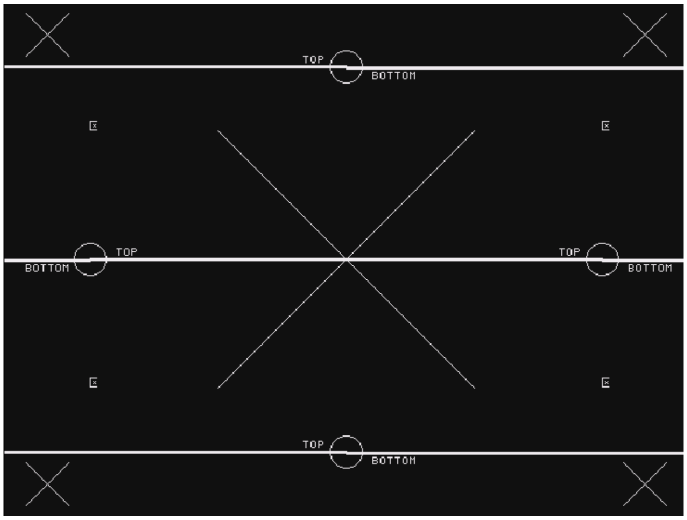
16.129.1 Description

Displays the InfoFrame data transmitted from the HDMI transmitter.

16.130 Pairing

16.130.1 Description

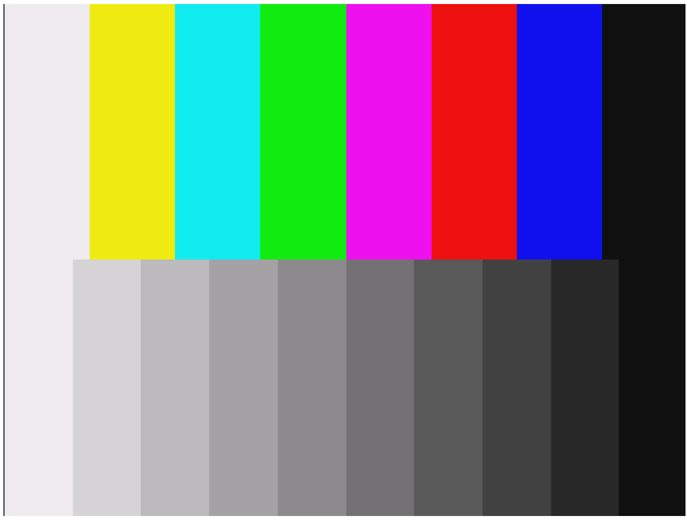
Displays the InfoFrame data transmitted from the HDMI transmitter.



16.131 PanBars

16.131.1 Description

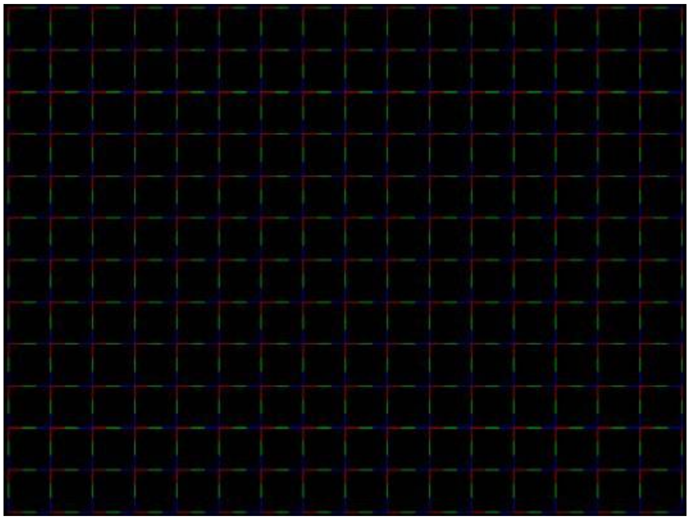
Special test images developed per customer specifications.



16.132 PdsCrt1

16.132.1 Description

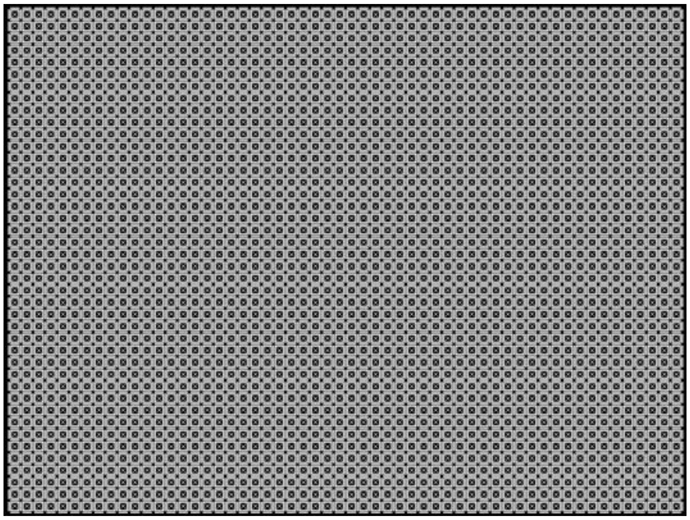
Special test image developed per customer specifications.



16.133 PdsCrt2

16.133.1 Description

Special test image developed per customer specifications.



16.134 Persist

16.134.1 Description

In the primary version, 15 small white boxes move back and forth between diagonal guide lines. The lines form 15 side-by-side tracks. The size of each box is scaled to the light meter box size set by the MSIZ system parameter. The image does the following:

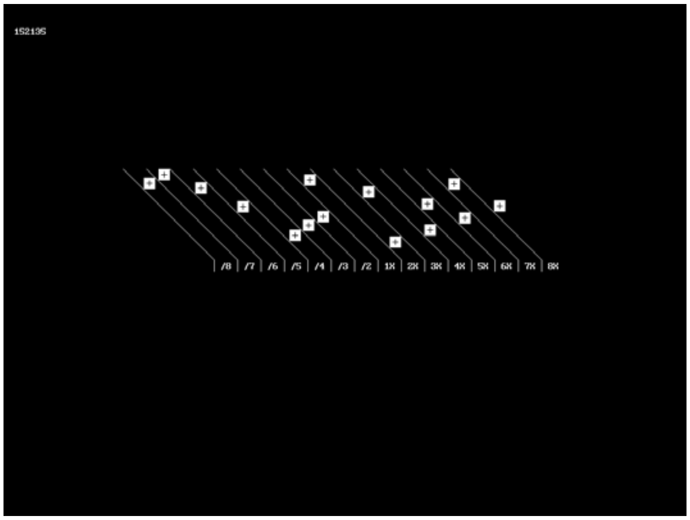
- The box in the center track (marked “1X”) moves one scan line vertically and one pixel horizontally for each vertical frame of refresh.
- The seven boxes to the right of the center track (marked “2X” through “8X”) move 2, 3,4, 5, 6, 7, and 8 pixels and lines per frame, respectively.
- The seven boxes to the left of the center track (marked “/2” through “/8”) move one scan line vertically and one pixel horizontally for every 2, 3, 4, 5, 6, 7, and 8 vertical frames of refresh, respectively. These boxes are at the bottom of the tracks.

In cases where the next move would cause the box to move beyond the end of its track, it immediately reverses and moves the correct distance in the opposite direction for the next frame.

A continuously-running counter appears in the upper left corner of the image. The number shown is the number of vertical frame refreshes that have occurred since the generator was first powered up.

The secondary version draws a black image on a white background.

An example of the primary version of the Persist image is shown below:



16.134.2 Test

Phosphor persistence

16.134.3 Purpose

The phosphors on the face of most CRTs continue to glow for a short period of time after the electron beam has stopped energizing them. This phenomenon is called persistence. A certain amount of persistence is desirable in most applications. It prevents a flickering of a displayed image that most users would find objectionable. On the other hand, a CRT with an overly long persistence time causes moving objects to leave a blurred trail.

16.134.4 Method

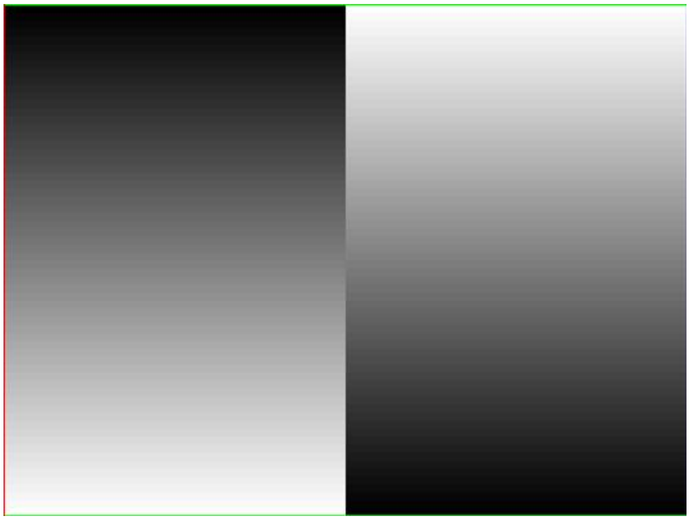
A flickering in the slower moving boxes indicates that the combination of refresh rate and phosphor persistence is not suitable for long-term viewing.

A fading tail left behind by the faster moving boxes indicates that the display may not be suitable for viewing animated images.

16.135 PgBar64H, PgBar64V

16.135.1 Description

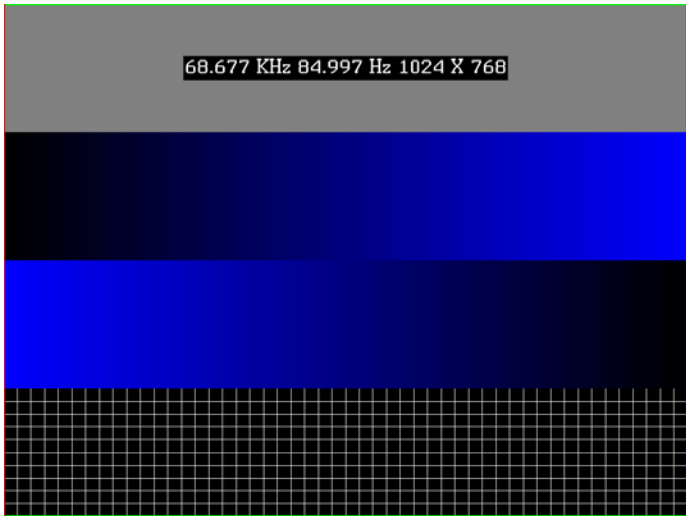
Special test image developed per customer specifications. The PgBar64H image is shown below.



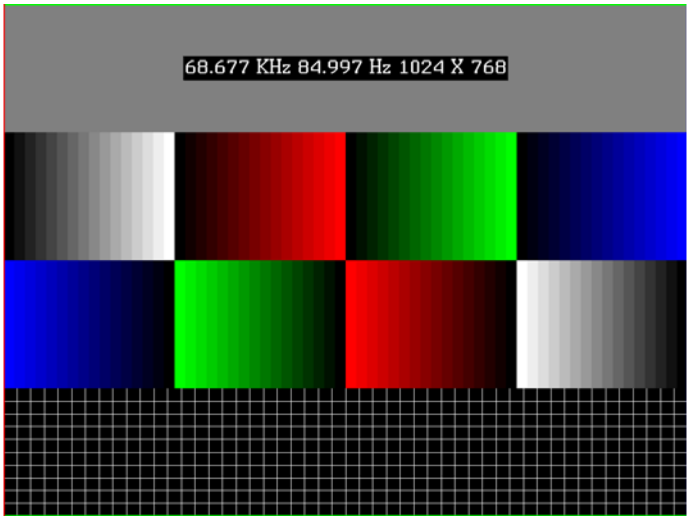
16.136 PgCB, PgCG, PgCR, PgCW, PgCWrgb

16.136.1 Description

Special test image developed per customer specifications. Primary version of PgCB is shown below. The secondary versions draw all white over the last bar.



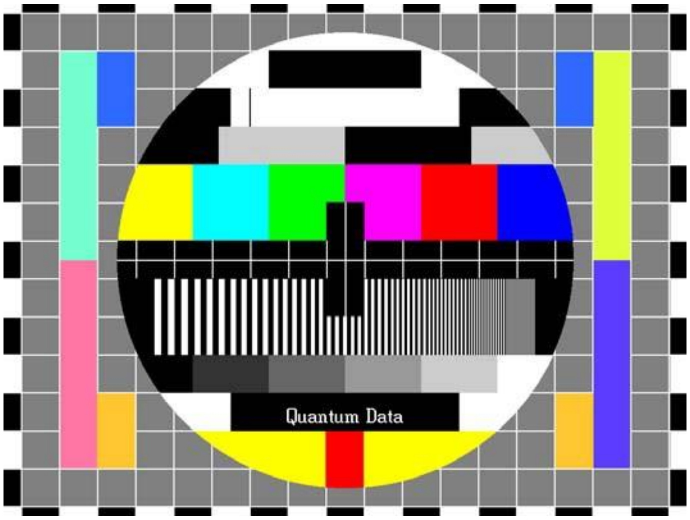
The PGCWrgb is shown below.



16.137 Philips1

16.137.1 Description

Special test image developed per customer specifications.



16.138 Pluge

16.138.1 Description

The two feint vertical stripes on the left are just above and just below black level. The monitor's brightness control should be adjusted so that the super-black stripe is lost, but the other can just be seen.

16.139 PRN24bit

16.139.1 Description

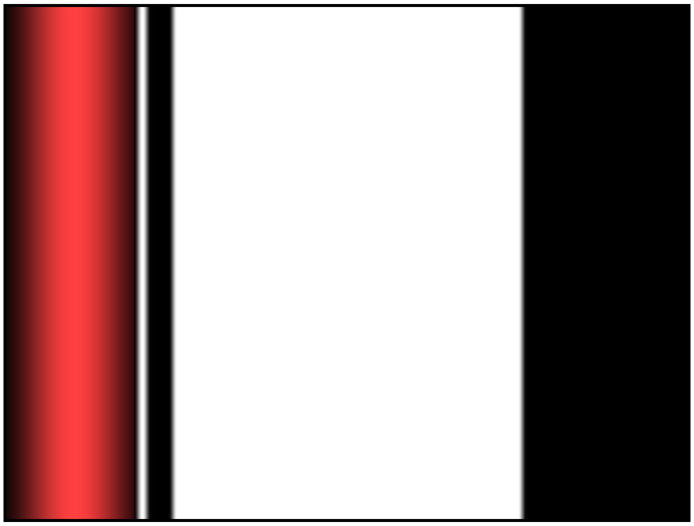
This image displays pseudo-random noise using 24-bits-per-pixel color depth.

16.140 PulseBar

16.140.1 Description

This image is intended for TV formats, but can be displayed with any format up to 100

MHz. The image looks like two vertical lines followed by a wide vertical bar on a display's screen. The first line is a sine-squared modulated pulse that fades from black to red and back to black. The pulse is 20 T for PAL and 12.5 T for NTSC formats. The second narrower line is a 2 T white sine-squared pulse. T = 100 nSec for PAL and 125 nSec for NTSC formats. The wide bar is white with sine-squared edges.



16.140.2 Test

Video system testing.

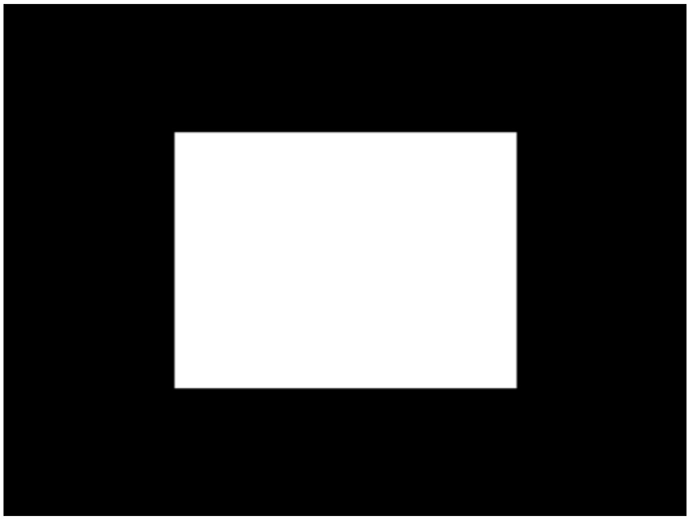
This multi-purpose pattern can be used with other instruments to check television K factors. The modulated pulse can be used to check chrominance-to-luminance delay and gain. The narrow white line can be used to measure short term linear distortion (K2T).

16.141 QuartBox

16.141.1 Description

The primary version (shown below) has a single white box in the center of active video.

The size of the box is one-half the width and height of the active video area (a quarter of the entire active video area). The secondary version draws a black box on a white background.



16.141.2 Test

Brightness control adjustment.

16.141.3 Purpose

The wrong brightness setting on your monitor may cause other tests such as Contrast, Focus, and Beam Size to be invalid. An accurate brightness setting helps give repeatable measurements throughout other tests. This version of the brightness box should be used if the display's specifications call for the brightness to be set with one-fourth of the screen lit.

16.141.4 Method

Place your light meter probe within the center box and adjust the monitor's brightness control to obtain the required light meter reading.

16.141.5 Notes

The color of the center box is a special color, named foreground. The FRGB command can be used to change the default color of foreground to any RGB value.

```
IMGL quartbox: ALLU// loads QuartBox image
FRGB 122 122 122// sets RGB color of box
```

After loading a different format, send the FRGB command again to set the box fill color.

If you want to draw your own box, use foreground as the fill color, and then use the FRGB command to define the color of “foreground.” For example:

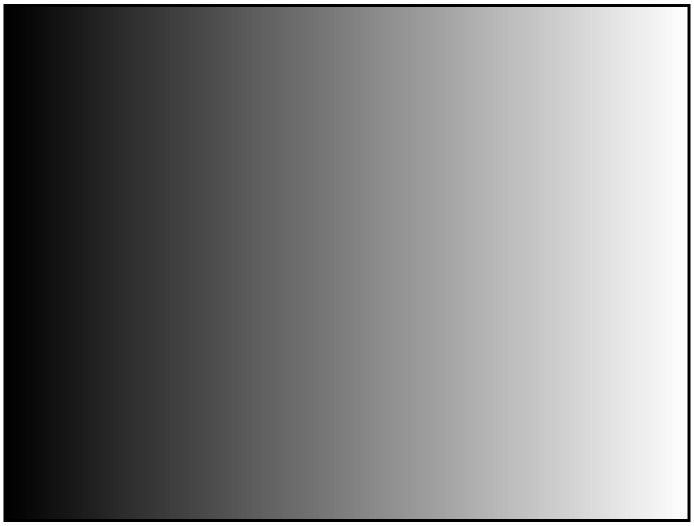
```
IMGL raster; ALLU// clears display
RECT foreground 100 100 100 100 dither100
FRGB 128 128 0
FRGB 192 192 64
FMTL DMT0660; ALLU FRGB 192 192 64
```

16.142 Ramp

16.142.1 Description

This image provides an active video area starting from full black (+7.5 IRE) at one edge of the screen to full white (+100 IRE) at opposite end of the screen.

There are 4 versions of this image—one for each edge of the display. When selected, this image is displayed.



You can access additional versions of this image through the **Settings/Rendition** dialog box.

16.143 Ramp12

16.143.1 Description

This image is used to view a specific range of grayscale levels (ranges up to 1024) throughout the entire range allowed by deep color support in the generator (i.e. 36 bit/pixel or 12-bit/component = 4096). If you set the ramp to display the maximum color depth supported by the display under test you will see a nearly uniform ramp depending on the horizontal resolution of the active format.

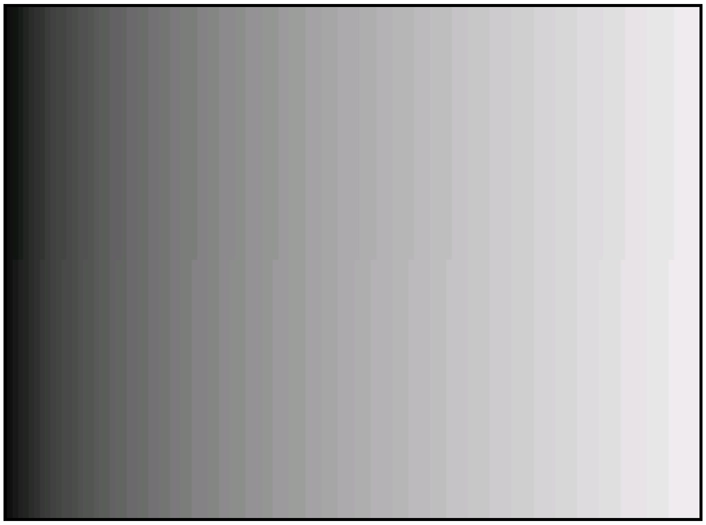
The following is a sample of the Ramp12 image is rendered on a display.

16.144 RampDif

16.144.1 Description

This image has two ramps. One on the top and one on the bottom. It enables you to show a contrast of color depths. For example you can specify that the top ramp use 12-bit/component deep color and the bottom ramp 10-bit color. You can then view the image and see whether banding occurs and how pronounced, in the either of the ramps. If the display under test supports 12-bit/component color, the top ramp will show a near uniform ramp on the top (depending on the horizontal resolution of the active format). The bottom ramp will show more pronounced banding because the range of the ramp is greater than the color depth.

This image is used to view two specific range of grayscale or color levels (ranges up to 512) throughout the entire range allowed by deep color support in the generator (i.e. 36 bit or 4096). You need to set the pixel depth in the generator to 24 bit (PELD = 32) in order to access 512 grayscale or color levels on a single image rendered on a display. The following is a sample of the RampDif image is rendered on a display.

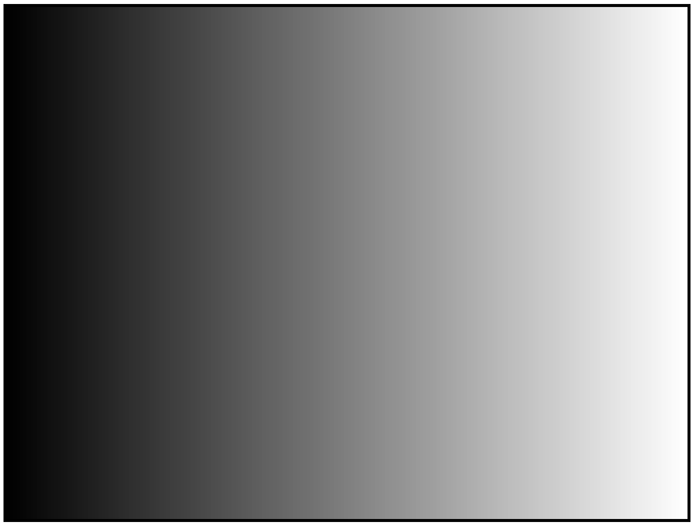


16.145 RampX

16.145.1 Description

This image provides a ramp image that continuously sweeps (moves) to the right on an adjustable time basis.

When selected, this image is displayed.



You can access additional versions of this image through the **Settings/Rendition** dialog box.

16.146 Ramp_B, Ramp_G, and Ramp_R

16.146.1 Description

The active video area goes from full black (+7.5 IRE) at the left edge of the screen to full blue (_B), green (_G), or red (_R) at the right edge. The Ramp_B image is shown below.

16.146.2 Test

Video gain linearity.

16.146.3 Method

When viewed on a TV screen, the full range of grays should be visible. There should be no color shifts visible.

16.147 Raster

16.147.1 Description

The primary version shows a totally black display (nothing being displayed). The secondary version shows a totally white display.

16.147.2 Test

Raster centering.

16.147.3 Purpose

Many monitor applications require that the displayed image or text fit completely within a bezel that surrounds the CRT. This usually requires that you first center the blank raster on the face of the CRT, and then center the image within the raster. Use this image for centering the raster on the CRT.

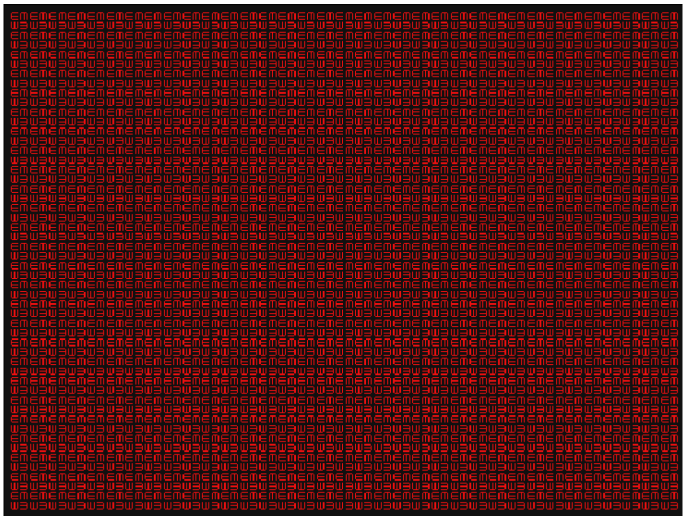
16.147.4 Method

Turn up your monitor’s brightness control until the raster is just visible. Adjust the raster’s position and size using the size and raster centering controls. The raster centering adjustment for many monochrome monitors consists of moving magnetic rings on the deflection yoke.

16.148 RED_EM, RED_EM+

16.148.1 Description

In the primary version, the screen is filled with red (RED) EM character blocks on a black background.



16.149 Regulate

16.149.1 Description

The image cycles between two (2) patterns. In the primary version, the first pattern is a white outline that defines the edges of displayed video. The other pattern has the same outline plus a solid white rectangle in the center. The size of the solid rectangle equal 95% of the height and width of displayed video. The speed of the cycle cannot be changed. The secondary version has a thick white frame with a black center for the first pattern and a solid white active video area for the other pattern.

The first pattern of the primary version is shown below.

16.149.2 Test

High voltage regulation.

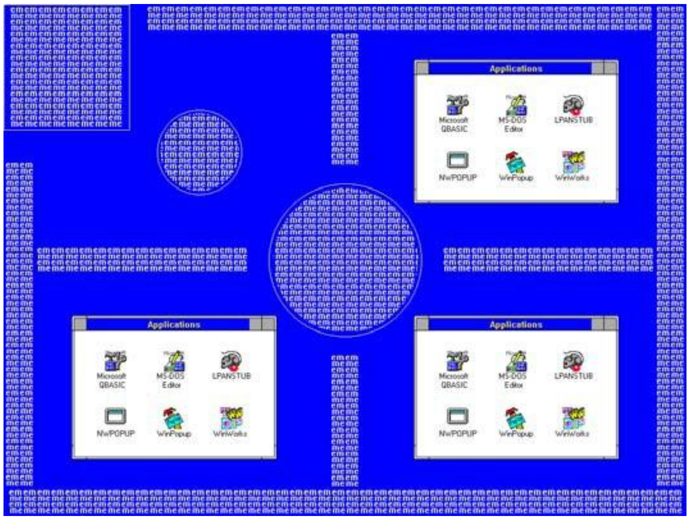
16.149.3 Method

The size of the border should not change for each half of the image. The change in border size between the two images should be within the specification limits of the monitor.

16.150 Samsung1, Samsung2

16.150.1 Description

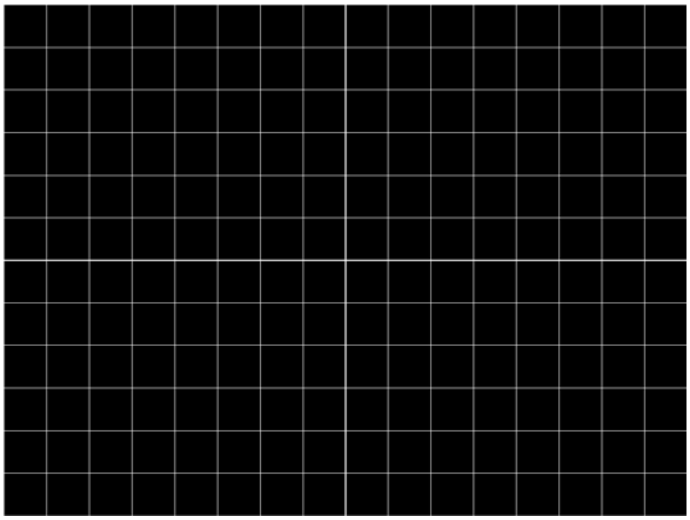
Special test images developed per customer specifications. The image consists of three small simulations of Microsoft Windows® screens on a blue background (Samsung1) or black background (Samsung2). A border and centered cross are formed with repeating groups of the characters “e” and “m”. The repeating characters are also used to form a rectangular patch in the upper left hand corner and a circular area in the center of the image. The secondary version of Samsung2 draws a white background.



16.151 Samsung3

16.151.1 Description

Special test image developed per customer specifications.



16.152 Samsung 4

16.152.1 Description

Special test image developed per customer specifications.

16.153 Samsung5

16.153.1 Description

Special test image developed per customer specifications.

16.154 Samsung6

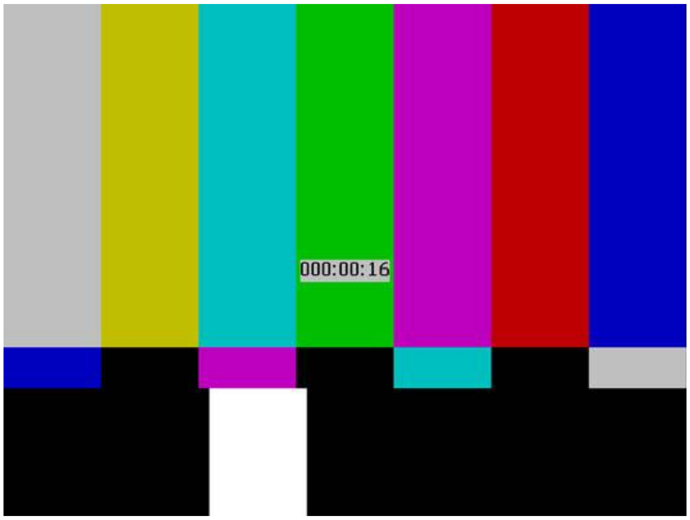
16.154.1 Description

Special test image developed per customer specifications.

16.155 SansungB

16.155.1 Description

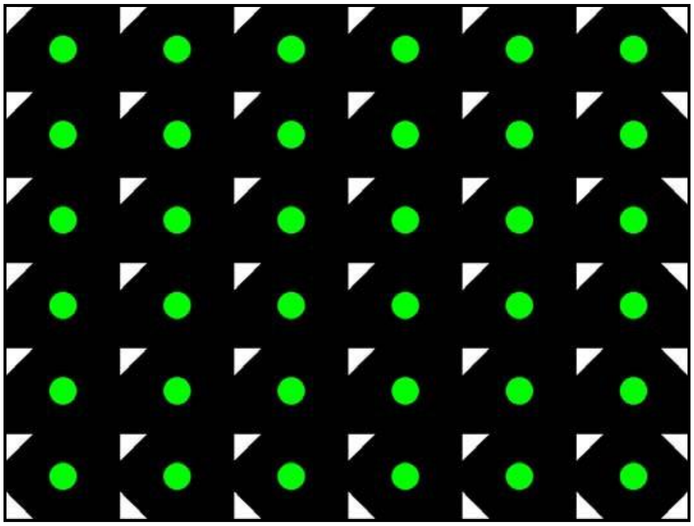
Special test image developed per customer specifications.



16.156 SamsungT

16.156.1 Description

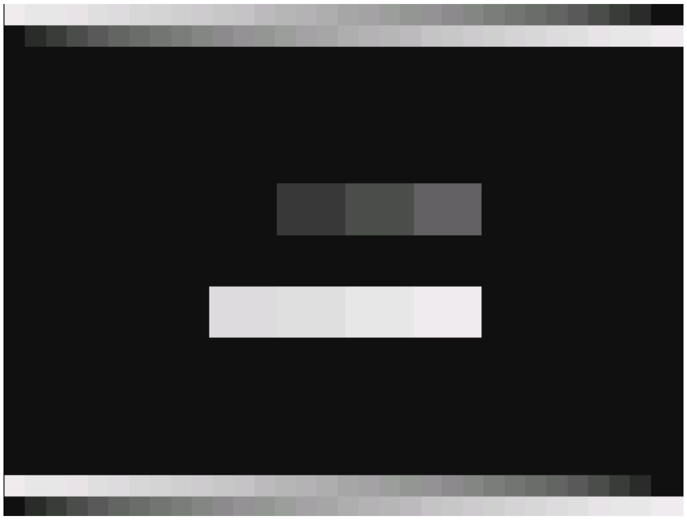
Special test image developed per customer specifications. There are four versions of this image. When selected, the following image is displayed.



16.157 Set01k

16.157.1 Description

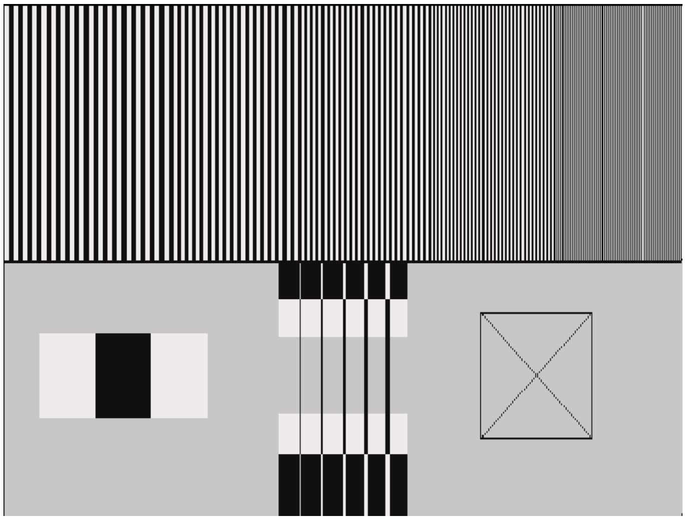
Special test image developed per customer specifications. There are 8 shades of gray from full black (0 volts) to full white.



16.158 Sharpnes

16.158.1 Description

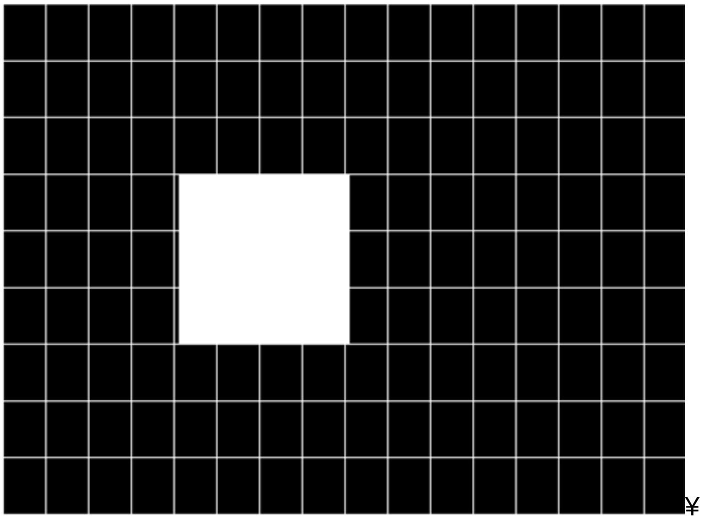
The top of this pattern is the same as the Multiburst. The bottom, with all its single-pixel black lines, allows you to fine-tune the sharpness control.



16.159 SlideBox

16.159.1 Description

This image displays a 16x9 white crosshatch with a large white patch moving across the screen.



¥

To change the animation speed:

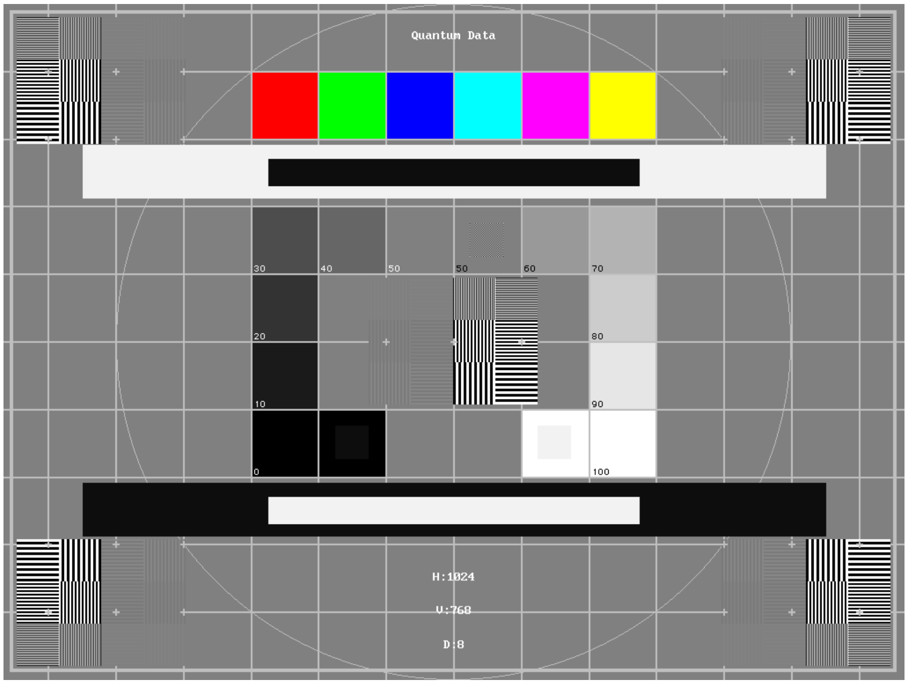
1. Load the SlideBox image.
2. Establish a terminal session with the generator (see page 30).
3. Enter the following commands:

```
ISUB 1
IVER 1
IMGU
DELX 10; IMGU
DELX 20; IMGU
```

16.160 SMPTE133

16.160.1 Description

This image is based on a recommended practice (RP-133) test pattern designed by the Society of Motion Picture and Television Engineers (SMPTE). The original application was used in testing and evaluating medical imaging monochrome displays. The image now is used in many different display applications. The image is self-scaling as to the number of active pixels and active lines used. Some of the image's elements have minor differences from the original SMPTE specification.



These differences are noted in descriptions of the individual elements.

The image is drawn on a reference background having a 50% intensity level. The background covers the entire active video area.

Crosshatch – There are 10 boxes vertically. The number of horizontal boxes is based on the physical aspect ratio determined by the HSIZ and VSIZparameters in the currently loaded format. The boxes are perfectly square with any fractional spaces placed around the outside edges of the image. The vertical lines are two (2) pixels thick while the horizontal lines are two (2) scan lines thick. Small crosses indicate the intersection of the horizontal and vertical lines when they are covered by other parts of the image. All parts of the crosshatch are normally drawn using a 70% intensity level. A 75% level is used in the secondary version.

Resolution patch – The patch is made up of six (6) smaller boxes that are each about 6.25% of the height of the display. The boxes are made of alternating intensity (0 and 100%) stripes. The stripes run vertically and horizontally. The stripes may be one (1), two (2) or three (3) pixels wide each. Details of the patch are shown in the lower half of the following illustration. The patches are located in each corner of the main image and in the center. They are oriented with the highest resolution and contrast boxes closest to the outside corners. The 48%-53%, 48%-51% and 50%-51% level patches are omitted in the secondary version.

Grayscale boxes – Twelve (12) boxes at eleven (11) intensity levels are clustered around the center of the main image. They start at 0% and increase in 10% steps to100% with two (2) boxes at a 50% level. All of the grayscale boxes are omitted in the secondary version.

Gamma check dither box – A small box is drawn inside the right-hand 50% grayscale box. The box is half the width and height of the larger box. The box consists of a checkerboard of alternate one-on and one-off pixels. The alternate pixels have levels of 0 and 100%. This smaller box is not part of the original SMPTE specification and is omitted in the secondary version.

Contrast boxes – Two (2) boxes are drawn adjacent to the grayscale boxes. They are at 0 and 100% levels. There are smaller boxes drawn inside each box at 5 and 95% levels. The contrast boxes are omitted in the secondary version.

Black and white windows – Two (2) horizontal bars are located above and below the grayscale boxes. Their height equals 8% of the display height. There are half-size bars centered in the larger bars. In the primary version, the dark portion of the windows is at a 5% level and the bright portion is at a 95% level. Zero and 100% levels are used in the secondary version.

Border – A border line is drawn around the image. It is set in from the edges of displayed video a distance equal to 1% of the displayed height and has a thickness equal to 0.5% of the displayed height. The intensity level is the same as that of the crosshatch lines.

Circle – A large circle is centered in the image. It touches the top and bottom of the active video area when the aspect ratio is wider than it is high (landscape-type display). The circle touches the left and right sides of active video when the aspect ratio is taller than it is wide (portrait-type display). The intensity level is the same as that of the crosshatch lines. The circle is not part of the original SMPTE specification.

Resolution data - The number of active pixels per line and the number of active lines is shown as text below the lower black and white window. The pixel depth also is shown. The intensity level of the text is the same as that of the crosshatch lines. The displaying of the data is not part of the original SMPTE specification.

The secondary version adds a row of six (6) color bars above and below the black-and-white windows. The order of the colors, from left to right, is red, green, blue, cyan (g+b), magenta (r+b) and yellow (r+g). The top row is drawn at 100% intensity levels and the bottom row is drawn at 50% intensity levels. Color bars are not part of the original SMPTE specification.

16.160.2 Test

Deflection linearity.

16.160.3 Method

If the overall height and width of the display’s active video area match the sizes in the format, the large circle should be perfectly round. Each box in the crosshatch pattern should be the same size and shape.

16.160.4 Test

High contrast resolution.

16.160.5 Method

All the 0 and 100% level stripes in all the resolution patches should be separate and distinct.

16.160.6 Test

Low contrast resolution and noise.

16.160.7 Method

All the mid-level 2 on - 2 off stripes in all the resolution patches should be visible and distinct. This is a sensitive test for noise in the display’s video amplifiers.

16.160.8 Test

Quick gamma check.

16.160.9 Method

The average brightness level of the small gamma dither box should match the brightness of the larger surrounding box. This is a visual check to see if the display’s gamma correction is producing the correct mid-level response.

16.160.10 Test

Video gain linearity and gamma.

16.160.11 Method

The individual grayscale boxes all should be at their indicated levels. A small aperture photometer is usually required to get accurate and repeatable readings.

16.160.12 Test

Contrast and brightness check.

16.160.13 Method

On a display with properly adjusted brightness and contrast controls, both the 5% and

95% contrast boxes should be clearly visible inside their larger surrounding 0% and 100% boxes.

16.160.14 Test

Video amplifier stability.

16.160.15 Method

The two black-and-white windows should show sharp transitions between the smaller box and the surrounding window. Streaking may be an indication of undershoot or overshoot while ghost images may indicate a ringing problem.

16.160.16 Test

Excessive overscan and off-center alignment

16.160.17 Method

The entire border should be clearly visible on the face of the tube and not be hidden by the edge of the glass or by any bezel.

16.160.18 Test

Interlace flicker.

16.160.19 Method

The horizontal 1 on - 1 off stripes in the resolution boxes should not have objectionable flicker when shown with an interlaced format. Excessive flicker indicates that the combination of the display's CRT persistence and frame scan rate is below the persistence time of the human eye.

16.161 SMPTEbar, SMPTEbr2

16.161.1 Description

This image is based on an engineering guideline (EG1-1990) test signal specified by the Society of Motion Picture and Television Engineers (SMPTE). The SMPTE pattern, in turn, is derived from an EIA standard test pattern (RS-189-A). The image, is set up to be generated by an 801GX generator as an encoded TV output. It is designed for adjusting the color settings of a television monitor by eye. It can also be used with a TV waveform analyzer and vectorscope for testing video signal processors and color decoders. The image is available on all models as a component RGB signal. Some of the image's elements have some differences from the original SMPTE specification.

These differences are given in descriptions of the individual elements.

- The upper 67% of the image consists of a series of color bars. These bars match the order of the bars in the SMPTE and EIA patterns. They are similar to the 801GX's TVBar_75 image without the last black bar.
- The left side of the lower 25% of the image contains isolated -I and Q color difference signals that match the original EIA and SMPTE patterns. The -I signal appears as a bluish-gray bar and the Q signal appears as a purple bar on a TV monitor. The bars are separated by a white (+100 IRE) bar.
- The right side of the lower 25% of the image contains a narrow 12.5 IRE gray bar. Due to a hardware limitation on the 801GX, this portion of the pattern does not match the original EIA and SMPTE patterns. The original patterns had +3.5 (blacker than black) and +11.5 IRE bars separated by a +7.5 IRE (black) bar.
- The remaining central 8% of the image contains a row of chroma set bars. These bars are part of the SMPTE pattern but are not in the EIA pattern. The order of the alternating color and black bars matches those in the SMPTE pattern.

16.161.2 Test

Color video performance.

16.161.3 Purpose

This general purpose pattern can be used to check the video handling capabilities of most parts of a television system.

16.161.4 Method

When viewed on a TV screen, all of the upper color bars should be correct and in the order shown. The hue and intensity of each bar should be uniform over the entire bar.

The image can be used with a TV waveform analyzer to check the performance of a video system. The upper color bars, as they would appear on a waveform analyzer, are shown on a previous page.

16.161.5 Test

Color decoder performance.

16.161.6 Purpose

The image can used with a TV vectorscope to check for proper operation of a video color decoder. Vectorscope signatures of the upper and lower portions of the image using NTSC encoding can be found on the previous page.

16.161.7 Method

The vectorscope signature for the color bars should hit the target test point for each color on the vectorscope’s graticule. If you are using PAL encoded video, the signature will be similar to the one shown for the TVBar_75 test image.

The three “legs” of the vectorscope signature for the -I and Q color difference signals should match the Burst, -I and Q reference lines on the vectorscope’s graticule.

The following tests are based on the original SMPTE guideline:

16.161.8 Test

Visual chroma gain adjustment.

16.161.9 Method

To perform this test, you must have a way of turning off the red and green guns in the monitor under test. Turning off the red and green video components of the 801GX generator’s video output will not work for this test.

This test uses the upper and central color bars. Switch off the red and green guns on the monitor. This will produce four blue bars, separated by black bars. Adjust the chroma gain so that the brightness of each outer blue bar is uniform over the entire bar. The gain is correct when the bottom 10% of each bar is the same brightness as the rest of the bar.

16.161.10 Test

Visual chroma phase adjustment.

16.161.11 Method

In order to perform this test, you must have a way of turning off the red and green guns in the monitor under test. Turning off the red and green video components of the 801GX generator's video output will not work for this test.

This test uses the upper and central color bars. Switch off the red and green guns on the monitor. This will produce four blue bars, separated by black bars. Adjust the chroma phase so that the brightness of each of the two central blue bars is uniform over the entire bar. The phase is correct when the bottom 10% of each bar is the same brightness as the rest of the bar.

16.161.12 Test

Visual black level adjustment.

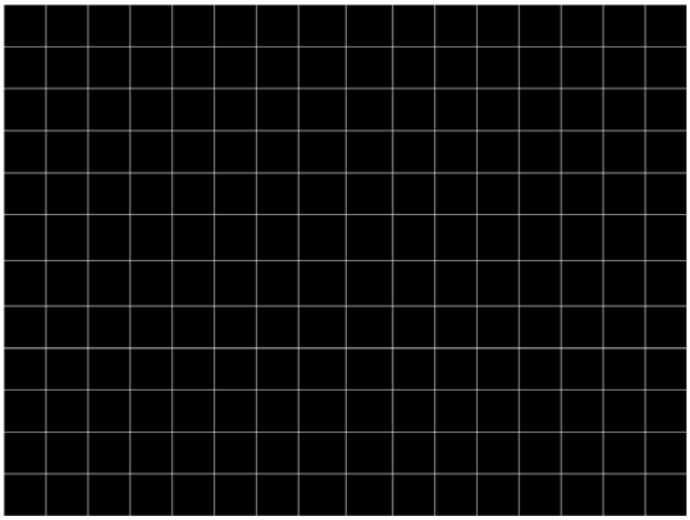
16.161.13 Method

This test uses the lower right hand portion of the image. Reduce the black level until the gray bar disappears. Slowly increase the black level until the bar just becomes clearly visible.

16.162 Sony6

16.162.1 Description

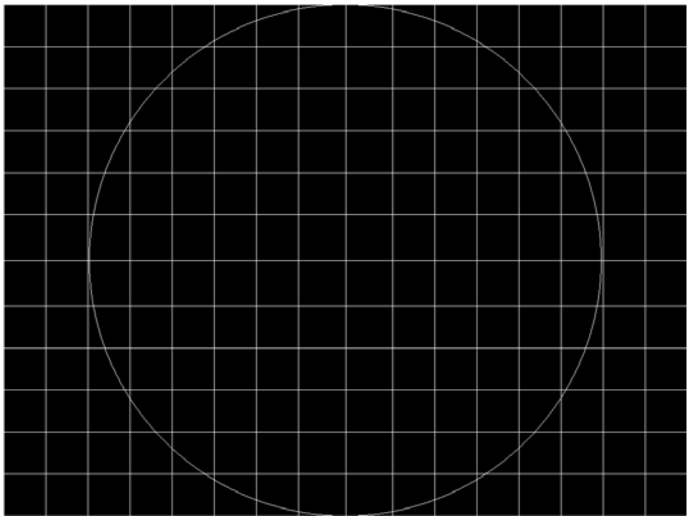
Special test image developed per customer specifications.



16.163 Sony6WLC

16.163.1 Description

Special test image developed per customer specifications.



16.164 sRGBflat

16.164.1 Description

For testing color response per Microsoft's WinColorKit standard. This standard was developed by Microsoft to standardize methods relating to the matching of colors appearing on various displays. There are 38 different versions of this image to support this feature.

When selected, a flat image appears with a color that is remembered from the last time the image was set up. The example below shows version 8 (Red1) of the sRGBflat image:

A small label in the upper left corner of the image indicates the Microsoft name for the color that is currently being displayed (for example, "sRGB-Gray5"). Note that some of the names that appear conflict with generator color names (for example, "sRGB-Gray5" is not the same as the generator color "Gray5").

After pressing the Contents key and then the Options key. You then enable More and use the +/- increment keys to select up to 38 different versions of this image. Each image displays another WinColorKit color.

16.165 Staircase

16.165.1 Description

The active video area goes from full black at the left edge of the screen to full white at the right edge. There are sixteen (16) steps.

16.165.2 Test

Video gain linearity

16.165.3 Method

When viewed on a monitor’s screen, a black bar plus five (5) gray bars should be visible.

There should be no color shifts, and each of the bars should be uniform in color.

The image also can be used with an oscilloscope or TV waveform analyzer to check the gain linearity and gamma correction of a video system.

16.166 Strokes0, Strokes1

16.166.1 Description

This image may cited by some display manufacturers' test procedures. The Strokes0 version consists of multiple groups of separated red, green and blue horizontal lines drawn on a black background. The Strokes1 version consists of multiple groups of separated red, green and blue diagonal lines drawn on a black background.

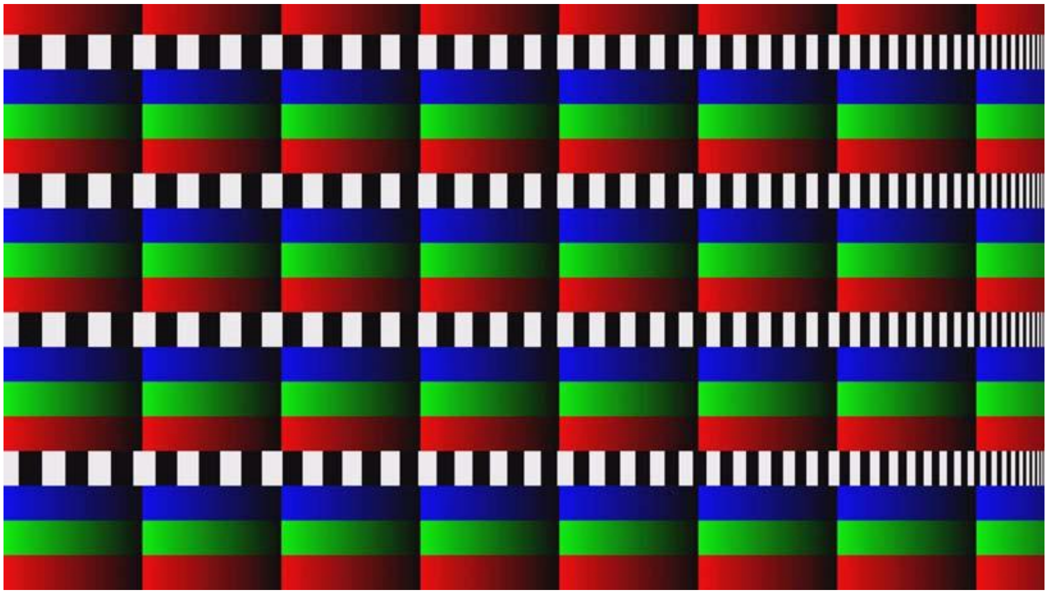
16.166.2 Purpose

These images are special-purpose test patterns used in test and alignment procedures specified by some display manufacturers.

16.167 TAARamp

16.167.1 Description

The TAARamp pattern is shown below.



16.168 Taffeta

16.168.1 Description

16.169 Text_9, Text_9T, Text_11, Text_12T, Text_16

16.169.1 Description

In the primary versions, the screen is filled with random paragraphs of white text on a black background. The amount of text is determined by the size of the font used and the horizontal and vertical resolution of the format. The Text_16 image uses a larger font than the Text_9 image. The secondary versions use black text on a white background.

The primary version of the Text_9 image is shown below.

16.169.2 Test

Word processor simulation

16.169.3 Purpose

If your monitor is used in word processor workstations or other applications that call for large amounts of text to be displayed, you can use this image to simulate actual user conditions.

16.169.4 Method

Select a suitable font size and text color. Adjust your monitor's brightness and contrast controls to obtain the best image. The characters in all areas of the display should be well formed and in focus.

16.170 TextFlat

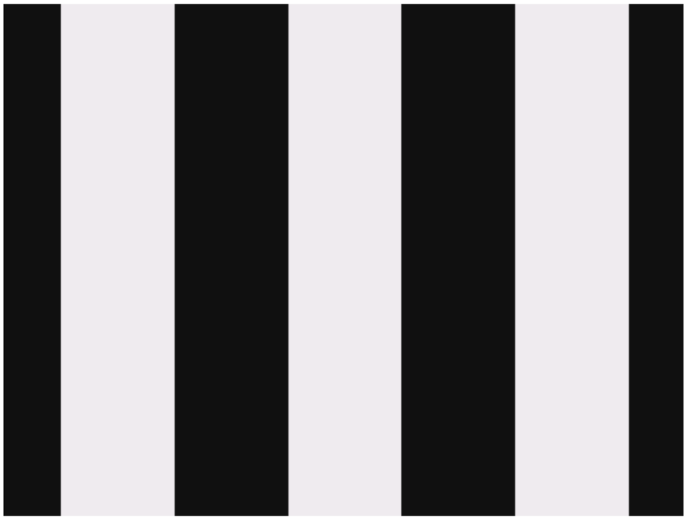
16.170.1 Description

In the primary versions, the screen is filled with random paragraphs of white text on a black background. The amount of text is determined by the size of the font used and the horizontal and vertical resolution of the format. The Text_16 image uses a larger font than the Text_9 image. The secondary versions use black text on a white background.

16.171 ThreeBar

16.171.1 Description

The screen is filled three vertical white bars on black background.



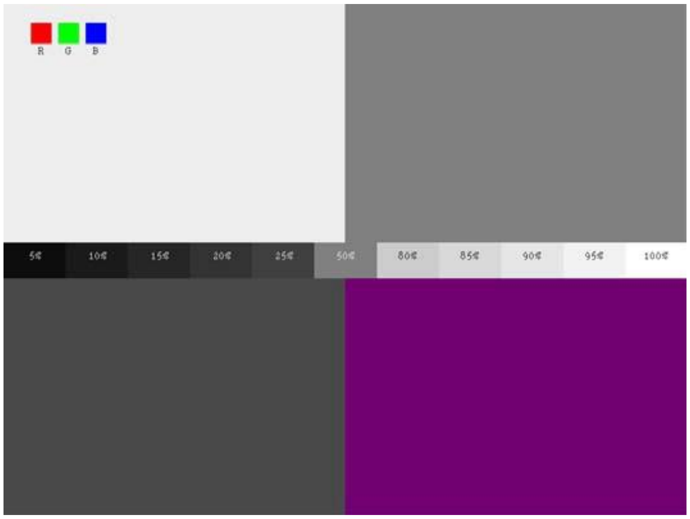
16.172 TintAlign

16.172.1 Description

16.173 Toshiba

16.173.1 Description

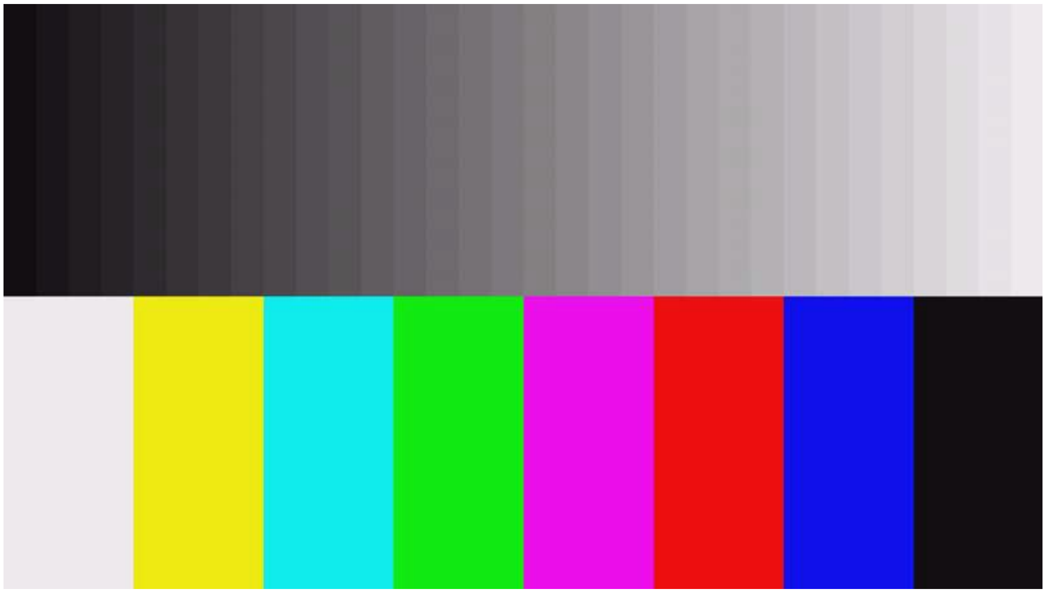
Special test image developed per customer specifications. There are two sub images, the secondary image is depicted below. The top half of the image has three small boxes (red, green, blue) with the upper left half at 92.7% luminence and the upper right half at 50% luminence. There is a series of 11 small boxes of increasing luminence left to right with the luminence identified in text. The lower left quarter of the image is 28.5% luminence and the lower right is magenta at 44.3 IRE.



16.174 TPVAOC1 and TPVAOC2

16.174.1 Description

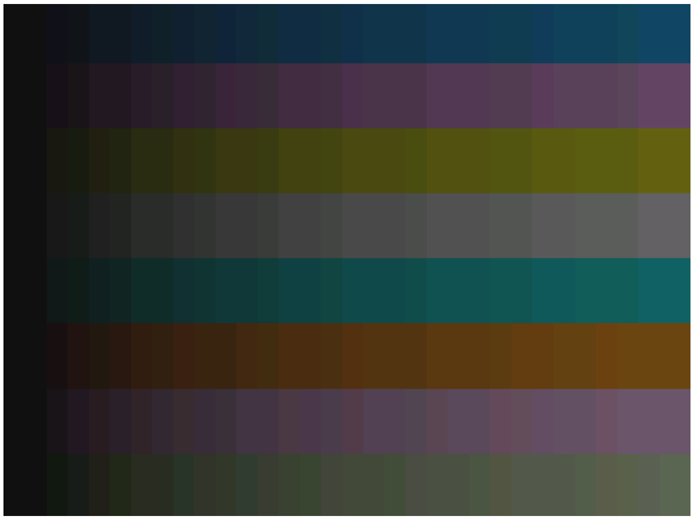
The TPVAOC1 pattern is shown below.



16.175 TTECorp1

16.175.1 Description

Special test image developed per customer specifications.

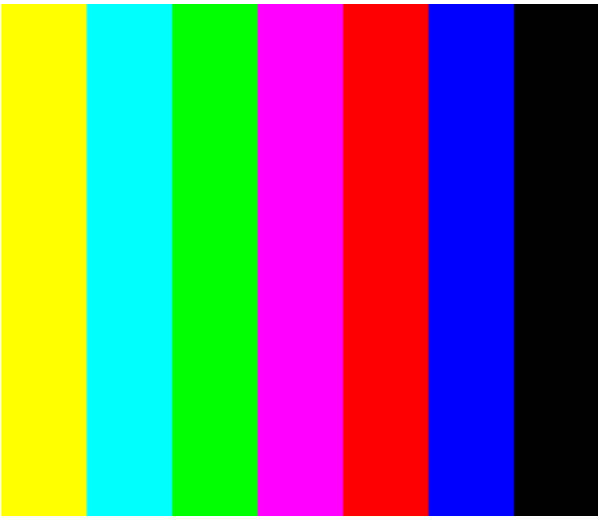


16.176 TVBar100 & TVBar_75 (TV formats only)

16.176.1 Description

The image consists of seven vertical bars that fill the entire active video area. The color and order of the bars is shown in the figure below. The TVBar100 image has a peak video level of 100 IRE and the TVBar_75 image has a peak video level of 75 IRE.

The TVBar100 image is shown below.



16.176.2 Test

Color video performance.

16.176.3 Purpose

This general purpose pattern can be used to check the video handling capabilities of most parts of a television system.

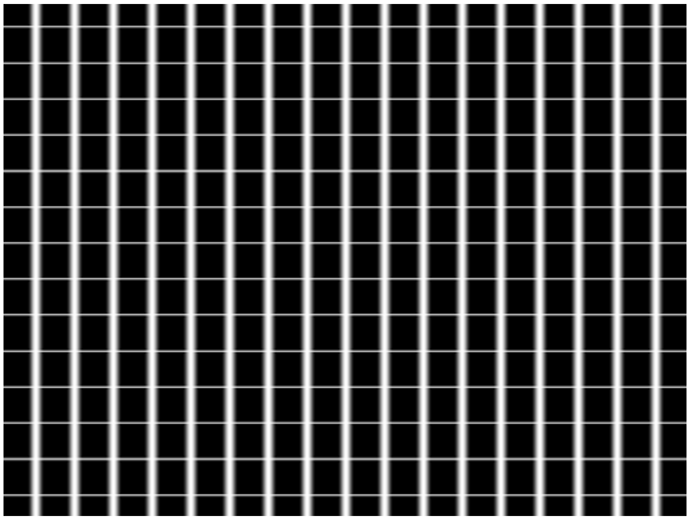
16.176.4 Method

When viewed on a TV screen, all of the colors should be correct and in the order shown.

The hue and intensity of each bar should be uniform over the entire bar.

The image can be used with a TV waveform analyzer to check the performance of a video system. Individual scan lines of each image, as they would appear on a waveform analyzer, are shown on the following page.

The image is quite effective when used with a TV vectorscope to see how a video system handles an encoded color signal.The image consists of a white crosshatch on a black background. The lines form square boxes when the display’s active video area has a 4:3 aspect ratio. The vertical lines are made using sine-squared (2 T) pulses (T = 125 nSec for NTSC and T = 100 nSec for PAL).



16.176.5 Test

Convergence adjustment.

16.176.6 Purpose

To accurately produce an image on a color monitor, the three electron beams in the CRT must meet (converge) at the same location at the same time. Lines displayed on a mis-converged monitor will appear as several multi-colored lines, and the transitions between different colored areas will contain “fringes” of other colors.

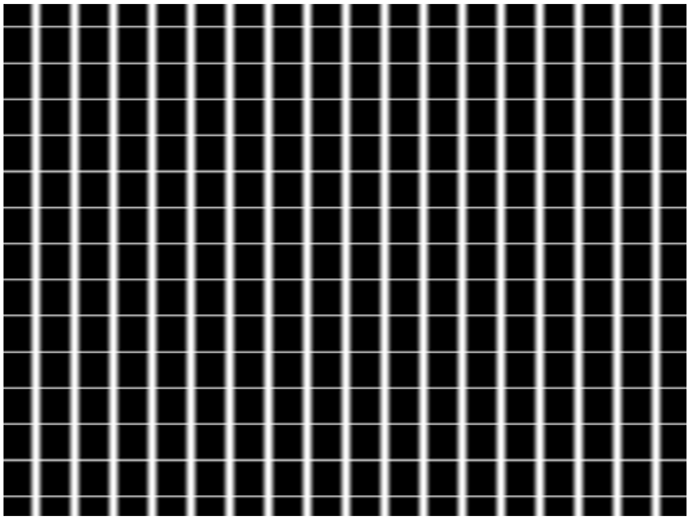
16.176.7 Method

The convergence adjustments of most color monitors can be divided into two main categories. The first set of adjustments, usually called “Static Convergence,” calls for aligning the three beams in the center of the display. This method involves turning on all three guns and adjusting the various magnets on the convergence assembly to produce all white lines and dots in the center of the display. The convergence assembly is located on the neck of the CRT. Different monitors and CRT types may each require their own magnet adjustment sequence.

After the center of the display is properly converged, the outer areas can be adjusted by using the monitor’s “Dynamic Convergence” controls. The number of controls, the area of the screen that they affect and their adjustment procedure is dependent upon the monitor under test.

16.176.8 Test

Sweep linearity adjustment.



16.176.9 Purpose

To present an undistorted display, the horizontal and vertical sweeps of the electron beam across the face of the CRT should be at uniform speeds. Any non-uniformity in the sweep will cause portions of an image to be stretched while other portions will be compressed. Non-linearity in a monitor can show up in several ways. It may be present across the entire screen, a large portion of the screen, or it may be localized in a very small area.

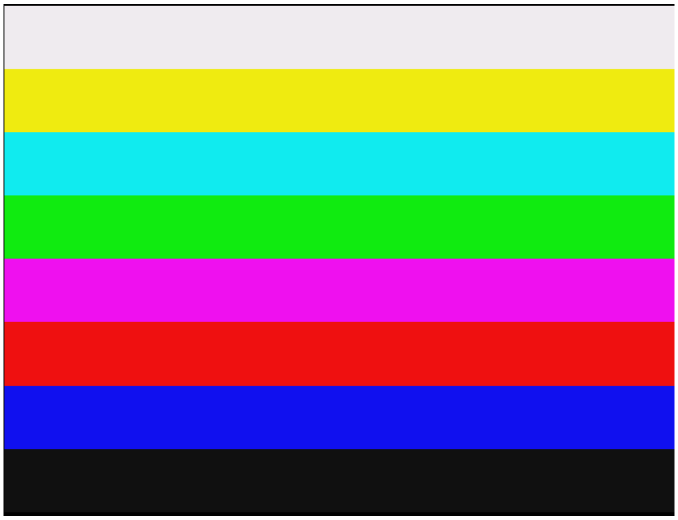
16.176.10 Method

Adjust the display's linearity controls so that all of the boxes in the crosshatch are identical in size. You can measure the boxes with a ruler or with a gauge made for the monitor under test. Any deviation should be within your specification limits.

16.177 TVBarH

16.177.1 Description

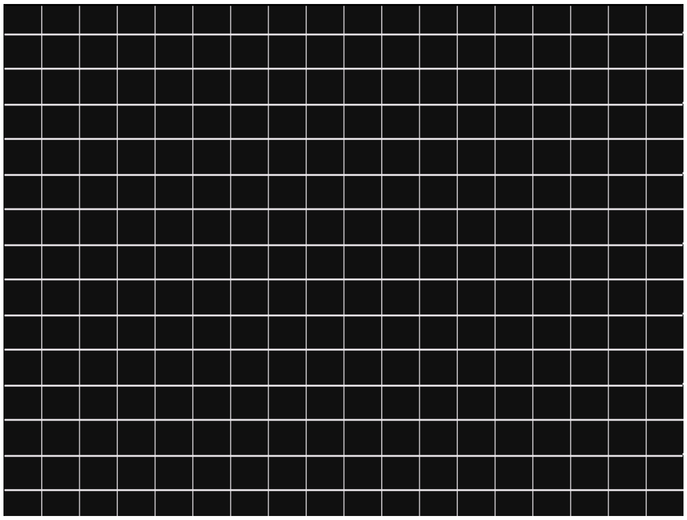
The image consists of seven horizontal bars that fill the entire active video area. The color and order of the bars is shown in the figure below.



16.178 TVHatch

16.178.1 Description

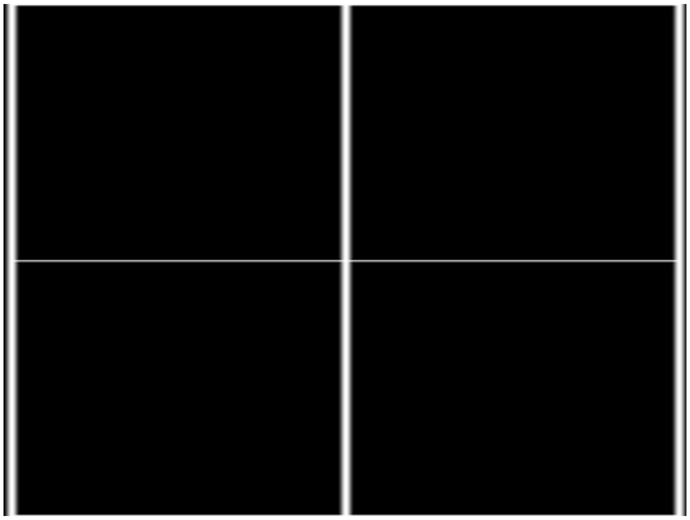
Primary version of TVHatch is shown below.



16.179 TVoutLin

16.179.1 Description

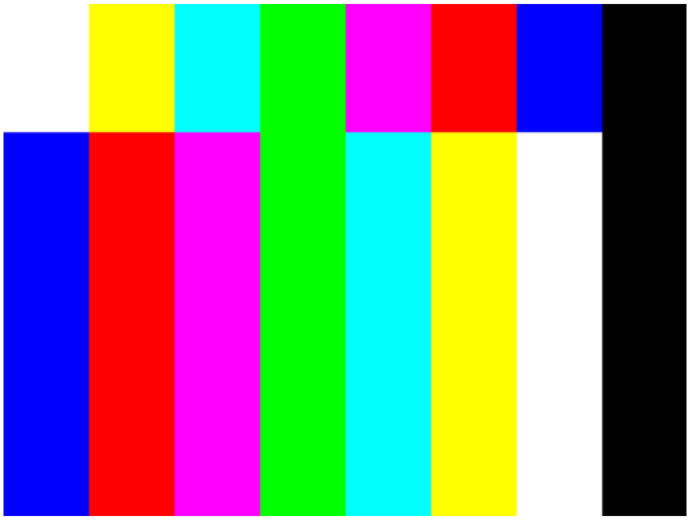
Equivalent to Outline1 image but it uses anti-aliasing for vertical bars and double horizontal lines, which reduces flickering.



16.180 TVSplBar

16.180.1 Description

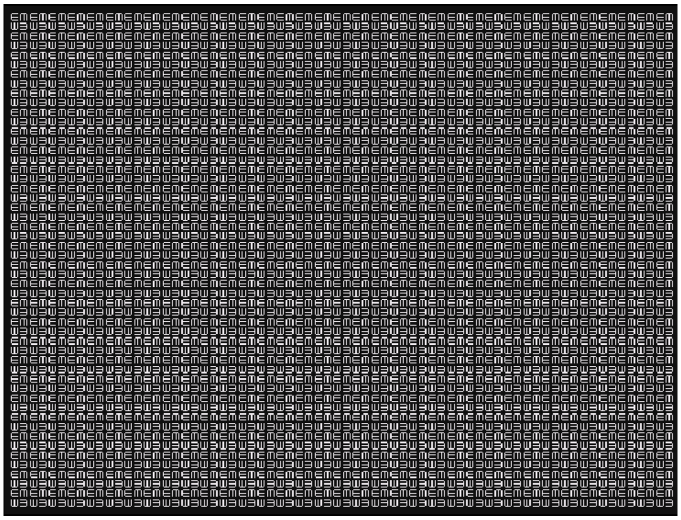
Special test image developed per customer specifications.



16.181 WHT_EM, WHT_EM+

16.181.1 Description

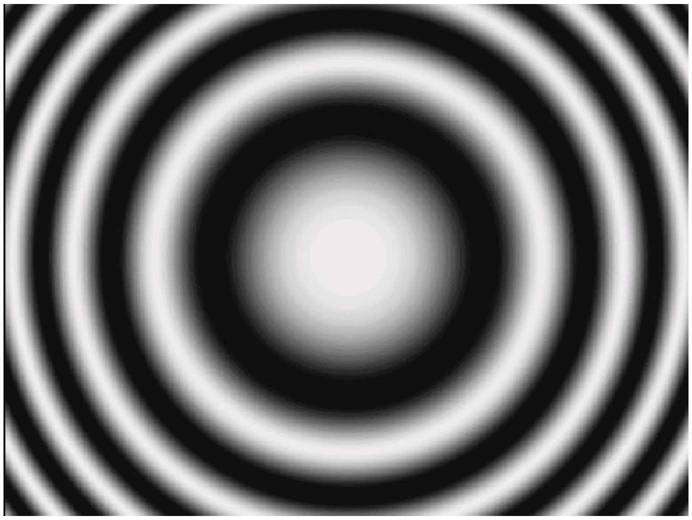
In the primary version, the screen is filled with white (WHT) EM character blocks on a black background.



16.182 ZonePlt

16.182.1 Description

A zone plate is a radially symmetric pattern with low frequencies in the middle and high frequencies near the edge. It is useful for experimenting with frequency- and direction-sensitive filtering and also for testing the anti-aliasing capability of image resizing methods.



END OF USER GUIDE