TELEDYNE LECROY
Everywhereyoulook™
quantumdata

quantumdata™ M42d DisplayPort 2.0 Video Analyzer/Generator

Full 80Gb/s Link Rate Functional and Compliance Tester

Key Features

- Equipped with both DP standard and USB-C ports for Tx and Rx functions
- Test DP sources 10Gb/s & 13.5Gb/s (20Gb/s future) lane rates at the new 128b/132b line coding
- View incoming video and metadata—including DSC compressed--from a source device
- Capture and decode incoming video, protocol, and control packets including Display Stream Compression (DSC)
- Run functional tests on displays and monitors at UHBR lane rates with large format and test pattern library
- Configure link training parameters to test display's handling of link training
- Generate Display Stream Compression (DSC), select patterns and configure slices and video parameters
- View and edit EDID and DPCD registers
- Monitor Aux Channel transactions while emulating a DP 1.4 or DP 2.0 source or sink
- Passively monitor the Main Link and Aux Channel between a source & display at UHBR lane rates
- Panel Replay testing for sources and sinks (future)
- NEW! LTTPR device emulation in Transparent mode for testing LTTPR-capable source devices at 8b/10b line code for lane rates up to HBR3 (support for LTTPR in non-transparent mode for 128b/132b at UHBR rates is coming soon)
- View Power Delivery (PD) negotiations for USB-C DP Alt Mode
- NEW! DP 2.0 Link Layer compliance tests on source devices up to 13.5Gb/s per lane
- 1.4 Link Layer compliance tests on sources and sinks up to 8.1Gb/s per lane
- Run DP 1.4 Forward Error Correction (FEC) and Display Stream Compression (DSC) compliance tests for sources and sinks
- Run HDCP 2.2/3 compliance tests on DisplayPort sources, sinks and branch devices
- Run audio tests using programmable LPCM sine wave audio tones
- Run tests on embedded DisplayPort (eDP) 1.4b sources and panels using fast link training, ALPM & backlight control

The Teledyne LeCroy quantumdata M42d Video Analyzer/Generator provides an unprecedented combination of functional and compliance testing for video, audio and protocol of DisplayPort 2.0 and DisplayPort 1.4. The M42d supports legacy DisplayPort lane rates of 1.62, 2.7, 5.4, 8.1 Gb/s and the new DP 2.0 higher speed lane rates and new line coding—128b/132b—of 10.0 & 13.5Gb/s (20.0Gb/s future) data rates up to 4 lanes. The protocol analyzer provides a snapshot status view and deep analysis using captures of incoming DisplayPort 2.0 (and DP 1.4) streams from source devices including DSC/FEC compressed streams. The M42d's video generator can be used for testing displays, USB-C adapters, extenders, etc. The video generator offers a large library of standard video timings and test patterns necessary for testing next generation high resolution displays.

The M42d supports a full suite of DP 1.4 link layer, forward error correction (FEC) and display stream compression (DSC) compliance tests for both sources and sinks. (Compliance tests for DP 2.0 are planned for the future.)

The Passive Probe feature (future), based on Teledyne LeCroy's cutting-edge T.A.P.4™ technology, enables full monitoring of the DisplayPort Main Link and the Aux Channel between two DisplayPort devices up to 13.5Gb/s (with 20 Gb/s lane rates future).

Operation

The M42d supports generation and analysis of the DisplayPort data streams through the user-friendly ATP Manager. The M42d can be controlled through the ATP Manager operated either via a laptop connected to the M42d RJ45 LAN port or through a USB keyboard and mouse and a connected UHD HDMI admin display.

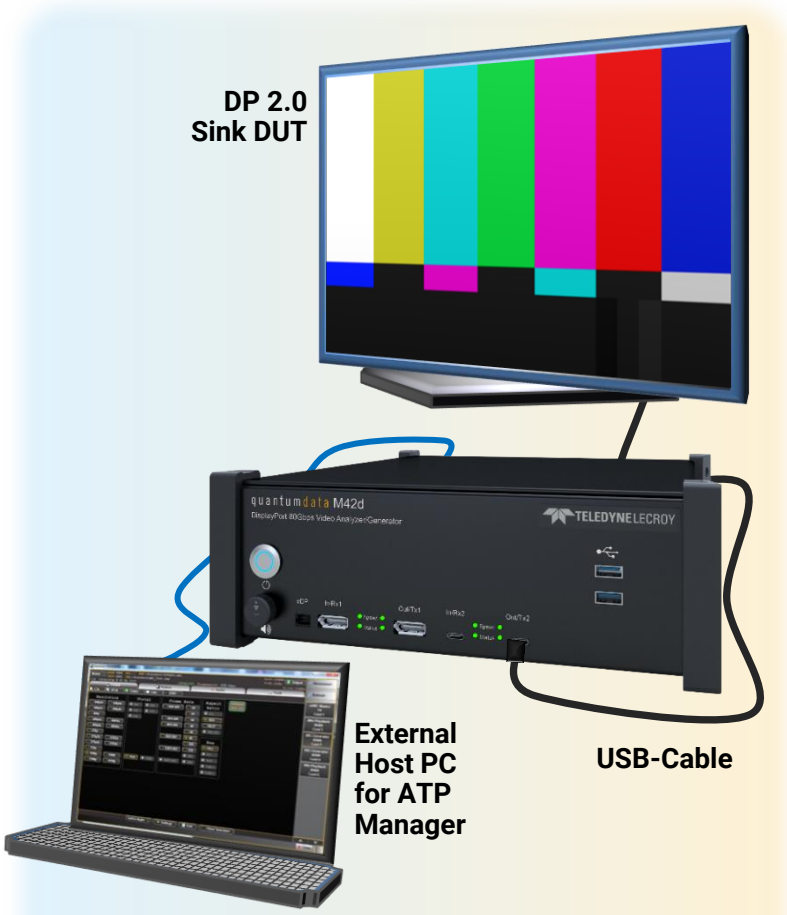
M42d Video Analyzer Generator

Keyboard & mouse for M42d ATP Manager Control

DISPLAY TESTS – VIDEO TESTING

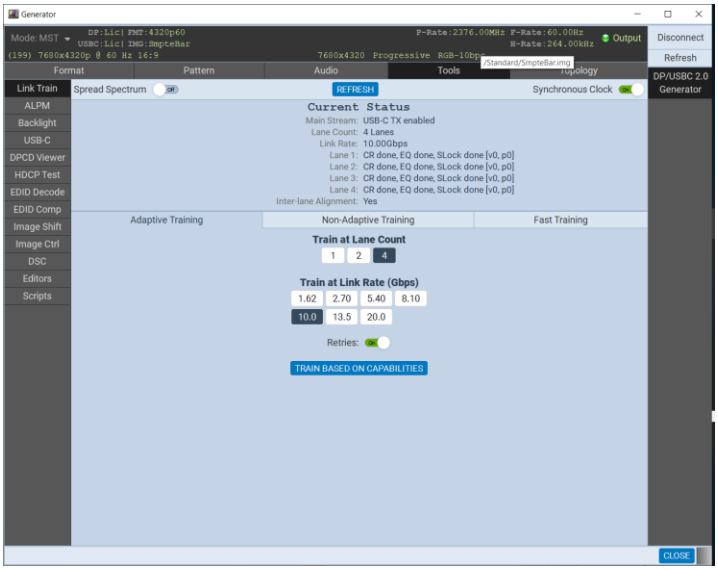
Video Generation

The M42d supports video and audio functional testing at UHBR lane rates up on 1, 2 and 4 lanes to support high resolution formats. The M42d has an extensive set of video formats and library of test patterns. You can specify lane configurations for link training (below).

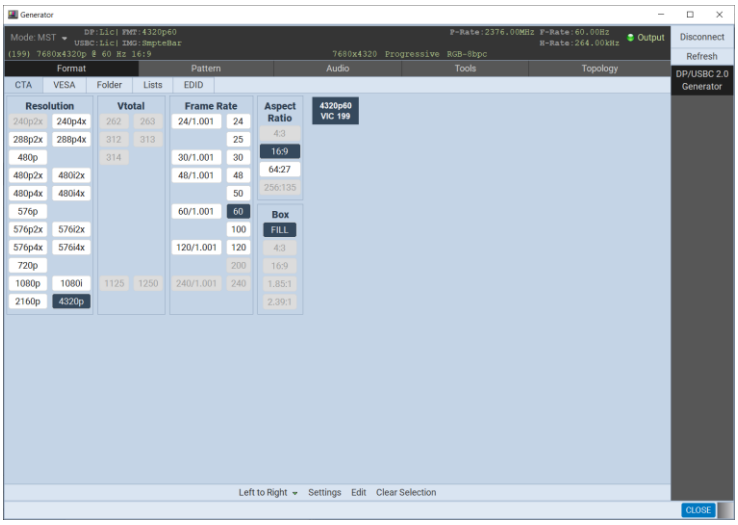


Display (Sink) Test Setup

Link Training Control and Configuration



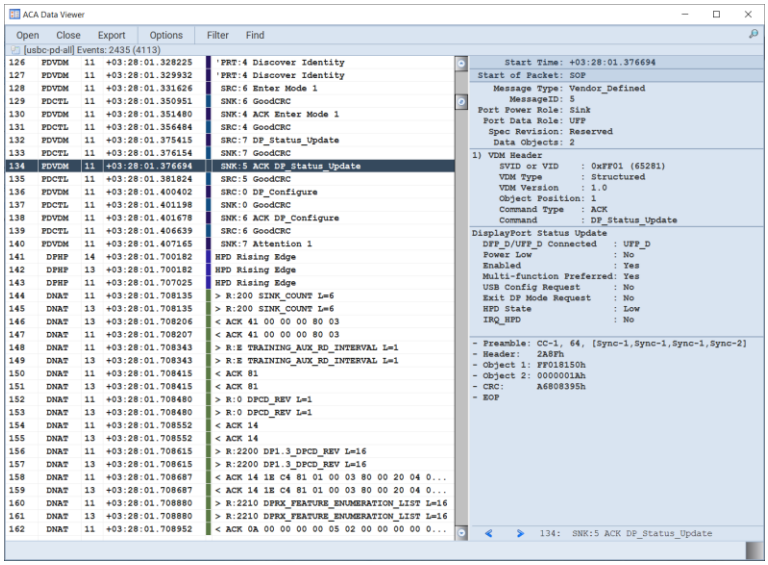
Format Selection



Aux Channel Analyzer (ACA)

The M42d 's Auxiliary Channel Analyzer (ACA) feature enables you to monitor the DP Aux Channel for link training, MST negotiations, HDCP transactions, DP Alt Mode PD negotiations and EDID exchanges between the M42d Rx port and a connected source. The ACA logs these events and assigns precise timestamps to them. You can view the details of each transaction. These ACA logs can be saved and disseminated for further analysis by colleagues and other subject matter experts.

Aux Channel Analyzer



Link Training Control and Configuration

The M41d 's link training control feature enables you to configure the link training parameters. You can set limits on the lane count and link rate and allow the link training engine to establish link training based on those limitations or you can force link training parameters—lane count, link rate, voltage swing, pre-emphasis.

SOURCE TESTS – VIDEO & PROTOCOL ANALYSIS

Receiver - Basic & Capture Analyzer

The M42d 's Basic Analyzer enables you to view the incoming video, lanes and link rate, timing, colorimetry and various other metadata in real time at a glance. The Basic Analyzer mode provides a basic confidence test to verify that the incoming video is essentially correct. The Rx port emulates any EDID on to test a source devices handling of various EDIDs. You can also configure DPCD registers for emulating on the DP Rx port using the DPCD Editor.

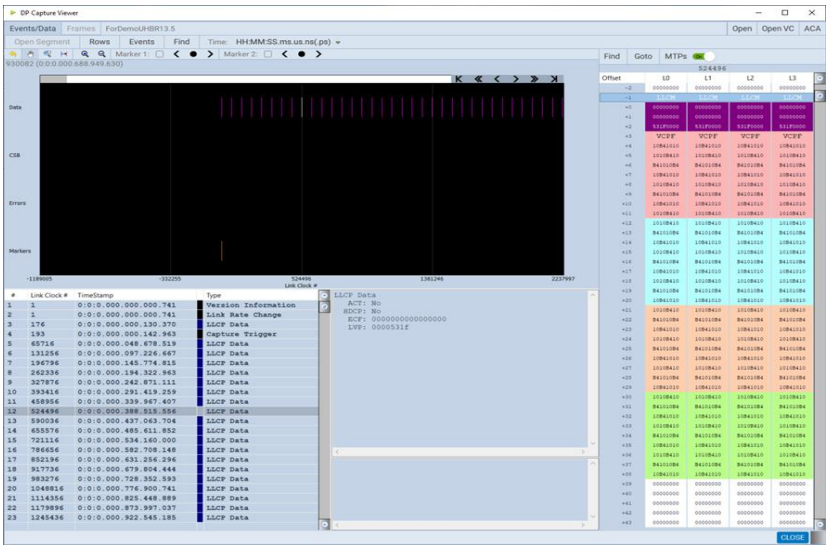
Source Test Setup

Receiver – Basic Analysis

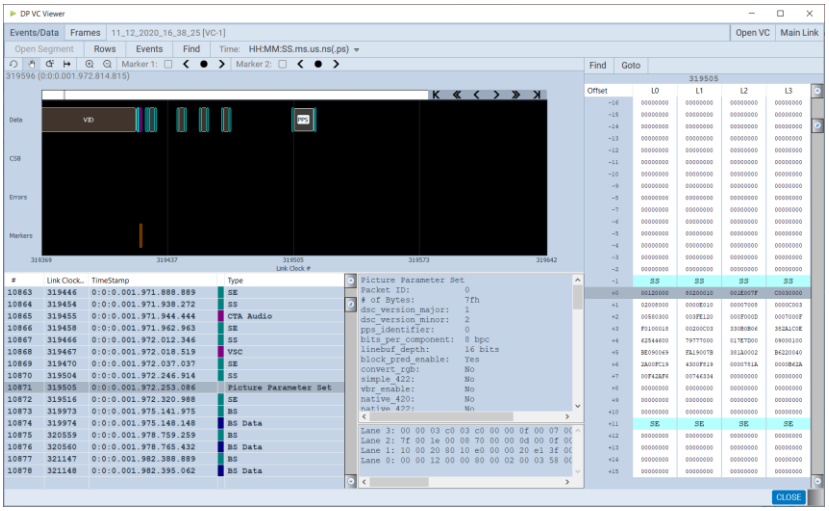
Receiver - Capture Analyzer

The deep Capture Analyzer enables you to view the protocol data of the high-speed link (shown below) and the underlying virtual channels (shown below). The Capture Analyzer provide deep insight into the data, control symbols, video, metadata and protocol data.

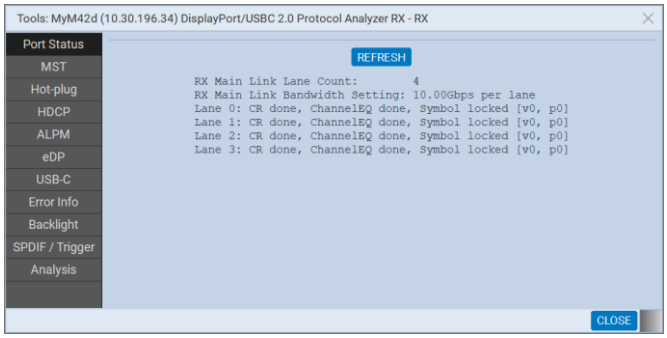
Capture Analysis (Main Link) – 13.5G Link



Capture Analysis – Virtual Channels



Link Training Status



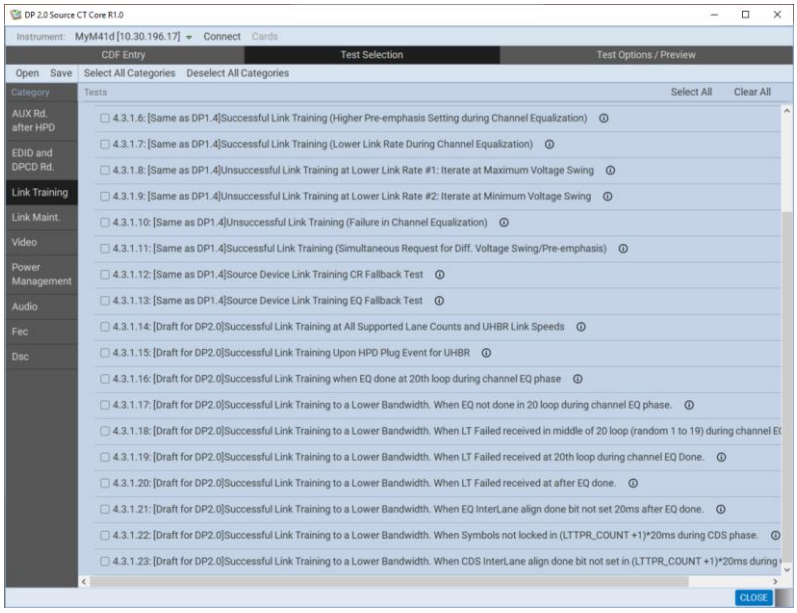
DP 1.4/2.0 NEW! LINK LAYER SOURCE COMPLIANCE

Source Link Layer Compliance

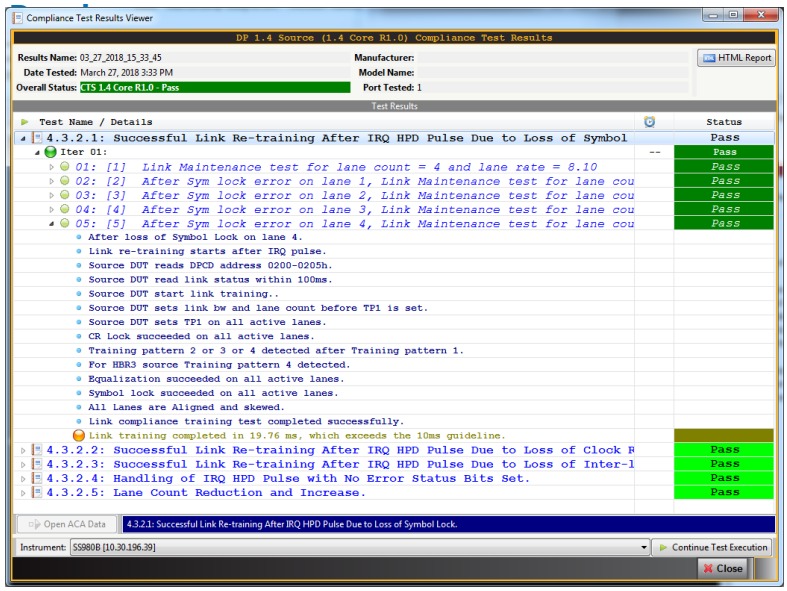
The DP source link layer compliance are ideal for self-testing or pre-testing your HBR3 or UHBR-capable DisplayPort source product prior to submission to an Authorized Test Center for approval. Pre-testing provides added assurance that your product will pass at the ATC when submitted. The compliance tests enable you to view the captured data and detailed test results which help pinpoint the cause of compliance test failures. You can link to the aux channel traces in the Aux Channel Analyzer (ACA) to view the root cause of failures.

Source Test Setup

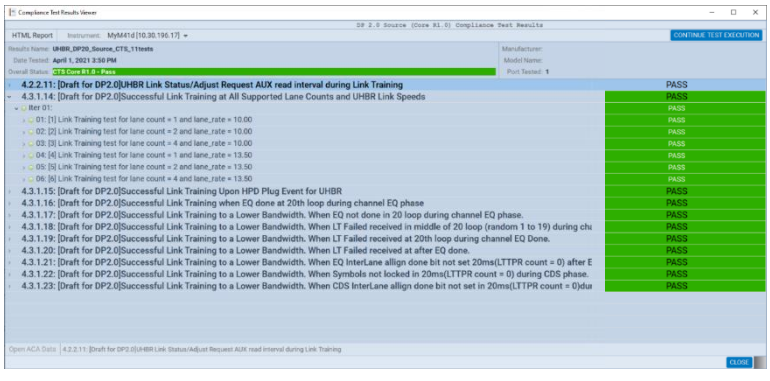
DP 1.4/2.0 Source Link Layer Compliance - Test Selection



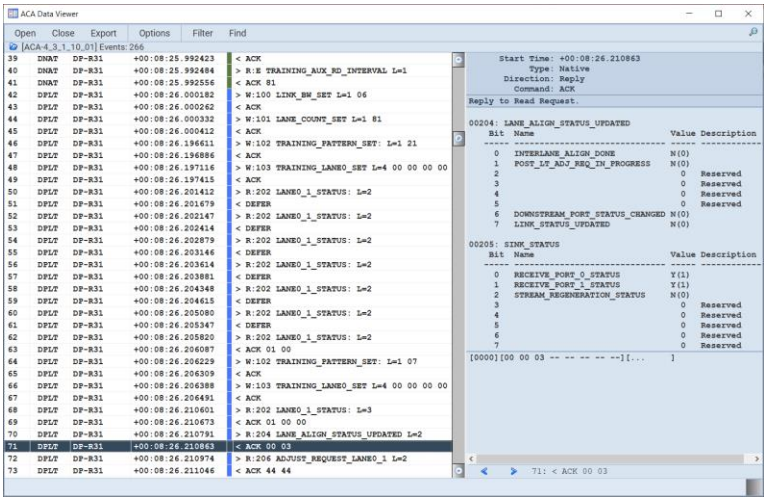
DP 1.4 Source Link Layer Compliance Test



DP 2.0 Source Link Layer Compliance Test Results



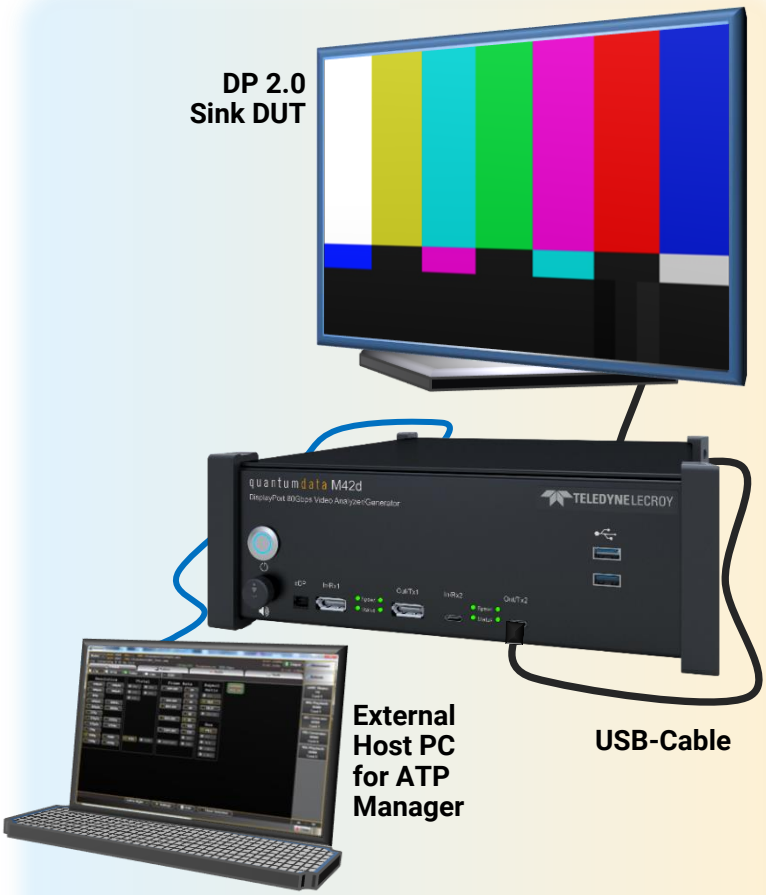
DP Aux Channel Traces – From LLC Test



DP 1.4 LINK LAYER SINK COMPLIANCE

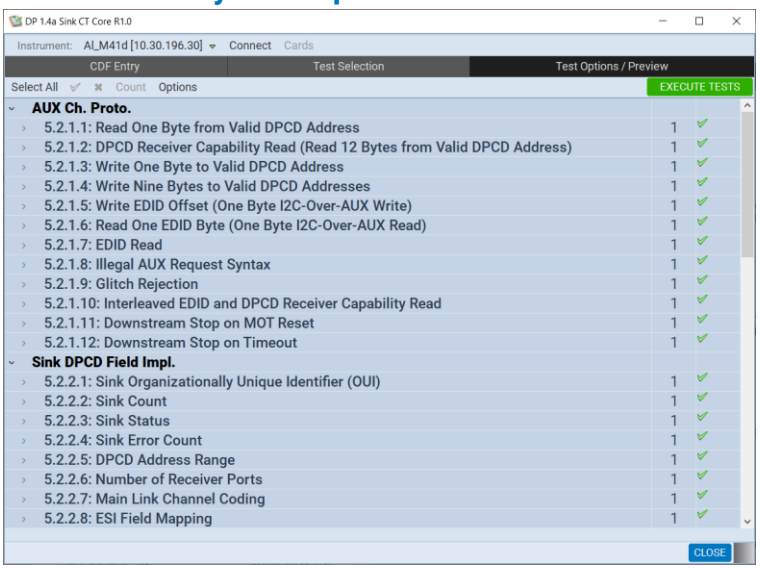
Sink Link Layer & EDID Compliance

The DP sink (display) and EDID/DisplayID and Link Layer compliance tests are ideal for pre-testing or self-testing (where permitted) your DisplayPort display product prior to submission to an Authorized Test Center for approval. Pre-testing provides added assurance that your product will pass at the ATC when submitted. The compliance tests (below right) enable you to view the captured data and detailed test results which help pinpoint the cause of compliance test failures. The link layer compliance test suite now includes tests for forward error correction (FEC). You can link to the aux channel traces in the Aux Channel Analyzer (ACA) to view the root cause of failures (below).

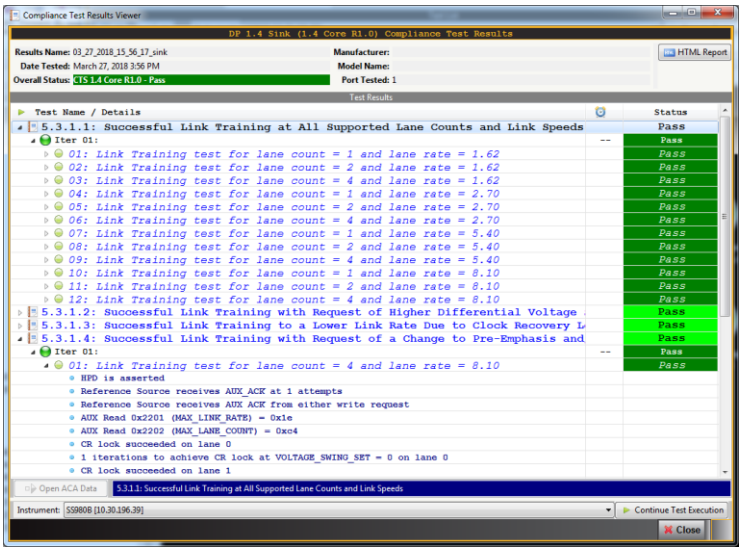


Display (Sink) Test Setup

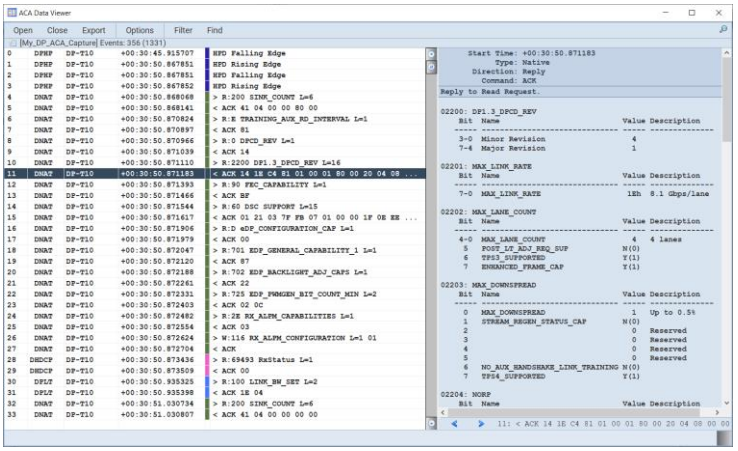
DP 1.4 Link Layer Compliance - Test Selection



DP 1.4 Link Layer Compliance - Test Results



DP Aux Channel Traces – From LLC Test



SPECIFICATIONS

DisplayPort 2.0 Capabilities

Version	DisplayPort 2.0 (and DP 1.4)
Standard Video Formats	VESA, CTA
Protocols and Line Coding	DP, DSC, FEC, MST, SSC, SDP with 128b/132b encoding (LTTPR, Panel Replay future)
Video Data Rates	1.62, 2.7, 5.4, 8.1, 10.0 Gb/s & 13.5 (20 Gb/s future); 1, 2, 4 Lanes
Color Depths	8, 10, 12, 16 bits (6 bits future)
Video Encoding	RGB, YCbCr
Video Sampling Modes	4:4:4, 4:2:2, (4:2:0 future)
HDCP	Versions 1.3 and 2.2/3
Audio	8 Channel LPCM programmable sine wave (future)
Capture memory	8 GBytes

Connectors - Front

DP Standard	Tx (1) DP Full-Sized; Rx (1) DP Full-Sized
USB-C	Tx (1) USB-C with DP Alt Mode; Rx (1) USB-C with DP Alt Mode
eDP Header	Pins to access eDP Tx backlight controls
USB (2)	For connecting keyboard and mouse for ATP Manager control & external storage media

Connectors - Back

HDMI - Admin Connector	HDMI 2.0 Port for external monitor for ATP Manager GUI
USB (2); USB-C (2)	Keyboard / mouse connected to USB ports to control ATP Manager on external display connected to Admin HDMI 2.0 port
RJ45 E1	For admin control over LAN from computer running ATP Manager
Cross Sync connector	Use for triggering a capture or for a capture event to trigger an oscilloscope
All other connectors	Not used

Physical / Electrical / Admin

Power	100-240 VAC, 50-60 Hz, 200 Watts
Weight	7.6 LBS; 5.057 Kg
Size	Height: 3.44 in. (8.74 cm) Width: 9.57 in. (24.30 cm) Depth: 10.94 in. (27.79 cm)
Rack mountable	2 RU mounts in 19 inch rack with rack mounting brackets
Internal speaker	Speaker with volume control for monitoring incoming LPCM audio
Command Line Control	Ethernet (RJ-45) for external GUI
System Control	Either through External PC connected over LAN to Ethernet RJ45 or:
	Keyboard / mouse to control external 4K UHDTV at Admin HDMI 2.0 port
Environmental	Operating Temp: 32 to 104 (F); 0 to 40 (C)

Ordering - Product Code	Description
00-00259	M42d UHBR Video Analyzer/Generator
00-00261	M42d HBR3 Video Analyzer/Generator
95-00221	M42d Upgrade 00-00261 to 00-00259 to enable UHBR rates
95-00222	Passive Probing Main Link and Aux Channel
95-00209	M41x Rack-mount Kit
95-00226	Source Enhanced Func test – Includes DSC, Capture Analysis & LTTPR/Panel Replay (future)
95-00225	Sink Enhanced Functional test - Includes DSC (LTTPR & Panel Replay future)
95-00232 NEW!	DP 2.0 Source Link Layer & MST (future) compliance (limited support currently) (req's 95-00226)
95-00213	DP 1.4 Source Link Layer compliance (requires 95-00226)
95-00216	DP 1.4 Sink Link Layer compliance (requires 95-00225)
95-00227	DP 1.4 Sink EDID compliance (requires 95-00225)
95-00215	DP 1.4 DSC/FEC Source functional test (requires 95-00226)
95-00218	DP 1.4 DSC/FEC Sink functional test (requires 95-00225)
95-00214	HDCP 2.2 Source compliance (requires 95-00226)
95-00217	HDCP 2.2 Sink compliance (requires 95-00225)
95-00212	Embedded DisplayPort (eDP)

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