quantumdata M42d Video Analyzer/Generator

November – 2020

TELEDYNE LECROY
Everywhereyoulook™

quantumdata Product Family…Our Mission:

Help silicon and product developers bring their next-generation video solutions to market—faster, without interoperability problems and at reduced cost

Our solutions quicken Time-to-Insight

TIME TO INSIGHT™

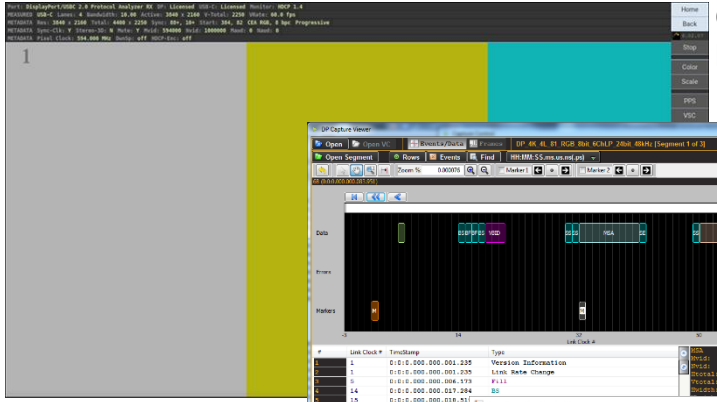
M42d Video Analyzer/Generator – Features and Functions

- Provides Protocol Analysis and Video Generation for DisplayPort 2.0 source and sink testing through standard DP ports and USB-C ports for DP Alt Mode.
- Enables viewing of incoming video and essential video and timing parameters.
- Protocol Capture Analyzer provides deep insight of the DP 2.0 video, audio, metadata, control data, and symbol data including DSC/FEC compression.
- Supports DP 1.4 Link Layer compliance tests for DP sources and sinks. Includes DSC and FEC compliance testing. DisplayPort 2.0 compliance testing planned for future release.
- Video generator outputs user-specified link configurations up to 8.1Gb/s rates for DP 1.4 and UHBR rates for DP 2.0 on four (4) lanes.
- Supports DCP-approved HDCP 2.2/3 source, sink and repeater compliance testing.
- Supports passive monitoring of the DisplayPort Aux Channel and Main Link at UHBR lane rates.
- Advanced Features such as Panel Replay and LTTPR are planned for future releases.

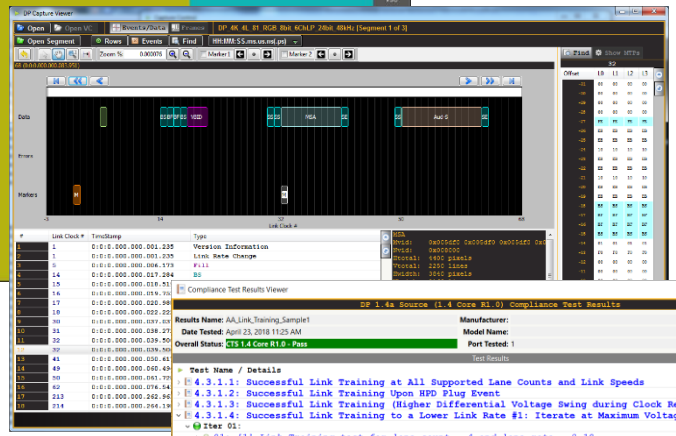
What is Time-to-Insight?

TIME TO INSIGHT™

- Time-to-Insight **saves time and money**. It involves the following:
  - **Quick Insight:** Provides at-a-glance information—insight—into the basic functioning of an DisplayPort video device or system.
  - **Deep Insight:** Provides full visibility—insight—into the low level protocol to verify the proper functioning of an DisplayPort device to improve interoperability.
  - **Compliance Tests:** Provides required test suites for DisplayPort Logo program.

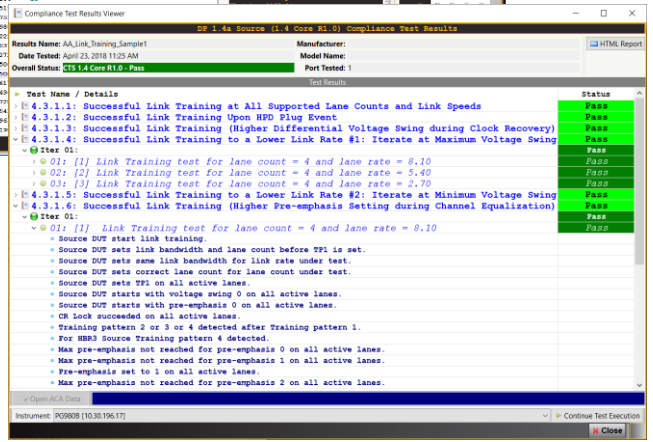


Quick Insight



Deep Insight

M42d Video Analyzer/ Generator



Compliance

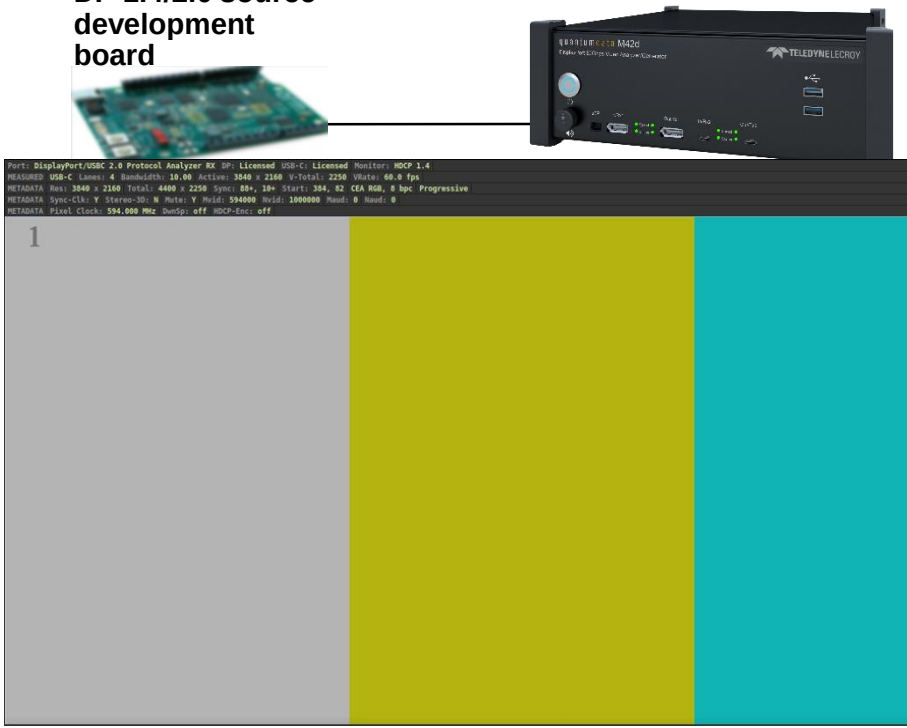
Quick Insight – Example 1

TIME TO INSIGHT™

- Quick Insight Solutions Include:
  - Basic analysis views of incoming videos streams.
  - Essential status information on dashboards, and status panels.
  - Device emulation of sources and sinks (displays).
- A Few Examples:
  - DisplayPort Receiver view w/ status bar at top. Shows incoming video and metadata from a source device.

DP 1.4/2.0 source development board

M42d Video Analyzer/Generator



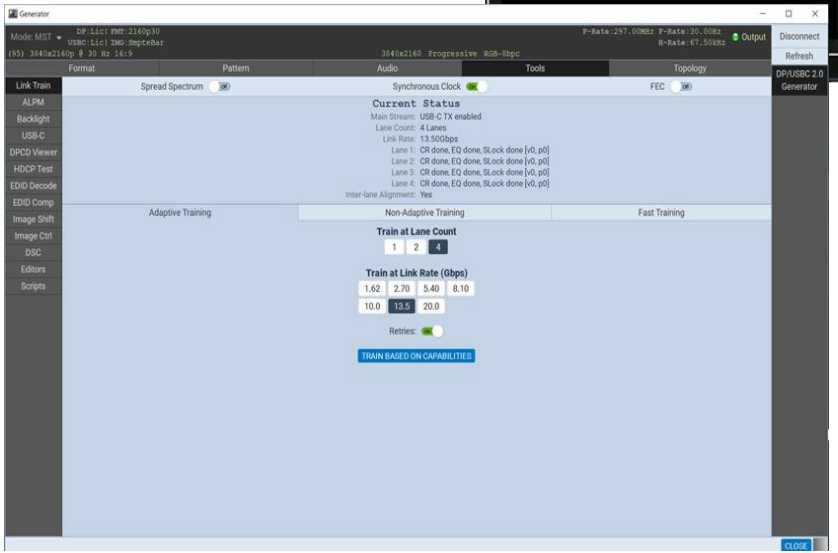
Quick Insight – Example 2

TIME TO INSIGHT™

- Quick Insight Solutions Include:
  - Real Time analysis views of incoming videos streams.
  - Essential status information on dashboards, and status panels.
  - Device emulation of sources and sinks (displays).
- A Few Examples:
  - DisplayPort link training control & status with connected display.

M42d Video Analyzer/Generator

DisplayPort Display



Quick Insight – Example 3

TIME TO INSIGHT™

- Quick Insight Solutions Include:
  - Real Time analysis views of incoming videos streams.
  - Essential status information on dashboards, and status panels.
  - Device emulation of sources and sinks (displays).
- A Few Examples:
  - DP EDID and DPCD data view of connected sink device.

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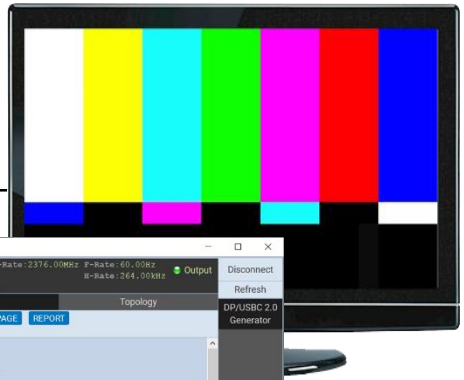
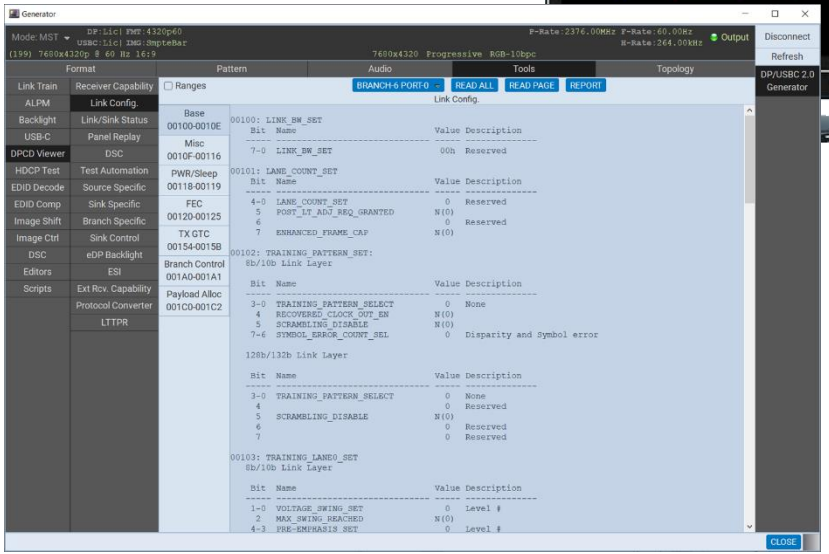
HDMI UHD TV

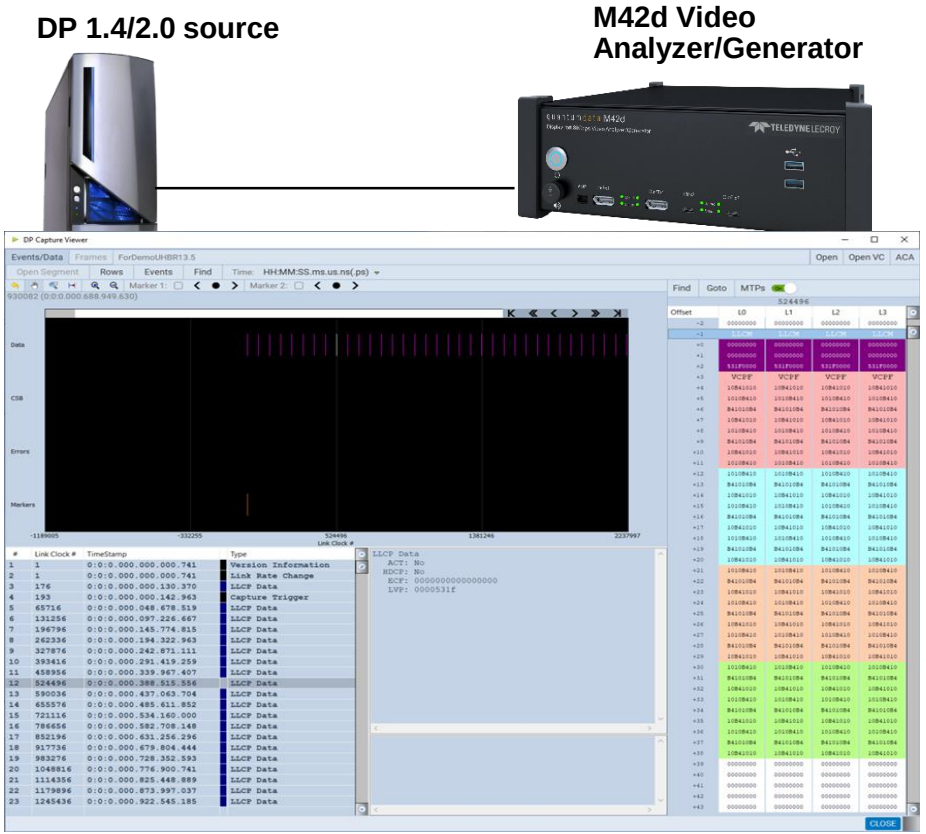




Deep Insight – Example 2a – DP 2.0 13.5G Capture

TIME TO INSIGHT™

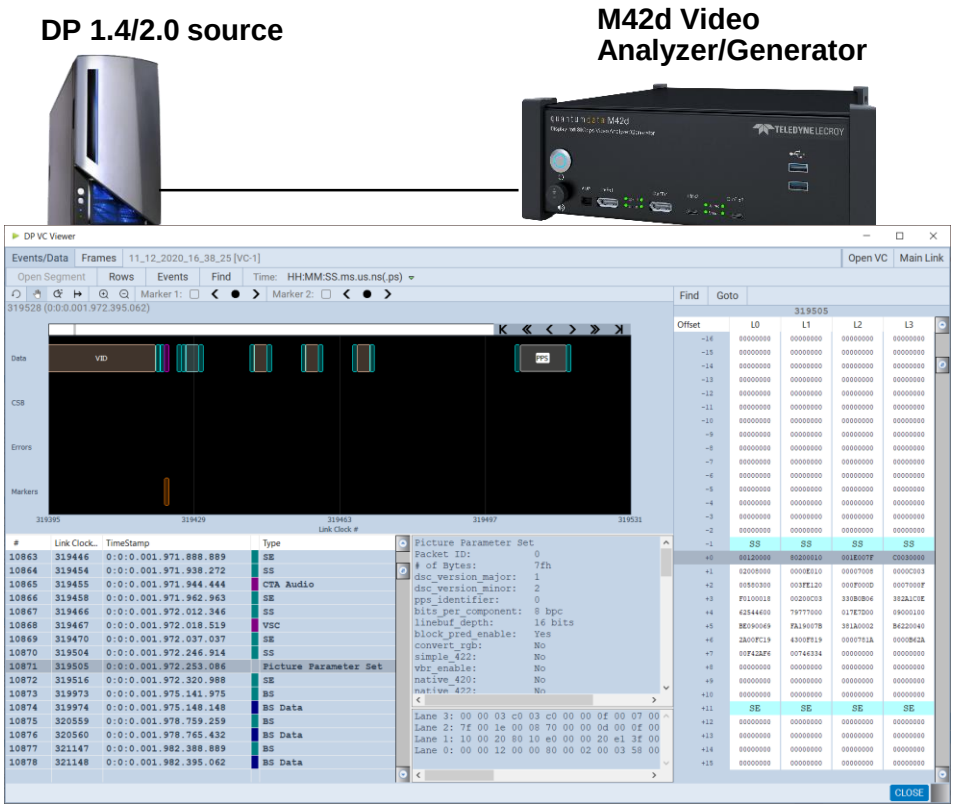
- Deep Insight offers:
  - In depth analysis of the low level protocol operation over the main video transmission link.
  - Analysis of connection sequence protocol transactions over the auxiliary channel.
- A Few Examples:
  - DisplayPort 2.0 MST capture 13.5Gb/s main stream. (Showing MST Link capture with 4 VCs.)



Deep Insight – Example 2a – DP 2.0 Virtual Channel

TIME TO INSIGHT™

- Deep Insight offers:
  - In depth analysis of the low level protocol operation over the main video transmission link.
  - Analysis of connection sequence protocol transactions over the auxiliary channel.
- A Few Examples:
  - DisplayPort 1.4/2.0 capture & analysis of 8.1Gb/s or UHBR rates up to 20Gb/s main stream. (Showing Virtual Channel capture.)
  - Example shows DSC PPS metadata packet.



Deep Insight – Example 2c DP 1.4 Capture

TIME TO INSIGHT™

- Deep Insight offers:
  - In depth analysis of the low level protocol operation over the main video transmission link.
  - Analysis of connection sequence protocol transactions over the auxiliary channel.
- A Few Examples:
  - DisplayPort 1.4 capture & analysis of 8.1Gb/s.

DP 1.4/2.0 source

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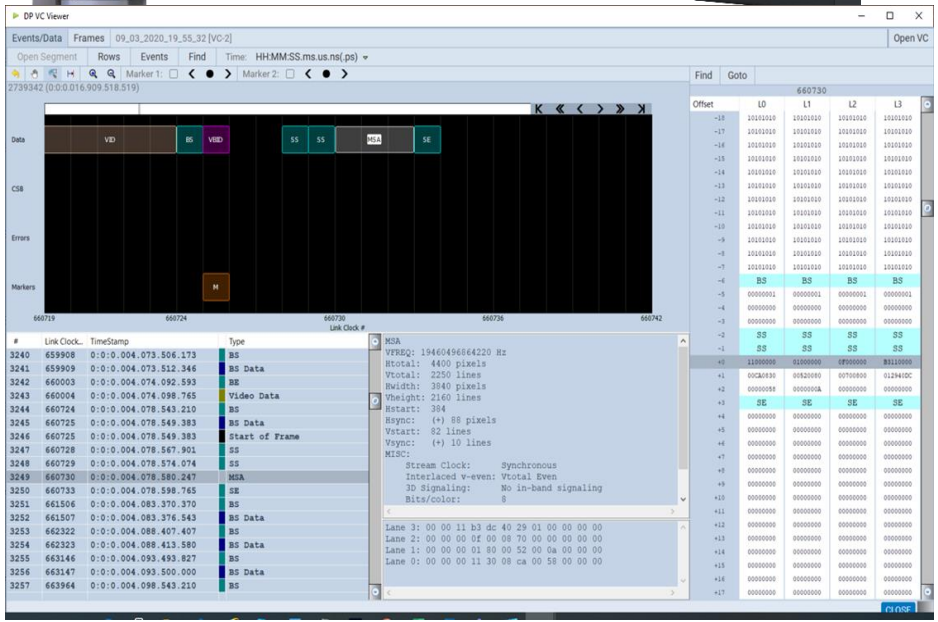

Deep Insight – Example 3a

TIME TO INSIGHT™

- Deep Insight offers:
  - In depth analysis of the low level protocol operation over the main video transmission link.
  - Analysis of connection sequence protocol transactions over the auxiliary channel.
- Example:
  - Analysis of DP 1.4/2.0 DPCD register and Link Training transactions. (Showing Link Training.)

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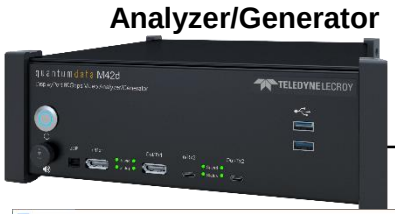
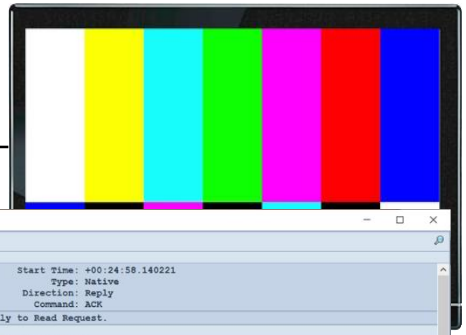
DisplayPort Monitor





ACA Data Viewer

Open Close Export Options Filter Find

[MyDP_13_5_ACA_Trace] Events: 1455 (3125)

407	DNAT	DPUSBC-R13	+00:24:58.124398	< ACK 81
408	DPLT	DPUSBC-R13	+00:24:58.124509	> W:102 TRAINING_PATTERN_SET: L=1 21
409	DPLT	DPUSBC-R13	+00:24:58.124687	< ACK
410	DPLT	DPUSBC-R13	+00:24:58.125873	> W:103 TRAINING_LANE0_SET L=4 24 24 24 24
411	DPLT	DPUSBC-R13	+00:24:58.126074	< ACK
412	DPLT	DPUSBC-R13	+00:24:58.130174	> R:202 LANE0_1_STATUS: L=2
413	DPLT	DPUSBC-R13	+00:24:58.130344	< DEFER
414	DPLT	DPUSBC-R13	+00:24:58.130924	> R:202 LANE0_1_STATUS: L=2
415	DPLT	DPUSBC-R13	+00:24:58.131094	< DEFER
416	DPLT	DPUSBC-R13	+00:24:58.131623	> R:202 LANE0_1_STATUS: L=2
417	DPLT	DPUSBC-R13	+00:24:58.131793	< DEFER
418	DPLT	DPUSBC-R13	+00:24:58.132330	> R:202 LANE0_1_STATUS: L=2
419	DPLT	DPUSBC-R13	+00:24:58.132499	< DEFER
420	DPLT	DPUSBC-R13	+00:24:58.133072	> R:202 LANE0_1_STATUS: L=2
421	DPLT	DPUSBC-R13	+00:24:58.133242	< DEFER
422	DPLT	DPUSBC-R13	+00:24:58.133780	> R:202 LANE0_1_STATUS: L=2
423	DPLT	DPUSBC-R13	+00:24:58.133949	< DEFER
424	DPLT	DPUSBC-R13	+00:24:58.134488	> R:202 LANE0_1_STATUS: L=2
425	DPLT	DPUSBC-R13	+00:24:58.134657	< ACK 11 11
426	DPLT	DPUSBC-R13	+00:24:58.134819	> W:102 TRAINING_PATTERN_SET: L=1 02
427	DPLT	DPUSBC-R13	+00:24:58.134899	< ACK
428	DPLT	DPUSBC-R13	+00:24:58.134967	> W:103 TRAINING_LANE0_SET L=4 24 24 24 24
429	DPLT	DPUSBC-R13	+00:24:58.135071	< ACK
430	DPLT	DPUSBC-R13	+00:24:58.139169	> R:202 LANE0_1_STATUS: L=3
431	DPLT	DPUSBC-R13	+00:24:58.139242	< ACK 77 77 81
432	DPLT	DPUSBC-R13	+00:24:58.139349	> R:204 LANE_ALIGN_STATUS_UPDATED L=2
433	DPLT	DPUSBC-R13	+00:24:58.139422	< ACK 01 03
434	DPLT	DPUSBC-R13	+00:24:58.139515	> W:102 TRAINING_PATTERN_SET: L=1 00
435	DPLT	DPUSBC-R13	+00:24:58.139595	< ACK
436	DPLT	DPUSBC-R13	+00:24:58.139687	> W:102 TRAINING_PATTERN_SET: L=1 00
437	DPLT	DPUSBC-R13	+00:24:58.139767	< ACK
438	DNAT	DPUSBC-R13	+00:24:58.139840	> R:200 SINK_COUNT L=6
439	DNAT	DPUSBC-R13	+00:24:58.139912	< ACK 41 00 77 77 01 02
440	DPLT	DPUSBC-R13	+00:24:58.140148	> R:100 LINK_BW_SET L=9
441	DPLT	DPUSBC-R13	+00:24:58.140221	< ACK 04 84 00 24 24 24 24 00 01
442	DNAT	DPUSBC-R13	+00:24:58.140353	> R:200 SINK_COUNT L=8
443	DNAT	DPUSBC-R13	+00:24:58.140426	< ACK 41 00 77 77 01 03 00 00

```
      Start Time: +00:24:58.140221
            Type: Native
       Direction: Reply
         Command: ACK
Reply to Read Request.

00100: LINK_BW_SET
   Bit  Name                          Value Description
   ---- ----------------------------- ----- -------------
   7-0  LINK_BW_SET                    04h  13.5 Gbps/lane (UHBR13.5)

00101: LANE_COUNT_SET
   Bit  Name                          Value Description
   ---- ----------------------------- ----- -------------
   4-0  LANE_COUNT_SET                   4  4 lanes
     5  POST_LT_ADJ_REQ_GRANTED       N(0)
     6                                   0  Reserved
     7  ENHANCED_FRAME_CAP            Y(1)

00102: TRAINING_PATTERN_SET:
   8b/10b Link Layer

   Bit  Name                          Value Description
   ---- ----------------------------- ----- -------------
   3-0  TRAINING_PATTERN_SELECT          0  None
     4  RECOVERED_CLOCK_OUT_EN        N(0)
     5  SCRAMBLING_DISABLE            N(0)
   7-6  SYMBOL_ERROR_COUNT_SEL           0  Disparity and Symbol error

   128b/132b Link Layer

   Bit  Name                          Value Description
   ---- ----------------------------- ----- -------------
   3-0  TRAINING_PATTERN_SELECT          0  None
     4                                   0  Reserved
     5  SCRAMBLING_DISABLE            N(0)
     6                                   0  Reserved
     7                                   0  Reserved

00103: TRAINING_LANE0_SET
   8b/10b Link Layer

   Bit  Name                          Value Description
```

441: < ACK 04 84 00 24 24 24 24 00 01

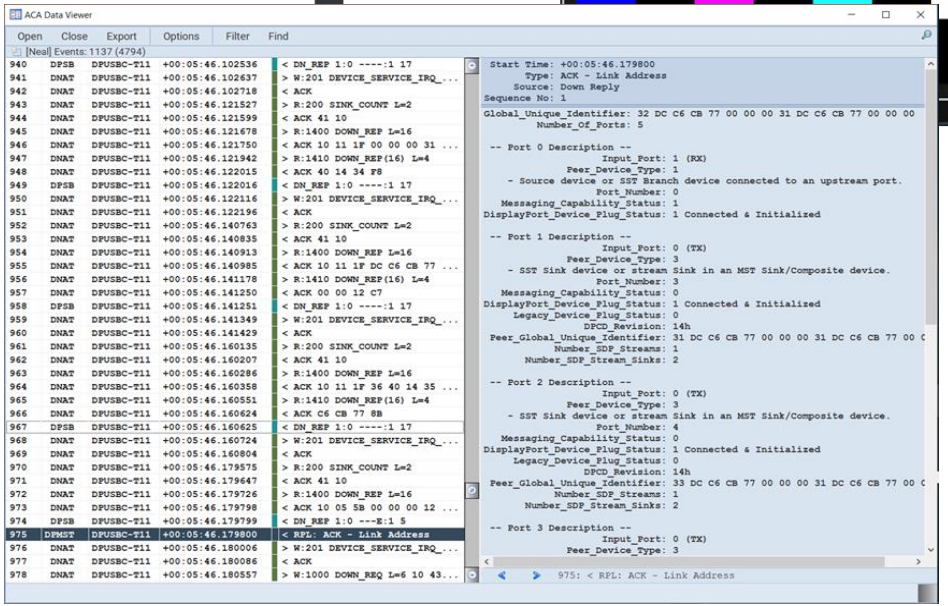
Deep Insight – Example 3b

TIME TO INSIGHT™

- Deep Insight offers:
  - In depth analysis of the low level protocol operation over the main video transmission link.
  - Analysis of connection sequence protocol transactions over the auxiliary channel.
- Example:
  - Analysis of DP 1.4/2.0 DPCD register and Link Training transactions. (Showing MST Topology discovery.)

M42d Video Analyzer/Generator

DisplayPort Monitor

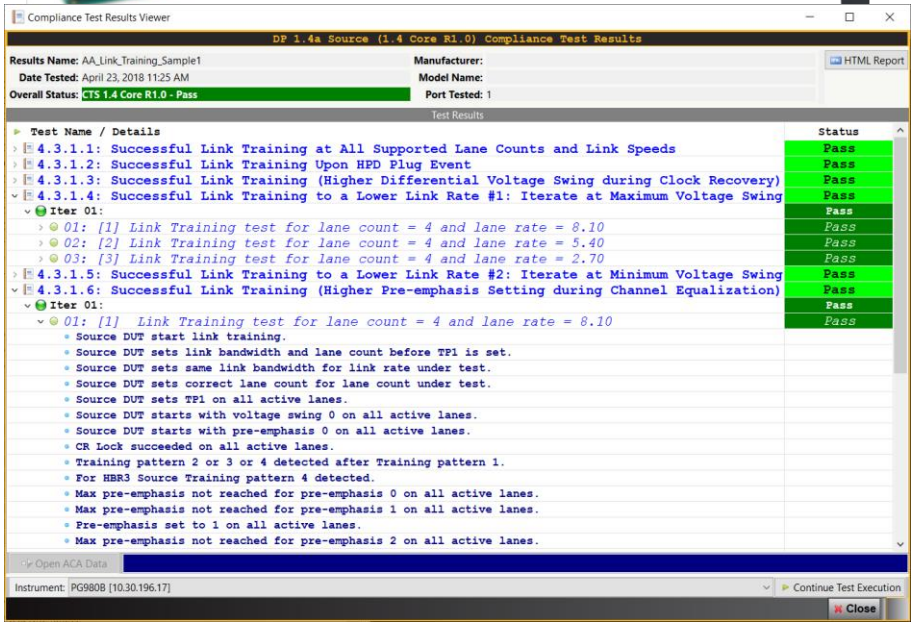


Compliance Tests – Example 1

- Compliance Testing Provides:
  - Required test suites to obtain industry logo.
  - Detailed test results and logs that provide insight into the cause of failures.
- Example:
  - DisplayPort 1.4 Link Layer source compliance test suite. Link Layer compliance testing for DP 2.0 sources and sinks is planned for a future release.

DP 1.4/2.0 source development board

M42d Video Analyzer/Generator



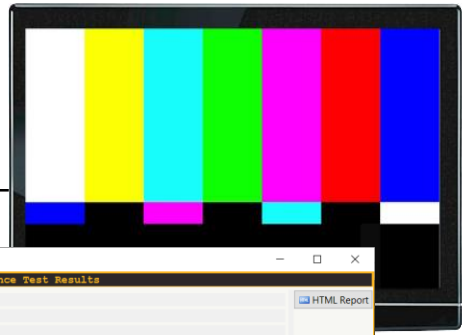
Compliance Tests – Example 2

TIME TO INSIGHT™

- Compliance Testing Provides:
  - Required test suites to obtain industry logo.
  - Detailed test results and logs that provide insight into the cause of failures.
- Example:
  - DisplayPort 1.4 sink compliance for Display Stream Compression (DSC). DSC Compliance testing for DP 2.0 sinks is planned for a future release.

M42d Video Analyzer/Generator

DP DSC Display



Compliance Test Results Viewer

DP 1.4a DSC Sink (R1.0) Compliance Test Results

Results Name: DUT1_DSC_TEST_ALL
Date Tested: October 30, 2019 5:53 PM
Overall Status: CTS R1.0 - Fail
Manufacturer:
Model Name:
Port Tested: 1
HTML Report

Test Results

Test Name / Details	Status
5.6.1.1: DSC capability verification	Pass
5.6.1.2: DSC RGB color depth test	Pass
5.6.1.3: DSC RGB Block prediction test	Pass
5.6.1.4: DSC RGB bits-per-pixel test	Pass
5.6.1.5: DSC RGB slice test	Pass
5.6.1.6: DSC RGB lanes test	Pass
5.6.1.7: DSC YCbCr 4:4:4 color depth test	Pass
5.6.1.8: DSC YCbCr 4:4:4 Block prediction test	Pass
5.6.1.9: DSC YCbCr 4:4:4 bits-per-pixel test	Pass
5.6.1.10: DSC YCbCr 4:4:4 slice test	Pass
5.6.1.11: DSC YCbCr 4:4:4 lanes test	Pass
5.6.1.12: DSC Simple 4:2:2 color depth test	Pass
5.6.1.13: DSC Simple 4:2:2 Block prediction test	Pass
5.6.1.14: DSC Simple 4:2:2 bits-per-pixel test	Pass
Iter 01:	Pass
01: Initial Link Training at maximum link rate and lane count success	Pass
02: For Timing 1920x1080p@30Hz bpc 8 bpp 8.0 CRC check or Visual check verification	Pass
03: For Timing 1920x1080p@30Hz bpc 8 bpp 8.125 CRC check or Visual check verification	Pass
04: For Timing 1920x1080p@30Hz bpc 8 bpp 8.250 CRC check or Visual check verification	Pass
05: For Timing 1920x1080p@30Hz bpc 8 bpp 8.375 CRC check or Visual check verification	Pass
06: For Timing 1920x1080p@30Hz bpc 8 bpp 10.0 CRC check or Visual check verification	Pass
07: For Timing 1920x1080p@30Hz bpc 8 bpp 10.125 CRC check or Visual check verification	Pass
08: For Timing 1920x1080p@30Hz bpc 8 bpp 10.250 CRC check or Visual check verification	Pass
09: For Timing 1920x1080p@30Hz bpc 8 bpp 10.375 CRC check or Visual check verification	Pass
10: For Timing 1920x1080p@30Hz bpc 10 bpp 8.0 CRC check or Visual check verification	Pass
11: For Timing 1920x1080p@30Hz bpc 10 bpp 8.125 CRC check or Visual check verification	Pass

Open ACA Data | 5.6.1.1: DSC capability verification

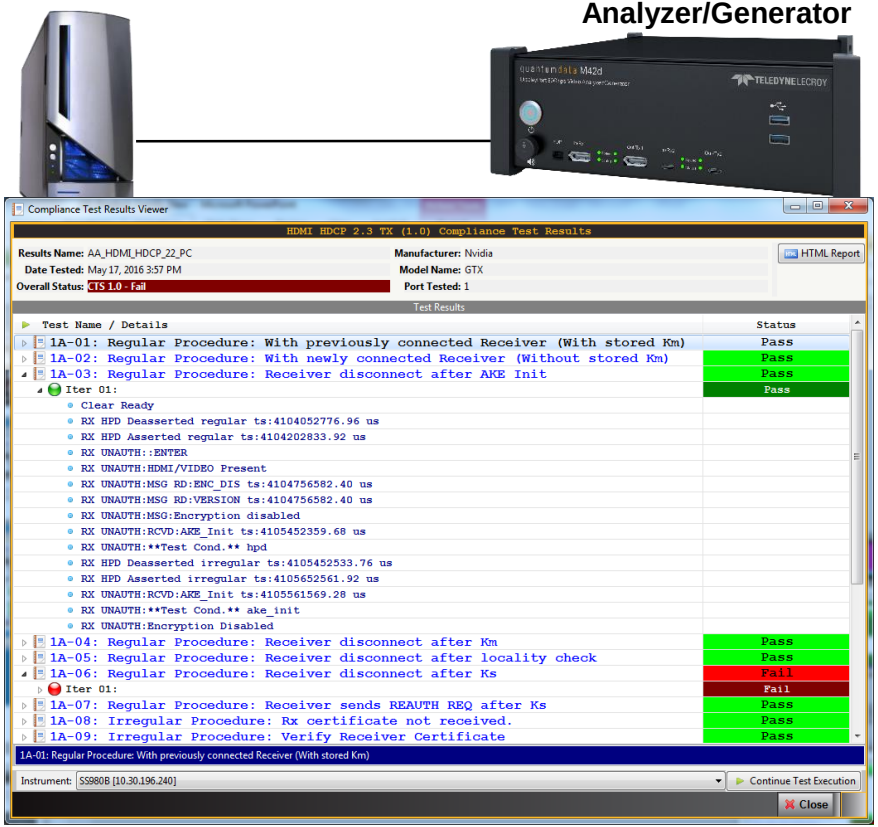
Instrument: PG9808 [10.30.196.17] | Continue Test Execution | Close

Compliance Tests – Example 3

- Compliance Testing Provides:
  - Required test suites to obtain industry logo.
  - Detailed test results and logs that provide insight into the cause of failures.
- Example:
  - HDCP 2.2/3 compliance for DisplayPort source devices.

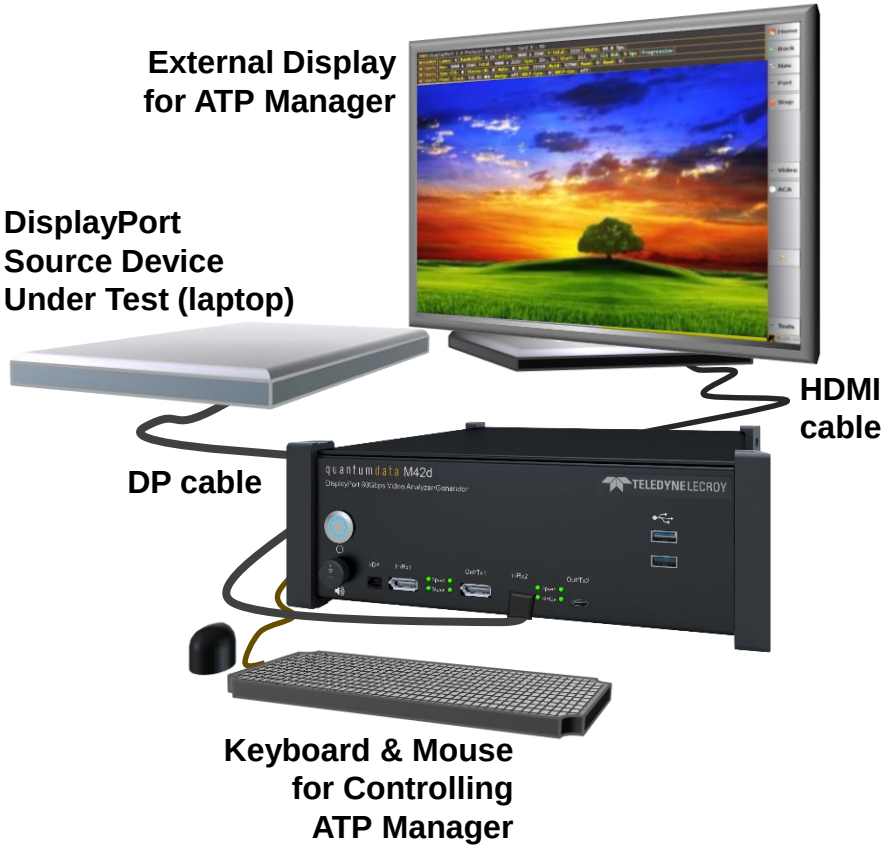
DP 1.4/2.0 source

M42d Video Analyzer/Generator



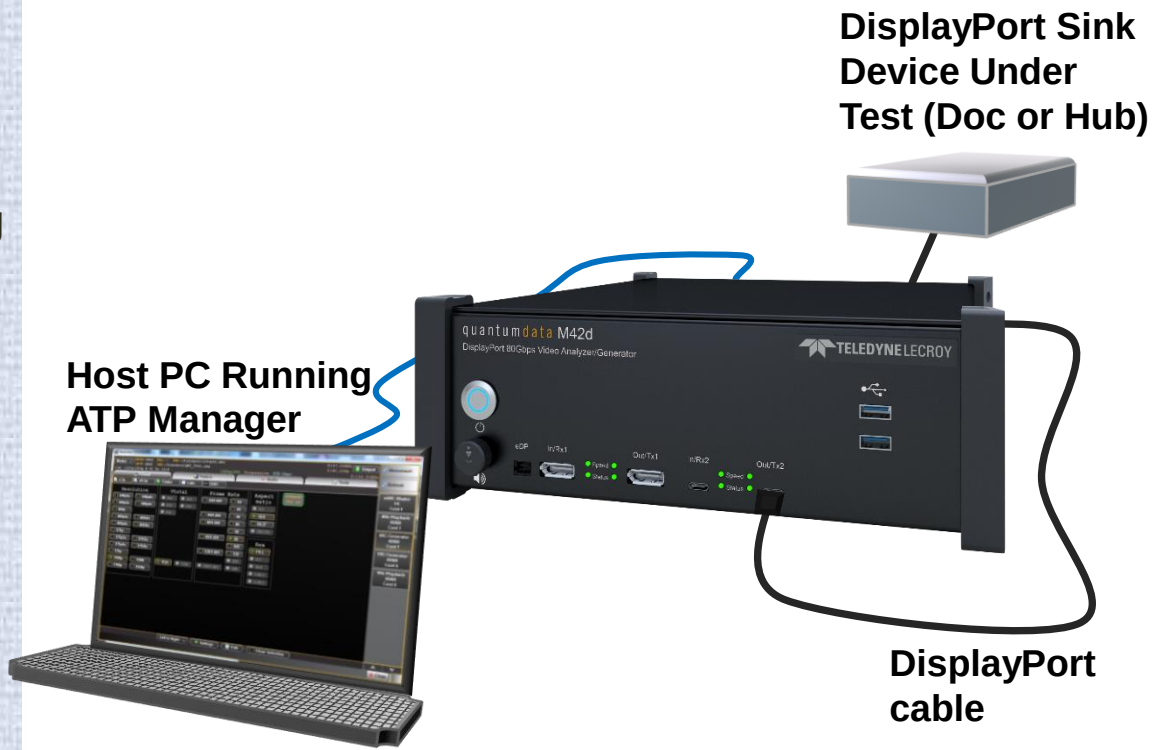
M42d Test Setup – DisplayPort 2.0 Source Testing

- Source testing
  - Use connected HDCP 2.2/3 compatible display to view M42d ATP Manager Graphical User Interface.
  - Connection to the HDMI port on back of M42d.
  - Use Keyboard and mouse to control ATP Manager GUI running on the connected display.



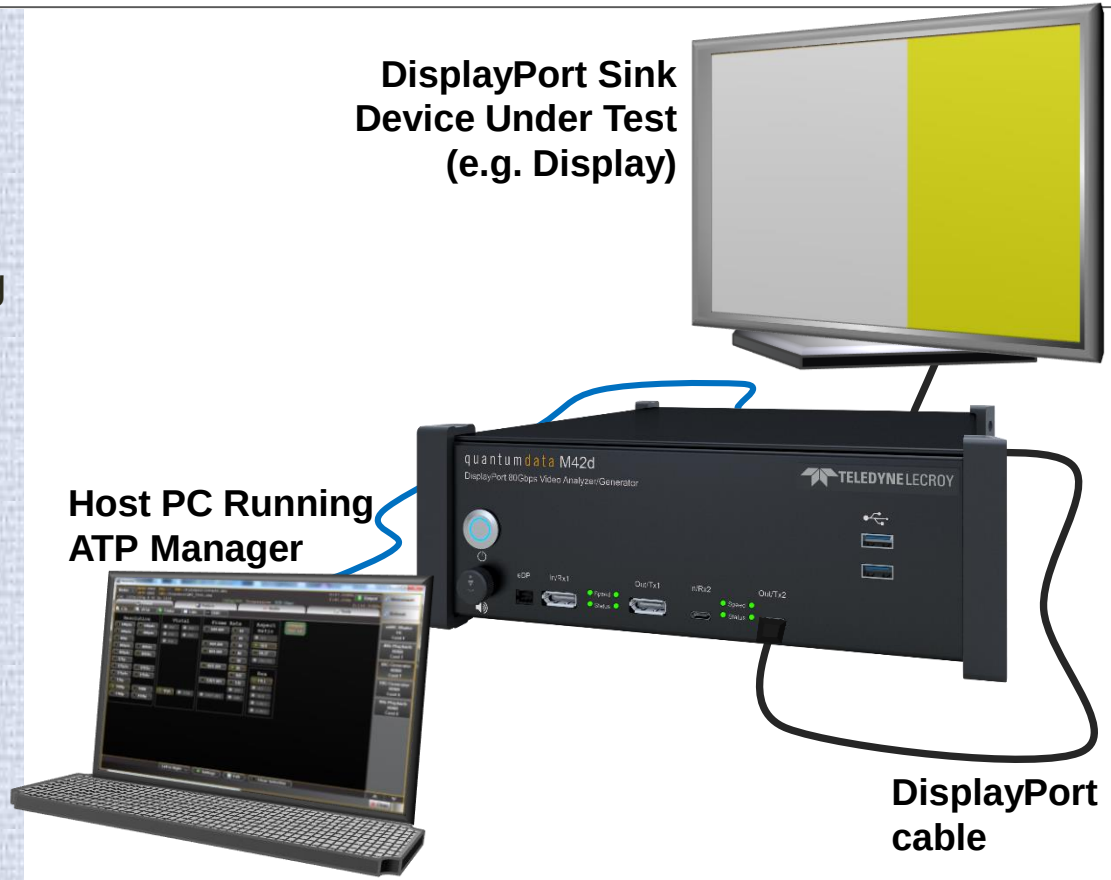
M42d Test Setup – DisplayPort 2.0 Sink Testing

- Sink testing
  - Use connected M42d ATP Manager graphical user interface installed on host PC.
  - Use Keyboard and mouse to control ATP Manager GUI running on the connected display.
  - Connect Host PC to M42d via Ethernet cable, either direct or through corporate LAN.
  - Example: Sink hub or docking station.



M42d Test Setup – DisplayPort 2.0 Sink Testing

- Sink testing
  - Use connected M42d ATP Manager graphical user interface installed on host PC.
  - Use Keyboard and mouse to control ATP Manager GUI running on the connected display.
  - Connect Host PC to M42d via Ethernet cable, either direct or through corporate LAN.
  - Example: High resolution display.



M42d Test Setup – DisplayPort Passive Monitoring Source/Sink

- Passive Monitoring – Aux Chan
  - Monitor the Aux Cannel between a DP 1.4/2.0 source and sink device.
  - View Link Training, EDID exchange, HDCP authentication between a source and sink through Aux Channel Analyzer utility.
- Passive Monitoring – Main Link
  - Monitor the Main Link between a DP 2.0 source and sink device up to 20Gbps lane rate.
  - View video, audio, control, metadata and symbol data through the basic analyzer viewer and the Capture Viewer.