

# quantumdata M42d Video Analyzer/Generator

November – 2020



*Help silicon and product developers bring their next-generation video solutions to market—faster, without interoperability problems and at reduced cost*



Our solutions quicken Time-to-Insight



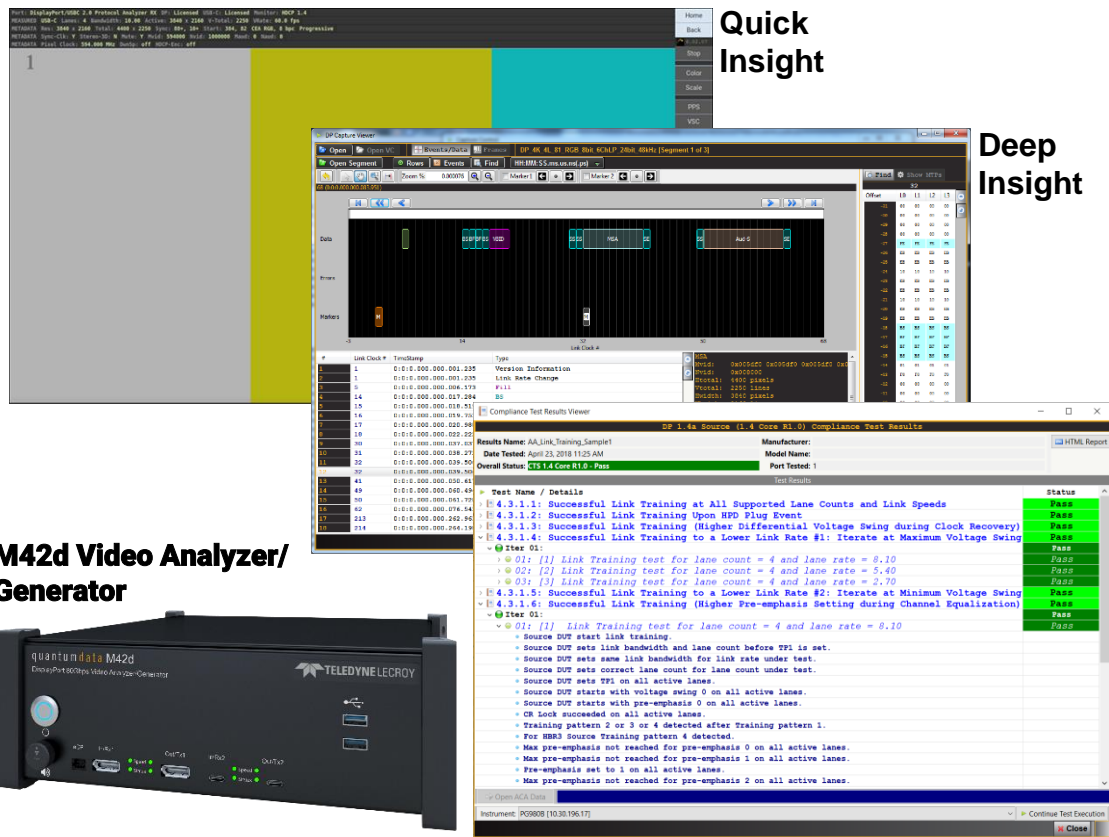
# M42d Video Analyzer/Generator – Features and Functions

- ◆ Provides Protocol Analysis and Video Generation for DisplayPort 2.0 source and sink testing through standard DP ports and USB-C ports for DP Alt Mode.
- ◆ Enables viewing of incoming video and essential video and timing parameters.
- ◆ Protocol Capture Analyzer provides deep insight of the DP 2.0 video, audio, metadata, control data, and symbol data including DSC/FEC compression.
- ◆ Supports DP 1.4 Link Layer compliance tests for DP sources and sinks. Includes DSC and FEC compliance testing. DisplayPort 2.0 compliance testing planned for future release.
- ◆ Video generator outputs user-specified link configurations up to 8.1Gb/s rates for DP 1.4 and UHBR rates for DP 2.0 on four (4) lanes.
- ◆ Supports DCP-approved HDCP 2.2/3 source, sink and repeater compliance testing.
- ◆ Supports passive monitoring of the DisplayPort Aux Channel and Main Link at UHBR lane rates.
- ◆ Advanced Features such as Panel Replay and LTTPR are planned for future releases.



# What is Time-to-Insight?

- ◆ **Time-to-Insight saves time and money.** It involves the following:
  - ◆ **Quick Insight:** Provides at-a-glance information—insight—into the basic functioning of an DisplayPort video device or system.
  - ◆ **Deep Insight:** Provides full visibility—insight—into the low level protocol to verify the proper functioning of an DisplayPort device to improve interoperability.
  - ◆ **Compliance Tests:** Provides required test suites for DisplayPort Logo program.



The screenshot shows the DP Capture Viewer interface. The top window displays a video signal waveform with a yellow and blue background. The bottom window shows a compliance test results viewer for a DisplayPort 1.4a Core R1.0. The test results are as follows:

Test Name / Details	Status
4.3.1.1: Successful Link Training at all Supported Lane Counts and Link Speeds	Pass
4.3.1.2: Successful Link Training Under HPD Plug Event	Pass
4.3.1.3: Successful Link Training (Higher Differential Voltage Swing during Clock Recovery)	Pass
4.3.1.4: Successful Link Training to a Lower Link Rate #1: Iterate at Maximum Voltage Swing	Pass
Iter 01:	Pass
01: [1] Link Training test for lane count = 4 and lane rate = 8.10	Pass
02: [2] Link Training test for lane count = 4 and lane rate = 5.40	Pass
03: [3] Link Training test for lane count = 4 and lane rate = 2.70	Pass
4.3.1.5: Successful Link Training to a Lower Link Rate #2: Iterate at Minimum Voltage Swing	Pass
4.3.1.6: Successful Link Training (Higher Pre-emphasis Setting during Channel Equalization)	Pass
Iter 02:	Pass
01: [1] Link Training test for lane count = 4 and lane rate = 8.10	Pass
Source DUT start link training.	
Source DUT sets link bandwidth and lane count before TPI is set.	
Source DUT sets same link bandwidth for link rate under test.	
Source DUT sets correct lane count for lane count under test.	
Source DUT sets FPS on all active lanes.	
Source DUT starts with voltage swing 0 on all active lanes.	
Source DUT starts with voltage swing 0 on all active lanes.	
CR Lock succeeded on all active lanes.	
Training pattern 2 or 3 or 4 detected after Training pattern 1.	
For HBR3 Source Training pattern 4 detected.	
Max pre-emphasis not reached for pre-emphasis 0 on all active lanes.	
Max pre-emphasis not reached for pre-emphasis 1 on all active lanes.	
Pre-emphasis set to 1 on all active lanes.	
Max pre-emphasis not reached for pre-emphasis 2 on all active lanes.	

## M42d Video Analyzer/Generator



## Compliance

# Quick Insight – Example 1

- ◆ Quick Insight Solutions Include:
  - ◆ Basic analysis views of incoming videos streams.
  - ◆ Essential status information on dashboards, and status panels.
  - ◆ Device emulation of sources and sinks (displays).
- ◆ A Few Examples:
  - ◆ DisplayPort Receiver view w/ status bar at top. Shows incoming video and metadata from a source device.

DP 1.4/2.0 source development board



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Port: DisplayPort/USB-C Protocol Analyzer RX DP, Licensed / USB-C, Licensed Monitor: HDCP 1.4

RECEIVED USB-C, Lane: 4 BitRate: 10.00 Active: 3540 x 2160 V-Totals: 2220 V-Rate: 60.0 Fps

METADATA Res: 3540 x 2160 Total: 4000 x 2250 Sync: 60, 10e Starts: 354, 52, CEA-86B, 0 Sync Progressive

METADATA Sync-Cli: Y Stereo-3D: N Mute: Y H-Val: 594000 H-Val: 1000000 H-Val: 0 H-Val: 0

METADATA Pixel Clock: 594.000 MHz Dump: off HDCP-Enc: off

1

Home  
Back  
History  
Stop  
Color  
Scale  
PPS  
VSC  
ACA  
Set EDID  
Set DPCD  
Tools  
Tests

# Quick Insight – Example 2

## ◆ Quick Insight Solutions Include:

- ◆ Real Time analysis views of incoming videos streams.
- ◆ Essential status information on dashboards, and status panels.
- ◆ Device emulation of sources and sinks (displays).

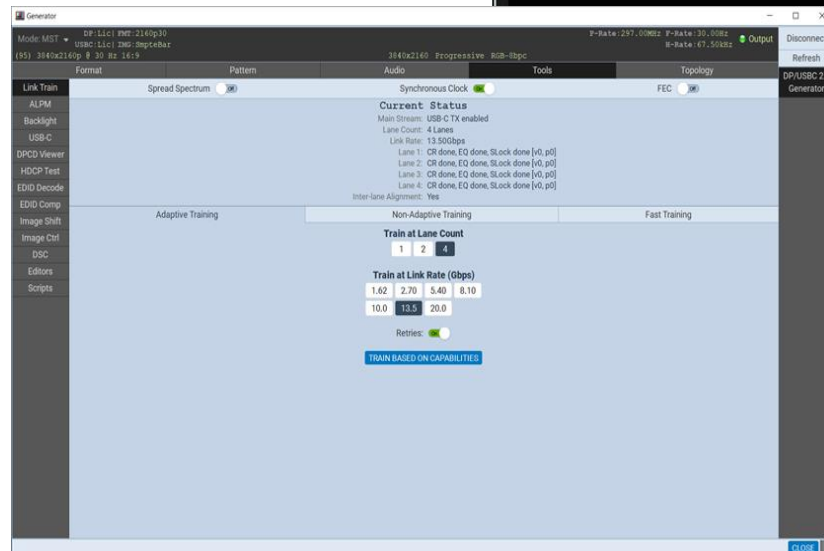
## ◆ A Few Examples:

- ◆ DisplayPort link training control & status with connected display.

**M42d Video Analyzer/Generator**



**DisplayPort Display**



# Quick Insight – Example 3

## Quick Insight Solutions Include:

- Real Time analysis views of incoming videos streams.
- Essential status information on dashboards, and status panels.
- Device emulation of sources and sinks (displays).

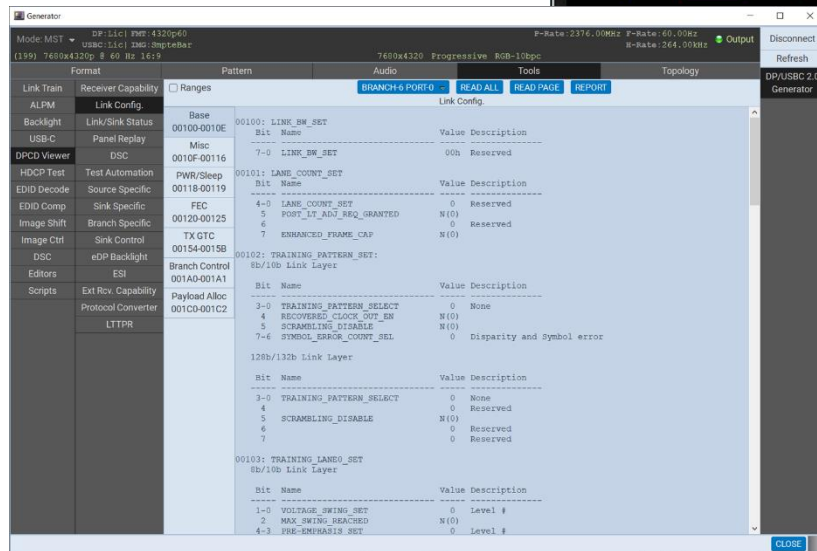
## A Few Examples:

- DP EDID and DPCD data view of connected sink device.

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**HDMI UHD TV**



# Deep Insight – Example 2a – DP 2.0 13.5G Capture



- ◆ Deep Insight offers:
  - ◆ In depth analysis of the low level protocol operation over the main video transmission link.
  - ◆ Analysis of connection sequence protocol transactions over the auxiliary channel.
- ◆ A Few Examples:
  - ◆ DisplayPort 2.0 MST capture 13.5Gb/s main stream. (Showing MST Link capture with 4 VCs.)

DP 1.4/2.0 source



M42d Video Analyzer/Generator



The screenshot shows the DP Capture Viewer interface. At the top, it displays 'Events/Data' and 'Frames' for 'ForDemoUHBR13.5'. The main area shows a waveform of the captured data. Below the waveform is a table of captured packets:

#	Link Clock #	TimeStamp	Type
1	1	0:0:0.000.000.000.741	Version Information
2	1	0:0:0.000.000.000.741	Link Rate Change
3	174	0:0:0.000.000.130.370	LLCP Data
4	193	0:0:0.000.000.142.963	Capture Trigger
5	65716	0:0:0.000.048.878.819	LLCP Data
6	131256	0:0:0.000.097.126.667	LLCP Data
7	196796	0:0:0.000.145.774.815	LLCP Data
8	262336	0:0:0.000.194.322.963	LLCP Data
9	327876	0:0:0.000.242.871.111	LLCP Data
10	393416	0:0:0.000.291.419.259	LLCP Data
11	458956	0:0:0.000.339.967.407	LLCP Data
12	524496	0:0:0.000.388.515.554	LLCP Data
13	590036	0:0:0.000.437.063.704	LLCP Data
14	655576	0:0:0.000.485.611.852	LLCP Data
15	721116	0:0:0.000.534.160.000	LLCP Data
16	786656	0:0:0.000.582.708.148	LLCP Data
17	852196	0:0:0.000.631.256.296	LLCP Data
18	917736	0:0:0.000.679.804.444	LLCP Data
19	983276	0:0:0.000.728.352.593	LLCP Data
20	1048816	0:0:0.000.776.900.741	LLCP Data
21	1114356	0:0:0.000.825.448.889	LLCP Data
22	1179896	0:0:0.000.873.997.037	LLCP Data
23	1245436	0:0:0.000.922.545.185	LLCP Data

The detailed packet view on the right shows the structure of an LLCP Data packet, including fields like ACT, RDCR, ECF, and LVP.



- ◆ Deep Insight offers:
  - ◆ In depth analysis of the low level protocol operation over the main video transmission link.
  - ◆ Analysis of connection sequence protocol transactions over the auxiliary channel.
- ◆ A Few Examples:
  - ◆ DisplayPort 1.4/2.0 capture & analysis of 8.1Gb/s or UHBR rates up to 20Gb/s main stream. (Showing Virtual Channel capture.)
  - ◆ Example shows DSC PPS metadata packet.

DP 1.4/2.0 source



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The screenshot shows the DP VC Viewer interface with a packet capture window and a detailed view of a Packet Parameter Set (PPS) packet. The packet list shows:

#	Link Clock	TimeStamp	Type
10863	319444	0:0:0.001.971.888.889	SS
10864	319454	0:0:0.001.971.938.272	SS
10865	319455	0:0:0.001.971.944.444	CTA Audio
10866	319458	0:0:0.001.971.962.963	SE
10867	319466	0:0:0.001.972.012.346	SE
10868	319467	0:0:0.001.972.018.519	VSC
10869	319470	0:0:0.001.972.037.037	SE
10870	319504	0:0:0.001.972.246.914	SS
10871	319505	0:0:0.001.972.253.086	Picture Parameter Set
10872	319516	0:0:0.001.972.320.988	SE
10873	319973	0:0:0.001.975.141.975	BS
10874	319974	0:0:0.001.975.148.148	BS Data
10875	320559	0:0:0.001.978.759.259	BS
10876	320560	0:0:0.001.978.765.432	BS Data
10877	321147	0:0:0.001.982.388.889	BS
10878	321148	0:0:0.001.982.395.062	BS Data

The detailed view of the Packet Parameter Set (PPS) packet shows the following parameters:

- Packet ID: 0
- # of Bytes: 7fh
- dsc\_version\_major: 1
- dsc\_version\_minor: 2
- pps\_identifier: 0
- bits\_per\_component: 8 bpc
- linebuf\_depth: 16 bits
- block\_pred\_enable: Yes
- convert\_rgb: No
- simple\_422: No
- vbr\_enable: No
- native\_420: No
- native\_422: No

The interface also shows a hex dump of the packet data and a table of offsets for the packet structure.

# Deep Insight – Example 2c DP 1.4 Capture



- ◆ Deep Insight offers:
  - ◆ In depth analysis of the low level protocol operation over the main video transmission link.
  - ◆ Analysis of connection sequence protocol transactions over the auxiliary channel.
- ◆ A Few Examples:
  - ◆ DisplayPort 1.4 capture & analysis of 8.1Gb/s.

DP 1.4/2.0 source



M42d Video Analyzer/Generator



The screenshot shows the DP VC Viewer software interface. The main window displays a timeline of events with columns for Data, CSB, Errors, and Markers. A detailed protocol analysis pane is open on the right, showing the following information:

- MSA**: VEREQ: 19460496864220 Hz
- HTotal**: 4400 pixels
- VTotal**: 2250 lines
- Rwidth**: 3940 pixels
- Weight**: 2160 lines
- Start**: 394
- Hsync**: (+) 88 pixels
- Vstart**: 82 lines
- Vsync**: (+) 10 lines
- MSOC**: Stream Clock: Synchronous, Interlaced v-even: Vtotal Even, 3D signaling: No in-band signaling, Bits/color: 8
- Lane 3**: 00 00 11 b3 dc 40 29 01 00 00 00 00
- Lane 2**: 00 00 00 0f 60 08 70 00 00 00 00 00
- Lane 1**: 00 00 00 01 60 08 52 00 0a 00 00 00
- Lane 0**: 00 00 00 11 30 08 ca 00 58 00 00 00

# Deep Insight – Example 3a

## ◆ Deep Insight offers:

- ◆ In depth analysis of the low level protocol operation over the main video transmission link.
- ◆ Analysis of connection sequence protocol transactions over the auxiliary channel.

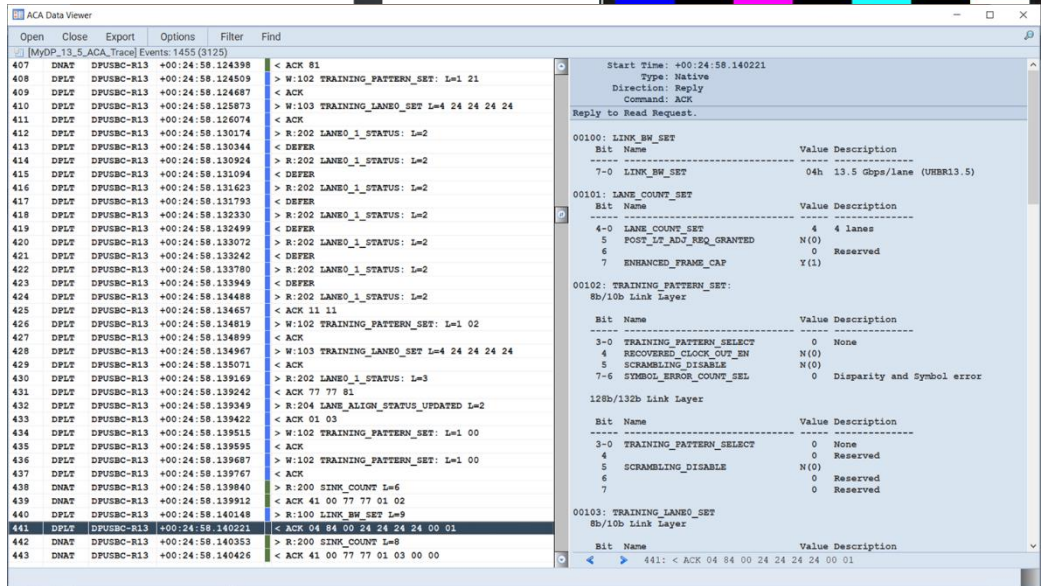
## ◆ Example:

- ◆ Analysis of DP 1.4/2.0 DPCD register and Link Training transactions. (Showing Link Training.)

### M42d Video Analyzer/Generator



### DisplayPort Monitor



The screenshot displays the ACA Data Viewer software interface. The main window shows a trace of DP 1.4/2.0 DPCD register and Link Training transactions. The trace is organized into columns for time, direction, and data. The data column shows various Link Training transactions, including ACK, TRAINING\_PATTERN\_SET, TRAINING\_LANE0\_SET, LANE0\_STATUS, LANE0\_COUNT\_SET, POST\_LINK\_RDY\_REQ\_GRANTED, ENHANCED\_FRAME\_CAP, TRAINING\_PATTERN\_SELECT, RECOVERED\_CLOCK\_OUT\_EN, SCRAMBLING\_DISABLE, and SYMBOL\_ERROR\_COUNT\_SEL. The right-hand pane shows a detailed view of the selected transaction, including the Start Time, Type, Direction, Command, and Reply to Read Request. The detailed view shows the Bit Name, Value, and Description for each bit in the transaction.

Time	Direction	Data
407	DMAT	DFUSBC-R13 +00:24:58.124398 < ACK 81
408	DPLT	DFUSBC-R13 +00:24:58.124509 > W:102 TRAINING_PATTERN_SET: L=1 21
409	DPLT	DFUSBC-R13 +00:24:58.124687 < ACK
410	DPLT	DFUSBC-R13 +00:24:58.125873 > W:103 TRAINING_LANE0_SET L=4 24 24 24 24
411	DPLT	DFUSBC-R13 +00:24:58.126074 < ACK
412	DPLT	DFUSBC-R13 +00:24:58.130174 > R:202 LANE0_1_STATUS: L=2
413	DPLT	DFUSBC-R13 +00:24:58.130344 < DEFER
414	DPLT	DFUSBC-R13 +00:24:58.130924 > R:202 LANE0_1_STATUS: L=2
415	DPLT	DFUSBC-R13 +00:24:58.131094 < DEFER
416	DPLT	DFUSBC-R13 +00:24:58.131623 > R:202 LANE0_1_STATUS: L=2
417	DPLT	DFUSBC-R13 +00:24:58.131793 < DEFER
418	DPLT	DFUSBC-R13 +00:24:58.132330 > R:202 LANE0_1_STATUS: L=2
419	DPLT	DFUSBC-R13 +00:24:58.132499 < DEFER
420	DPLT	DFUSBC-R13 +00:24:58.133072 > R:202 LANE0_1_STATUS: L=2
421	DPLT	DFUSBC-R13 +00:24:58.133242 < DEFER
422	DPLT	DFUSBC-R13 +00:24:58.133780 > R:202 LANE0_1_STATUS: L=2
423	DPLT	DFUSBC-R13 +00:24:58.133949 < DEFER
424	DPLT	DFUSBC-R13 +00:24:58.134488 > R:202 LANE0_1_STATUS: L=2
425	DPLT	DFUSBC-R13 +00:24:58.134657 < ACK 11 11
426	DPLT	DFUSBC-R13 +00:24:58.134819 > W:102 TRAINING_PATTERN_SET: L=1 02
427	DPLT	DFUSBC-R13 +00:24:58.134899 < ACK
428	DPLT	DFUSBC-R13 +00:24:58.134967 > W:103 TRAINING_LANE0_SET L=4 24 24 24 24
429	DPLT	DFUSBC-R13 +00:24:58.135071 < ACK
430	DPLT	DFUSBC-R13 +00:24:58.139169 > R:202 LANE0_1_STATUS: L=3
431	DPLT	DFUSBC-R13 +00:24:58.139242 < ACK 77 77 81
432	DPLT	DFUSBC-R13 +00:24:58.139349 > R:204 LANE_ALIGN_STATUS_UPDATED L=2
433	DPLT	DFUSBC-R13 +00:24:58.139422 < ACK 01 03
434	DPLT	DFUSBC-R13 +00:24:58.139515 > W:102 TRAINING_PATTERN_SET: L=1 00
435	DPLT	DFUSBC-R13 +00:24:58.139595 < ACK
436	DPLT	DFUSBC-R13 +00:24:58.139687 > W:102 TRAINING_PATTERN_SET: L=1 00
437	DPLT	DFUSBC-R13 +00:24:58.139767 < ACK
438	DNAT	DFUSBC-R13 +00:24:58.139840 > R:200 SINK_COUNT L=6
439	DNAT	DFUSBC-R13 +00:24:58.139912 < ACK 41 00 77 77 01 02
440	DPLT	DFUSBC-R13 +00:24:58.140148 > R:100 LINK_BW_SET L=9
441	DPLT	DFUSBC-R13 +00:24:58.140221 < ACK 04 04 00 24 24 24 00 01
442	DMAT	DFUSBC-R13 +00:24:58.140353 > R:200 SINK_COUNT L=9
443	DNAT	DFUSBC-R13 +00:24:58.140426 < ACK 41 00 77 77 01 03 00 00

# Deep Insight – Example 3b

## ◆ Deep Insight offers:

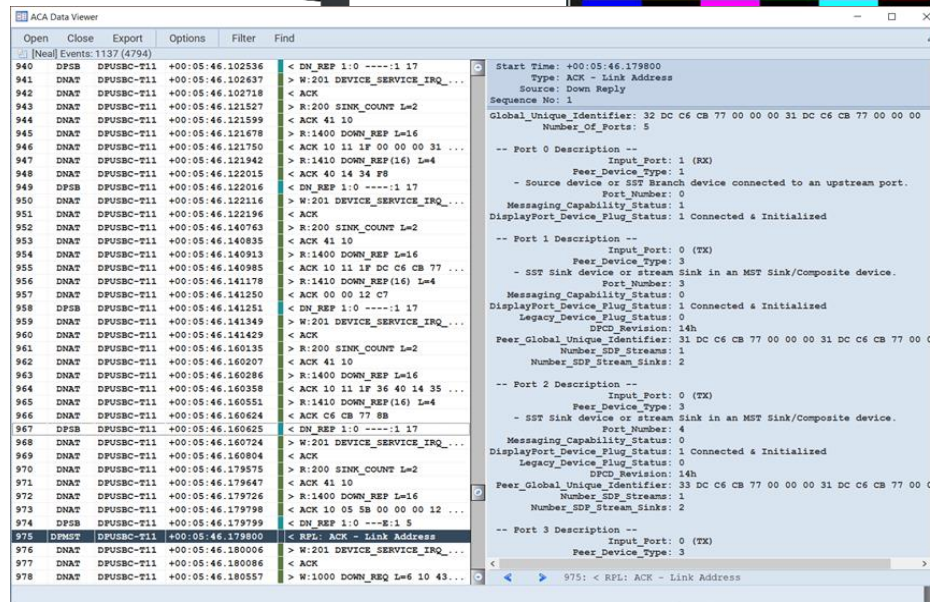
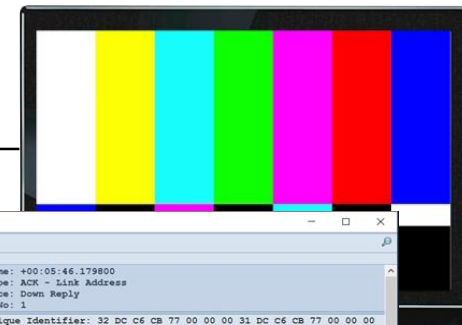
- ◆ In depth analysis of the low level protocol operation over the main video transmission link.
- ◆ Analysis of connection sequence protocol transactions over the auxiliary channel.

## ◆ Example:

- ◆ Analysis of DP 1.4/2.0 DPCD register and Link Training transactions. (Showing MST Topology discovery.)



**DisplayPort Monitor**



# Compliance Tests – Example 1

- ◆ Compliance Testing Provides:
  - ◆ Required test suites to obtain industry logo.
  - ◆ Detailed test results and logs that provide insight into the cause of failures.
- ◆ Example:
  - ◆ DisplayPort 1.4 Link Layer source compliance test suite. Link Layer compliance testing for DP 2.0 sources and sinks is planned for a future release.

DP 1.4/2.0 source development board



M42d Video Analyzer/Generator



Compliance Test Results Viewer

DP 1.4a Source (1.4 Core R1.0) Compliance Test Results

Results Name: AA\_Link\_Training\_Sample1      Manufacturer:      HTML Report  
Date Tested: April 23, 2018 11:25 AM      Model Name:  
Overall Status: **CTS 1.4 Core R1.0 - Pass**      Port Tested: 1

Test Name / Details	Status
4.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds	Pass
4.3.1.2: Successful Link Training Upon HPD Plug Event	Pass
4.3.1.3: Successful Link Training (Higher Differential Voltage Swing during Clock Recovery)	Pass
4.3.1.4: Successful Link Training to a Lower Link Rate #1: Iterate at Maximum Voltage Swing	Pass
Iter 01:	Pass
01: [1] Link Training test for lane count = 4 and lane rate = 8.10	Pass
02: [2] Link Training test for lane count = 4 and lane rate = 5.40	Pass
03: [3] Link Training test for lane count = 4 and lane rate = 2.70	Pass
4.3.1.5: Successful Link Training to a Lower Link Rate #2: Iterate at Minimum Voltage Swing	Pass
4.3.1.6: Successful Link Training (Higher Pre-emphasis Setting during Channel Equalization)	Pass
Iter 01:	Pass
01: [1] Link Training test for lane count = 4 and lane rate = 8.10	Pass
Source DUT start link training.	
Source DUT sets link bandwidth and lane count before TP1 is set.	
Source DUT sets same link bandwidth for link rate under test.	
Source DUT sets correct lane count for lane count under test.	
Source DUT sets TP1 on all active lanes.	
Source DUT starts with voltage swing 0 on all active lanes.	
Source DUT starts with pre-emphasis 0 on all active lanes.	
CR Lock succeeded on all active lanes.	
Training pattern 2 or 3 or 4 detected after Training pattern 1.	
For HBR3 Source Training pattern 4 detected.	
Max pre-emphasis not reached for pre-emphasis 0 on all active lanes.	
Max pre-emphasis not reached for pre-emphasis 1 on all active lanes.	
Pre-emphasis set to 1 on all active lanes.	
Max pre-emphasis not reached for pre-emphasis 2 on all active lanes.	

Instrument: PG9808 [10.30.196.17]      Continue Test Execution      Close

# Compliance Tests – Example 2

## ◆ Compliance Testing Provides:

- ◆ Required test suites to obtain industry logo.
- ◆ Detailed test results and logs that provide insight into the cause of failures.

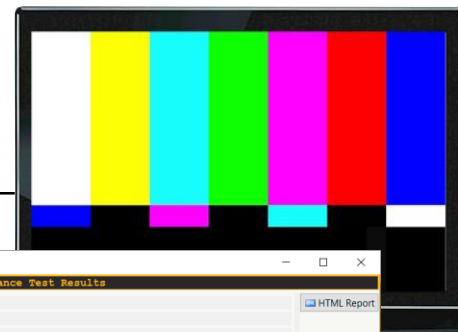
## ◆ Example:

- ◆ DisplayPort 1.4 sink compliance for Display Stream Compression (DSC). DSC Compliance testing for DP 2.0 sinks is planned for a future release.

M42d Video Analyzer/Generator



DP DSC Display



Compliance Test Results Viewer

DP 1.4a DSC Sink (R1.0) Compliance Test Results

Results Name: DUT1\_DSC\_TEST\_ALL  
Date Tested: October 30, 2019 5:53 PM  
Overall Status: **CTS R1.0 - Fail**

Manufacturer:  
Model Name:  
Port Tested: 1

Test Name / Details	Status
5.6.1.1: DSC capability verification	Pass
5.6.1.2: DSC RGB color depth test	Pass
5.6.1.3: DSC RGB Block prediction test	Pass
5.6.1.4: DSC RGB bits-per-pixel test	Pass
5.6.1.5: DSC RGB slice test	Pass
5.6.1.6: DSC RGB lanes test	Pass
5.6.1.7: DSC YCbCr 4:4:4 color depth test	Pass
5.6.1.8: DSC YCbCr 4:4:4 Block prediction test	Pass
5.6.1.9: DSC YCbCr 4:4:4 bits-per-pixel test	Pass
5.6.1.10: DSC YCbCr 4:4:4 slice test	Pass
5.6.1.11: DSC YCbCr 4:4:4 lanes test	Pass
5.6.1.12: DSC Simple 4:2:2 color depth test	Pass
5.6.1.13: DSC Simple 4:2:2 Block prediction test	Pass
5.6.1.14: DSC Simple 4:2:2 bits-per-pixel test	Pass
Iter 01:	Pass
01: Initial Link Training at maximum link rate and lane count success	Pass
02: For Timing 1920x1080p@30Hz bpc 8 bpp 8.0 CRC check or Visual check verification	Pass
03: For Timing 1920x1080p@30Hz bpc 8 bpp 8.125 CRC check or Visual check verification	Pass
04: For Timing 1920x1080p@30Hz bpc 8 bpp 8.250 CRC check or Visual check verification	Pass
05: For Timing 1920x1080p@30Hz bpc 8 bpp 8.375 CRC check or Visual check verification	Pass
06: For Timing 1920x1080p@30Hz bpc 8 bpp 10.0 CRC check or Visual check verification	Pass
07: For Timing 1920x1080p@30Hz bpc 8 bpp 10.125 CRC check or Visual check verification	Pass
08: For Timing 1920x1080p@30Hz bpc 8 bpp 10.250 CRC check or Visual check verification	Pass
09: For Timing 1920x1080p@30Hz bpc 8 bpp 10.375 CRC check or Visual check verification	Pass
10: For Timing 1920x1080p@30Hz bpc 10 bpp 8.0 CRC check or Visual check verification	Pass
11: For Timing 1920x1080p@30Hz bpc 10 bpp 8.125 CRC check or Visual check verification	Pass

Open ACA Data 5.6.1: DSC capability verification

Instrument: PC9808 [10.30.196.17]

Continue Test Execution

Close

# Compliance Tests – Example 3

## ◆ Compliance Testing Provides:

- ◆ Required test suites to obtain industry logo.
- ◆ Detailed test results and logs that provide insight into the cause of failures.

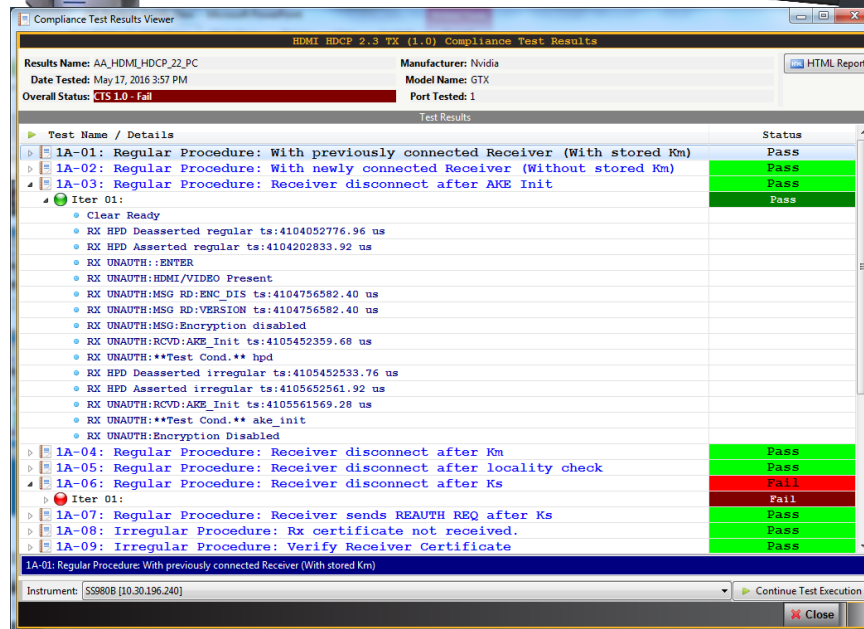
## ◆ Example:

- ◆ HDCP 2.2/3 compliance for DisplayPort source devices.

DP 1.4/2.0 source



M42d Video Analyzer/Generator

Compliance Test Results Viewer

HDMI HDCP 2.3 TX (1.0) Compliance Test Results

Results Name: AA\_HDMI\_HDCP\_22\_PC      Manufacturer: Nvidia  
 Date Tested: May17, 2016 3:57 PM      Model Name: GTX  
 Overall Status: **TIS 1.0 - Fail**      Port Tested: 1

HTML Report

Test Name / Details	Status
1A-01: Regular Procedure: With previously connected Receiver (With stored Km)	Pass
1A-02: Regular Procedure: With newly connected Receiver (Without stored Km)	Pass
1A-03: Regular Procedure: Receiver disconnect after AKE Init	Pass
Iter 01:	Pass
Clear Ready	
RX HPD Deasserted regular ts:4104052776.96 us	
RX HPD Asserted regular ts:4104202833.92 us	
RX UNAUTH::ENTER	
RX UNAUTH:HDMI/VIDEO Present	
RX UNAUTH:MSG RD:ENC_DIS ts:4104756582.40 us	
RX UNAUTH:MSG RD:VERSION ts:4104756582.40 us	
RX UNAUTH:MSG:Encryption disabled	
RX UNAUTH:RCVD:AKE_Init ts:4105452359.68 us	
RX UNAUTH:**Test Cond.** hpd	
RX HPD Deasserted irregular ts:4105452533.76 us	
RX HPD Asserted irregular ts:4105652561.92 us	
RX UNAUTH:RCVD:AKE_Init ts:4105561569.28 us	
RX UNAUTH:**Test Cond.** ake_init	
RX UNAUTH:Encryption Disabled	
1A-04: Regular Procedure: Receiver disconnect after Km	Pass
1A-05: Regular Procedure: Receiver disconnect after locality check	Pass
1A-06: Regular Procedure: Receiver disconnect after Ks	Fail
Iter 01:	Fail
1A-07: Regular Procedure: Receiver sends REAUTH REQ after Ks	Pass
1A-08: Irregular Procedure: Rx certificate not received.	Pass
1A-09: Irregular Procedure: Verify Receiver Certificate	Pass
1A-01: Regular Procedure: With previously connected Receiver (With stored Km)	

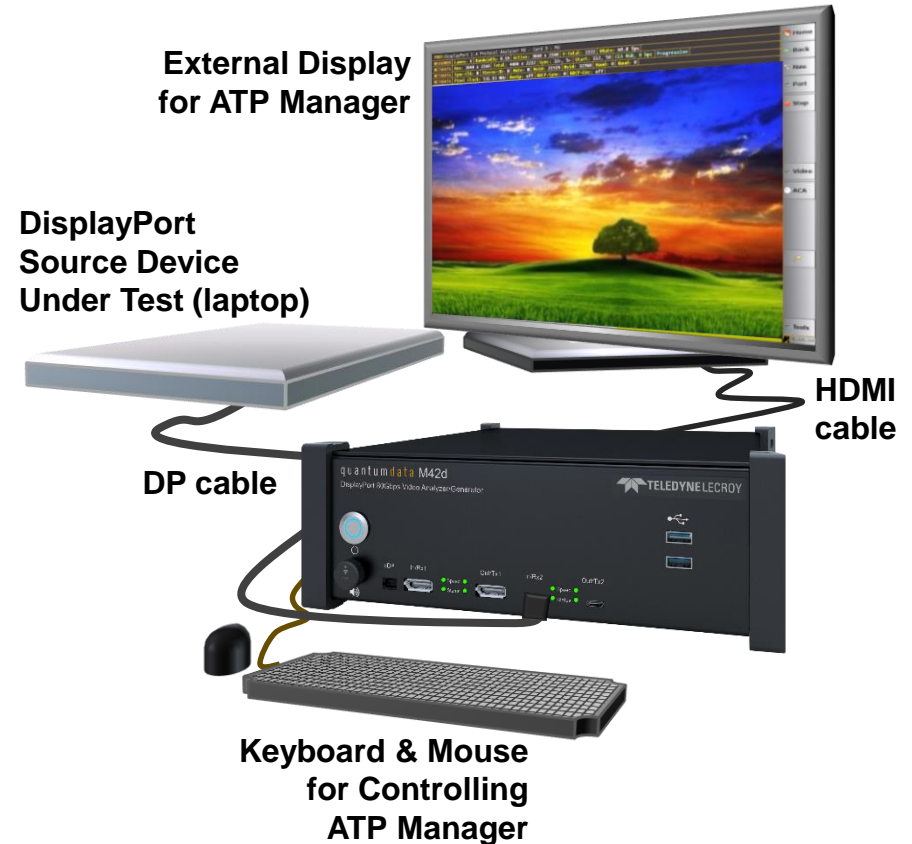
Instrument: [5980B [10.30.196.240]]      Continue Test Execution

Close

# M42d Test Setup – DisplayPort 2.0 Source Testing

## ◆ Source testing

- ◆ Use connected HDCP 2.2/3 compatible display to view M42d ATP Manager Graphical User Interface.
- ◆ Connection to the HDMI port on back of M42d.
- ◆ Use Keyboard and mouse to control ATP Manager GUI running on the connected display.

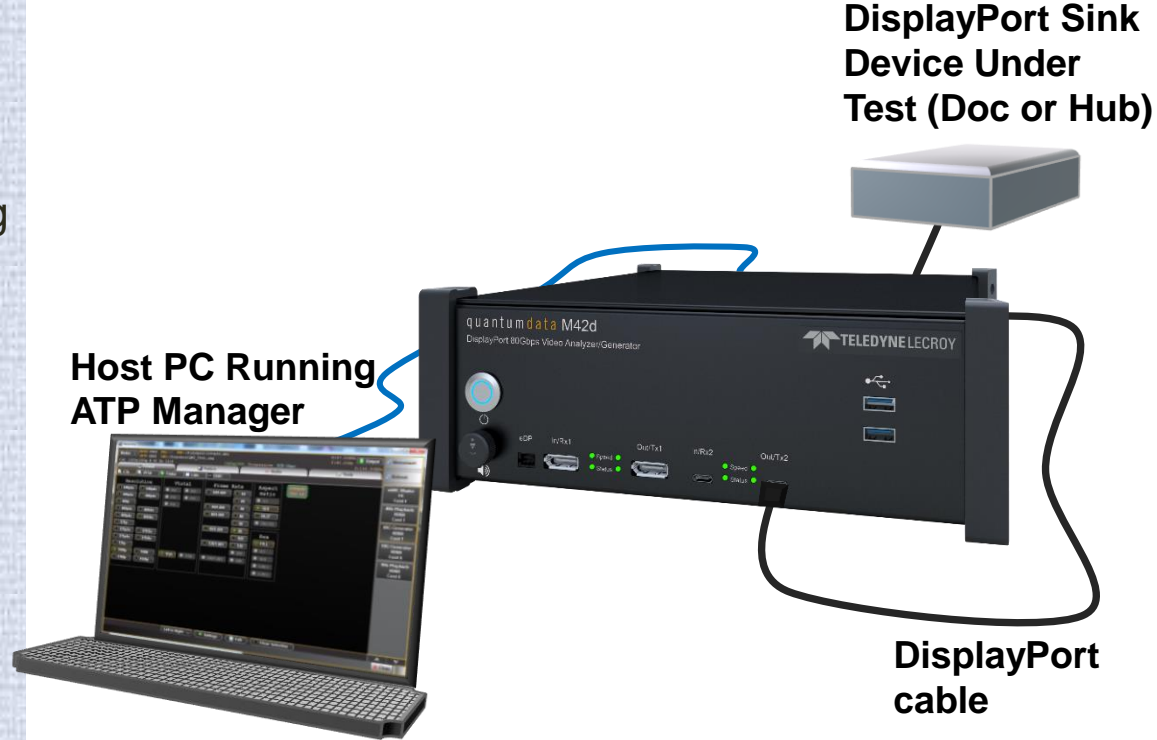




# M42d Test Setup – DisplayPort 2.0 Sink Testing

## ◆ Sink testing

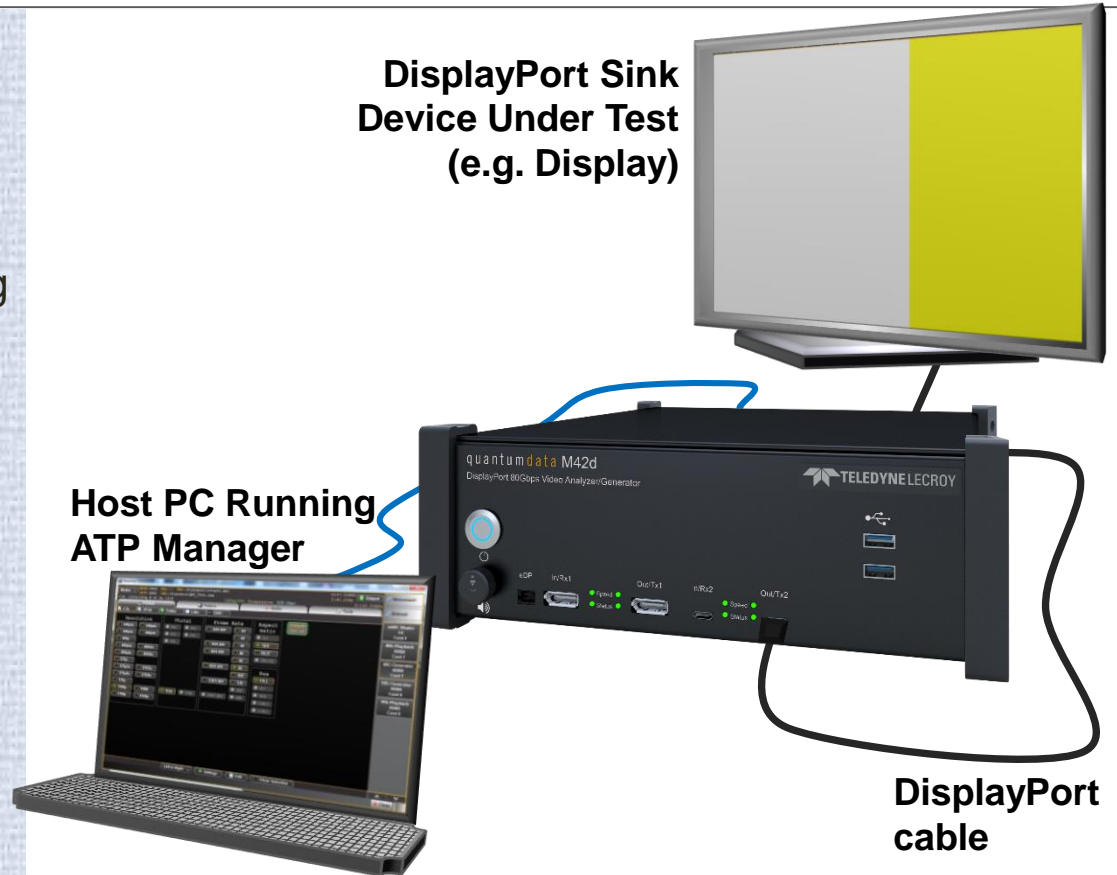
- ◆ Use connected M42d ATP Manager graphical user interface installed on host PC.
- ◆ Use Keyboard and mouse to control ATP Manager GUI running on the connected display.
- ◆ Connect Host PC to M42d via Ethernet cable, either direct or through corporate LAN.
- ◆ Example: Sink hub or docking station.



# M42d Test Setup – DisplayPort 2.0 Sink Testing

## ◆ Sink testing

- ◆ Use connected M42d ATP Manager graphical user interface installed on host PC.
- ◆ Use Keyboard and mouse to control ATP Manager GUI running on the connected display.
- ◆ Connect Host PC to M42d via Ethernet cable, either direct or through corporate LAN.
- ◆ Example: High resolution display.



# M42d Test Setup – DisplayPort Passive Monitoring Source/Sink

- ◆ **Passive Monitoring – Aux Chan**
  - ◆ Monitor the Aux Channel between a DP 1.4/2.0 source and sink device.
  - ◆ View Link Training, EDID exchange, HDCP authentication between a source and sink through Aux Channel Analyzer utility.
- ◆ **Passive Monitoring – Main Link**
  - ◆ Monitor the Main Link between a DP 2.0 source and sink device up to 20Gbps lane rate.
  - ◆ View video, audio, control, metadata and symbol data through the basic analyzer viewer and the Capture Viewer.

